Microsemi Application Note
AN-13

LX1686 Direct Drive CCFL Inverter Design Reference

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Contents

1.0 INTRODUCTION

Two equally important but technically diverse components determine overall performance, reliability and cost of CCFL inverters. One is the control integrated circuit; the other is the high voltage transformer. Since Microsemi is the only manufacturer that designs and manufactures both of these critical components, we alone are able to develop completely optimized modular solutions.

Microsemi Microelectronics has created the next generation in CCFL inverter topology with its patented new **LX1686** Direct Drive integrated circuit architecture. The **LX1686** backlight controller IC provides all the control functions necessary to implement Microsemi Direct Drive CCFL inverters . CCFLs are used for back or edge lighting of liquid crystal flat panel displays (LCD's) and typically find application in notebook computers, web browsers, automotive and industrial instrumentation, and entertainment systems. This IC can be used to control single or multiple lamp configurations.

This application note provides a guide for using this new control circuit in your module and magnetic designs. A comlete functional description of the chip is included, along with an applications information section in which typical module schematics are explained as an example to designers.

Direct Drive offers distinct advantages over conventional Buck/Royer inverters. These advantages are illustrated with practical examples and comparisons so that you may make informed decisions about which technology is best for your application.

The **LX1686** backlight controller IC includes a PWM (Pulse Width Modulation) controlled lamp current burst circuit that can provide greater than a 100:1 dimming range from a simple zero to 2.5V potentiometer input. The lamp current burst rate may be easily synchronized to the LCD panel's frame rate to prevent interference from optical beating between the two frequencies.

Safety and reliability features include dual feedback loops that permit regulation of maximum strike voltage as well as lamp current. Regulating maximum lamp voltage permits the designer to simultaneously provide for ample worst case lamp voltage while conservatively limiting maximum open circuit voltage.

An innovative new strike voltage generation technique enables the module designer to optimize high voltage transformer design for maximum efficiency while the lamp is ignited. The high voltage drop on the output ballast capacitor needed for Royer oscillators is much less, reducing transformer size and power dissipation.

LX1686 FEATURES

- RangeMAX™ Wide Range Dimming (>100:1)
- Dimming Burst Rate Synchronizable to Display Video Frequency
- High Voltage Feedback Loop Regulates Maximum Open Lamp and Minimum Strike Voltages
- Transformer Protected from Overheating During Lamp Striking
- Micro-Amp Sleep Mode
- User-Programmable Fixed Frequency Operation
- Under-Voltage Lockout Feature with Power-Up Reset
- Built-In Soft-Start Feature
- Operates with 3.3V or 5V Power Supplies
- 50mA Output Drive Capability

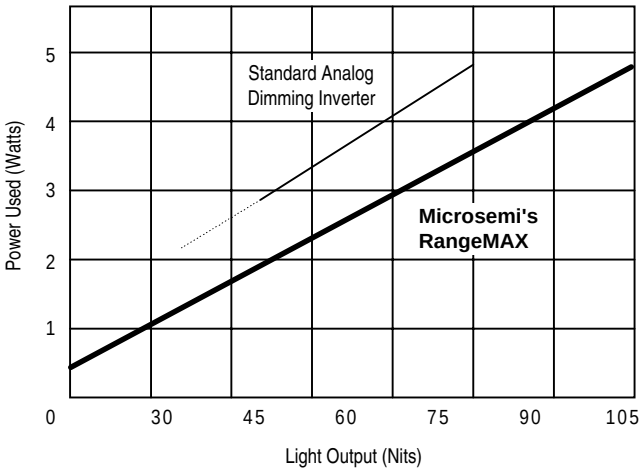
APPLICATIONS

- Notebooks
- Instrumentation Displays
- Desktop Computer Monitors
- Low Ambient Light Displays (Used in Aircraft, Automobiles and Hand-Held Equipment)

BENEFITS

- Extremely High Efficiency from 3.3V, 5V and 12V Power Supplies
- Lower Cost than Conventional Buck/Royer Inverter Topologies
- Patented Strike Voltage Generation Method Ensures Lamp Ignition While Increasing Efficiency
- Fool-Proof Output Voltage Regulation Prevents Over-Voltage Failures

RangeMAX vs. Analog Dimming



2.0 WHAT IS DIRECT DRIVE?

"Direct Drive" refers to the ability of Microsemi's new architecture to eliminate the inductor and resonant capacitors necessary to implement a conventional Royer oscillator based inverter solution. Instead, Direct Drive topology uses a fixed frequency PWM control circuit connected *directly* to a high voltage transformer primary via a pair of N-FET *drivers*. Removing these costly and power-hungry components simultaneously improves module cost, efficiency and size.

A two transistor N channel drive scheme was selected over popular bipolar and complementary P/N channel FET drives for three significant reasons:

- Using ground referenced transistors in conjunction with "push-pull" transformer operation permits the IC to be implemented with a low cost 5V fabrication process such as CMOS. This process permits the smallest die size, very high performance, and direct compatibility with 5V and 3.3V system power buses. The IC can interface through external N-FETs to any system voltage desired by simply changing the high voltage transformer turns ratio. Thus, an operating input voltage range for the module from 3V to more than 50V is possible.
- N-FETs are significantly more efficient switches than bipolar transistors or P-FETs of equal size and cost.
- Dual N-FETs are readily available in small surface mount packages at prices that compete favorably with the installed cost of bipolar transistors and their required additional circuit components.

Direct Drive topology is a non-resonant, fixed frequency PWM regulation method for operating CCFLs. The **LX1686** allows a wide choice of operating frequencies to match the lamp's most efficient operating point, and to minimize high frequency interference.

High Voltage Transformers for Direct Drive

Direct Drive's push-pull transformer design provides important technical advantages when used in low voltage applications such as notebook computers and hand-held battery operated products.

Because of its dual primary winding construction, the voltage impressed across the primary in Direct Drive modules is twice the supply voltage. This is electrically equivalent to a four transistor "full or H-bridge" drive configuration and makes for very efficient operation at low voltages. Direct Drive topology enables efficient inverters that can run directly from 3.3 and 5V logic supplies now common in LCD panels.

Unlike Royer oscillator implementations, Microsemi's new approach for lamp strike voltage generation relieves the transformer from operating continuously at full lamp strike voltage once the lamp is ignited. Direct Drive transformers can be optimized for normal operation where they spend most of their life. Transformers can be smaller while system reliability is improved because the extra high voltage required to strike a CCFL is only present for the instant it is required. High voltage corona discharge, which gradually destroys insulation material, can be more easily avoided with Direct Drive designs (see the detailed description of strike voltage generation below).

Microsemi has developed completely new transformers to be used with our LX1686 control IC. The first two are 6 watt units that can drive lamps having strike voltages of up to 1800Vrms. The smaller of these permits modules to be built with maximum profiles of 10.5mm wide by 6mm high while operating at a very conservative 18V per mil voltage stress in air. Microsemi develops and works with other world class manufacturers to develop transformers for other applications as needed. A two lamp magnetic now in development will support up to 2500Vrms strike and 12W operating power. A magnetic design guide is included in this note to help you design your own magnetics if ours do not meet your exact needs.

Designing for Cost

Continuous cost reduction is a way of life in the computer industry. Higher performance at ever decreasing cost is fundamental for success. Direct Drive topology takes this principle and applies it to LCD backlighting. For fixed input voltage dimmable inverter applications, the Microsemi solution provides the most efficient, least expensive, and smallest size available. Coupled with a step-down input voltage regulator, Direct Drive can handle extremely wide input voltage range applications while providing higher reliability and more features per dollar than older technologies.

Lamp Strike Voltage Generation

Prior to the introduction of Direct Drive technology, the need to generate strike voltages more than twice the operating voltage of a lamp have limited transformer size reduction. The number of lines of flux required to generate strike voltage governs transformer minimum size. The number of lines of flux available in a magnetic structure is directly proportional to both core cross-section (Ae), and operating frequency.

Instead of increasing the physical size of the transformer, Microsemi chose to increase frequency, but only during lamp strike time when very high voltage output is needed. This allows the transformer to be sized for normal run voltages, resulting in a smaller design for a given power level. Smaller core structures have lower losses which helps improve inverter efficiency.

The LX1686 integrated circuit ramps operating frequency slowly up and down over a user adjustable range when the open lamp sense input (OLSNS) indicates the lamp is not ignited. The high voltage transformer and output capacitance have an unloaded self-resonant frequency that is higher than normal operating frequency. As strike frequency is increased, unloaded resonance is approached, resulting in a resonant rise of voltage across the output capacitance of the lamp, and the lamp is ignited. Since the unloaded resonance circuit has a high Q, typically in the range of 5 to 10, it is easy to generate very high strike voltages. At the same time, transformer flux density is maintained at low levels due to the higher frequency, preventing magnetic saturation.

This technique also solves the problem of the lamp's parasitic capacitance to ground forming a voltage divider with the ballast capacitor placed between the transformer secondary and the lamp.

In Royer oscillator designs, the lamp ballast capacitor is usually in the range of 12 to 22 pico Farad in order to drop excess transformer output voltage after the lamp has ignited. Direct Drive designs reduce transformer output voltage after ignition, permitting ballast capacitance values to be much larger.

The 100nF ballast (In this application it is really a DC bypass cap) typically used in Direct Drive transfers far more of the available transformer voltage to the lamp. For example, if a 22pF the available transformer voltage to the lamp. For example, if a 22pF ballast capacitor is used for a backlight assembly with 10pF of parasitic capacitance across the lamp, only 69% of the voltage generated by the transformer is available to strike the lamp. If this same back light assembly uses a 100nF ballast, 100% of available voltage is impressed across the lamp at strike time. Said another way, the Direct Drive transformer needs to develop only 6% more output than maximum lamp voltage, while the Royer design must develop 31% more! Clearly, strike capability is enhanced while transformer size and reliability are improved.

Standard Safety Features

Microsemi's new Direct Drive controller includes an active open circuit voltage regulation feedback loop to prevent hazardous voltages, even if the lamp is removed from the circuit. When an open lamp condition is detected, the controller automatically enters strike mode as described above, and at the same time operates at 50% duty cycle to limit average power dissipation of the module to levels that can be maintained indefinitely. The module designer can select the open circuit voltage regulation point by choosing values of a non-dissipative capacitor voltage divider placed on the output terminals.

Lamp short circuit protection is inherent because lamp current is regulated even when lamp voltage is zero. Shorts from either lamp terminal to ground may also be protected by sensing all or part of the lamp current at the low voltage end of the transformer secondary winding.

RangeMAX Digital Dimming

The LX1686 provides both current *amplitude modulated* dimming circuitry, which typically achieves between 3:1 and 5:1 dimming range and "Range MAX" *time modulated* lamp current circuitry that can easily achieve dimming ratios of 100:1. While duty cycle control of CCFL lamp current is not new, the LX1686 is the first CCFL control IC to completely integrate the function. The user interface for both dimming modes is the familiar DC control voltage or potentiometer.

Amplitude modulation brightness control differences a 0 to 2.5V (or optionally a 2.5 to 0V) analog brightness control voltage from a voltage developed by sampling current flow through the lamp. The resulting error signal is used to regulate lamp current amplitude between user definable minimum and maximum values.

In Digital Dimming mode, the same analog brightness control voltage is processed to modulate lamp current duty cycle. In this case, lamp current is either "on" at a user determined rms value, or off. The on-time duty cycle determines brightness of the lamp. Duty cycle can be controlled from nearly zero to 100% by the analog control voltage. Lamp brightness adjustment by duty cycle control is possible without the turn-on stress that occurs when the lamp is initially ignited, because the burst repetition rate is high enough to prevent lamp gasses from de-ionizing between current pulses.

The LX1686 "bursts" current on and off in a smooth and precisely controlled manner, eliminating turn-on overshoot that could shorten lamp life and pulse-to-pulse jitter that could cause flickering. An on-chip PLL can synchronize lamp current bursts to an external sync pulse connected to the FVERT pin. This feature is important in high quality displays because it prevents optically visible beat frequencies between the lamp burst rate and the video frame rate. When an external sync pulse is used, the PLL multiplies the external frequency by 2 resulting in a burst frequency twice the sync input frequency. If the FVERT pin is left floating, lamp current burst frequency will free run at approximately 260Hz.

3.0 A COMPARISON OF CONVENTIONAL "BUCK/ROYER" INVERTERS WITH MICROSEMI'S "DIRECT DRIVE" TOPOLOGY

BUCK / ROYER ADVANTAGES:

1. Step-down voltage regulator (Buck regulator) adjusts input voltage to Royer oscillator, providing both line and load regulation.
2. Lamp brightness is extremely insensitive to both static and dynamic input voltage changes. Conversion efficiency is fairly constant across input voltage range.
3. Self-resonant Royer oscillator (transformer, ballast cap, PPS cap) provides low crest factor sine wave current waveform to the lamp. CCFLs operate most efficiently with low (1.4 to 1.6) crest factors.

BUCK / ROYER DISADVANTAGES:

1. Requires more components, resulting in higher cost and larger size.
2. Four power semiconductors, two power inductors and one PPS (Poly Phenelene Sulfide) high current capacitor burn power, reducing conversion efficiency. Very high quality components can be selected to regain some of these power losses, but high cost premiums and larger size must be paid.
3. Open circuit voltage is very difficult to limit due to multiple resonances in the power circuit, lack of voltage feedback, and lack of frequency control from the controller IC. These circuits are prone to arcing and self destruction when operated open circuit (lamp unplugged or broken).
4. Buck regulator and Royer oscillator operate asynchronously at different frequencies, making EMI and RFI more difficult to control.

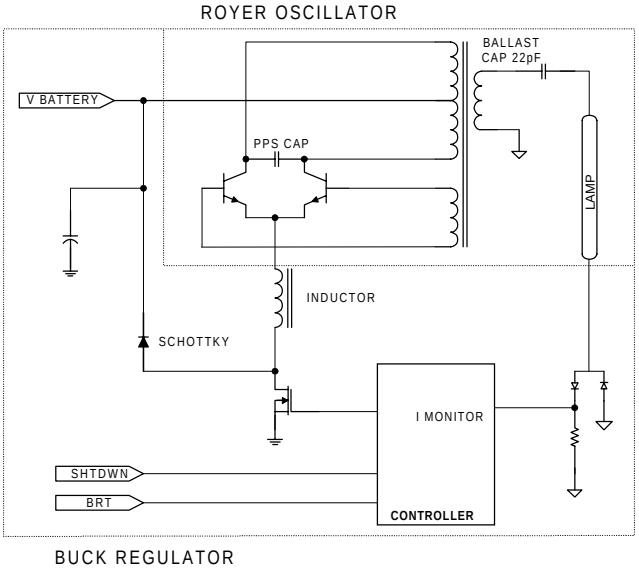


Figure 1: Buck/Royer Simplified Circuit

DIRECT DRIVE ADVANTAGES:

1. Single stage PWM power conversion requires only two power transistors to provide line and load regulation. A very high efficiency dual N-Channel FET in an SO-8 package handles up to 10W.
2. Non-resonant, fixed frequency drive eliminates inductor and high current resonant capacitor, reducing cost and size while increasing conversion efficiency.
3. Simplified high voltage transformer has one less winding and two less pins (smaller form factor = lower cost).
4. Higher value ballast cap requires less transformer output voltage while lamp is ignited for additional efficiency and/or smaller size transformer is realized.
5. Active open circuit output voltage regulation is achieved via non-dissipative capacitor feedback from the transformer, eliminating open circuit hazards forever without costly (and sometimes ineffective) thermal protection devices being thermally bonded to the power transformer.

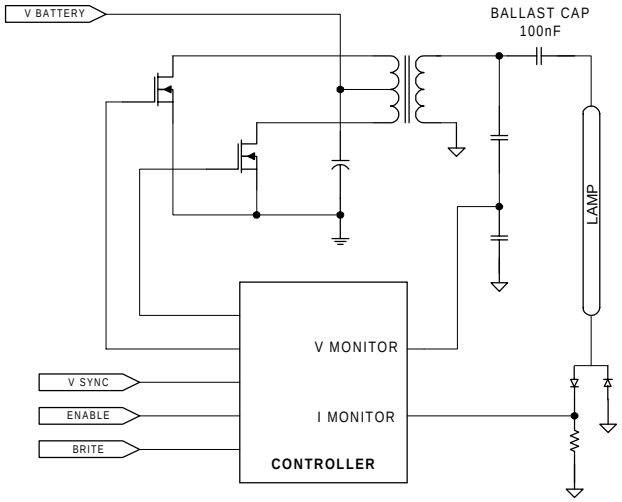


Figure 2: Direct Drive Simplified Circuit

DIRECT DRIVE DISADVANTAGES:

1. PWM regulation causes high lamp current crest factors when input voltage is more than 1.5 times the design minimum. This reduces nits/watt efficiency at high-line to approximately the same as a typical Buck/Royer design. At low-line (battery voltage levels) efficiency is 10-30% higher than Buck/Royer inverters. Direct Drive efficiency is so high at 5V and 3.3V that it makes up for Buck regulator losses in notebook systems, yielding comparable overall system efficiency while completely eliminating the disadvantage of high crest factors at high input voltages.

4.0 THE LX1686 CCFL CONTROLLER IC

Block Diagram

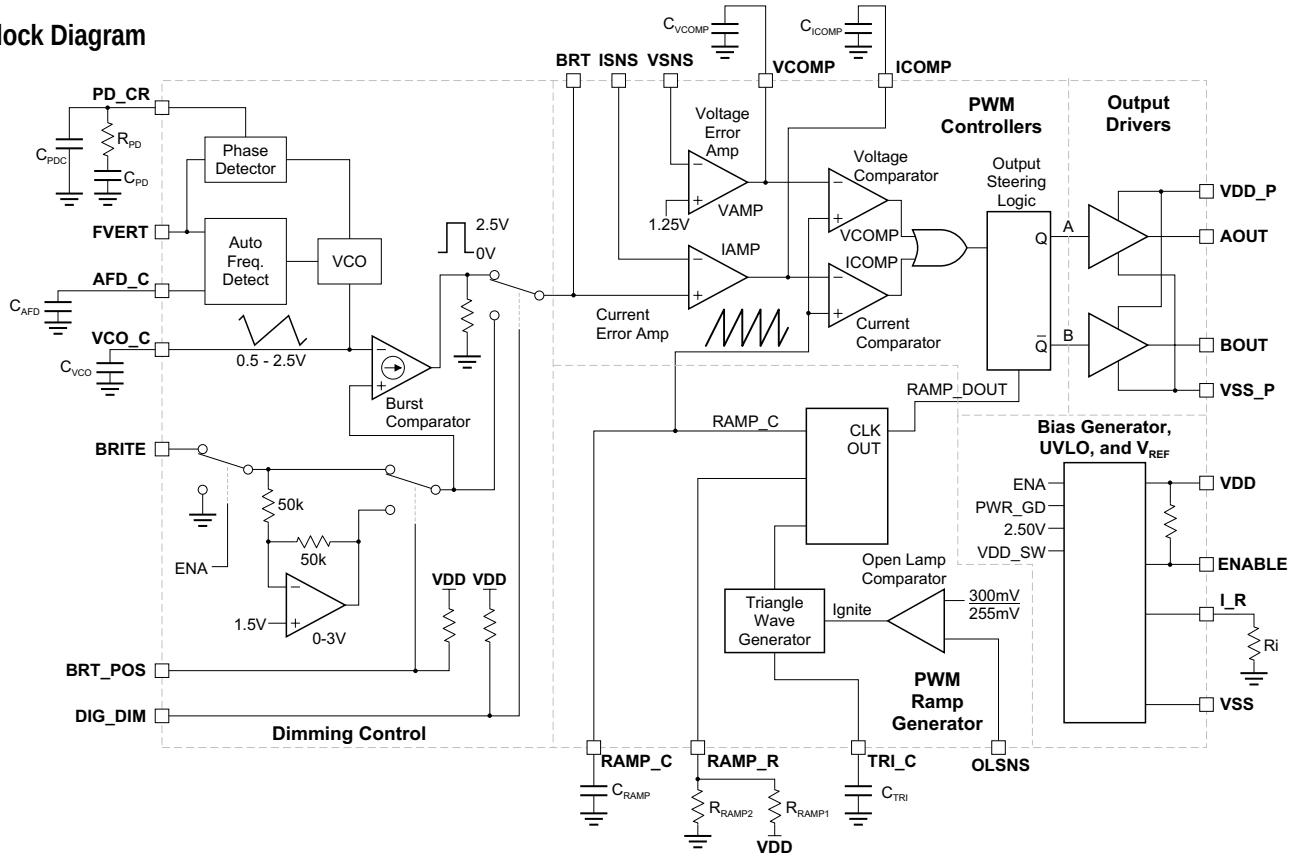


Figure 3: LX1686 Simplified Block Diagram

Dimming Control

- Performs the frequency locking for a $2V_{PP}$ ramp oscillator with oscillation frequency that locks to the LCD display vertical scanning frequency. Frequency locking is done by a 3rd order phase-lock loop formed by the phase detector, VCO and the divide-by-2 TF/F. The phase detector is a 3-state charge pump type that allows easy filtering and loop compensation. The VCO is a voltage-controlled ramp oscillator with fixed output voltage levels (0.5 to 2.5V). When there is no external FVERT detected by the Auto-Freq-Detector, the VCO will oscillate at 5.5/10.5 its maximum frequency. The VCO can be forced to oscillate at 5.5/10.5 of its maximum oscillation frequency by grounding Pin AFD_C.
- Performs BRITE voltage inversion (determined by BRT_POS pin voltage) and passes the converted voltage to BRT for analog and digital dimming. The BRITE signal is buffered by a MUX before connection to the internal op amp so that during SLEEP Mode or Power-Down, BRITE is isolated from internal circuitry to ensure no chip biasing occurs through the BRITE pin.
- Performs the generation of a digital dimming PWM signal derived from the VCO's ramp output with the burst comparator and the external analog DC input (BRITE) as shown in the timing diagram Figure 4. When digital dimming is selected, this signal is used to generate a 2.5V pulse muxed to port BRT. When analog dimming is selected, then either BRITE's DC voltage or its inversion will be muxed to the BRT port.
- Pin BRT_POS is used to control BRITE polarity during digital and analog dimming. When BRT_POS is "1", the regulated lamp current will be proportional to BRITE's voltage. When "0", the current will be inversely proportional to BRITE's voltage.

PWM Ramp Generator

- Performs the generation of a 2 V_{PP} ramp oscillator whose oscillation frequency can be changed through the voltage imposed on the input port TRI_C as shown in Figure 5. When TRI_C voltage is below 1.5V, the ramp oscillates at the normal run frequency. When TRI_C is above 1.5V, the ramp oscillation frequency will be proportional to V_{TRI_C}. When TRI_C is at 2.25V, the ramp will oscillate at a higher frequency, depending on the R_{RAMP} value. This ramp oscillator provides 2 timing signals for the controller: analog ramp output RAMP_C and digital ramp output RAMP_DOUT. Both of these outputs are used by the controller PWM block, in conjunction with the dimming output BRT, to create two digital PWM outputs (AOUT and BOUT) that operate in push-pull fashion.
- Performs frequency sweeping during CCFL startup mode (pre-strike) and run mode (post-strike). The tasks are performed and controlled by an approximately 10Hz triangular wave generator. The triangular analog output (V_{TRI_C}) swings from 0.75 to 2.25V. Normally, V_{TRI_C} will be reset at 0V, waiting to be ramped up. When the lamp is off,

detected by pin OLSNS, the triangular wave generator will start to ramp up. It takes about 25ms to ramp up to 1.5V; this time is used for the PWM block to settle out such that it can perform lamp current regulation. After reaching 1.5V, V_{TRI_C} will continue to ramp up and increase the RAMP_C frequency. Increase in ramp frequency will increase lamp voltage due to the CCFL backlight transformer parasitic LC resonance. Increase in lamp voltage will in turn improve lamp ignition probability. After the lamp ignites, detected again by OLSNS, V_{TRI_C} will start ramping down and decrease the RAMP frequency slowly back to nominal. Lamp ignition is indicated by an internal signal called IGNITE. The lamp striking timing and sequence are illustrated in Figure 6. If the lamp fails to ignite when V_{TRI_C} reaches 2.25V, V_{TRI_C} will ramp down. During this ramp down time AOUT and BOUT signals are turned OFF to prevent transformer overheating.

- Both the ramp generator and the triangular wave generator are reset during low power supply voltage.

PWM Controllers

- Performs voltage and current regulation functions. Timing is shown in Figure 7.
- Performs transformer output voltage regulation by comparator VCOMP and error amplifier VAMP. The error amplifier generates an error voltage derived from the voltage difference between VSNS and the internal 1.25V reference. The error voltage is compared with RAMP_C by VCOMP to generate two PWM signals (A, B) that drive two output buffers. These two buffers drive two external power FET switches that can increase or decrease the transformer output voltage. By feeding back the transformer voltage through pin VSNS, a negative feedback loop is formed to regulate the maximum transformer output voltage to a predetermined value.
- Performs lamp current regulation by comparator ICOMP and the error amplifier IAMP. The error amplifier generates an error voltage derived from the voltage difference between ISNS and BRT. The error voltage is compared by ICOMP with RAMP_C to generate two PWM signals (A, B) that drive the same two output buffers. By feeding back the lamp current through a sense resistor network to pin ISNS, a negative feedback loop is formed to regulate the lamp current to a set value determined by BRT voltage.
- All PWM flip-flops are reset and the VCOMP pin is discharged during power-up.

BIAS Generator

- Performs the power-down functions controlled by the ENABLE input. The power-down mode is activated by forcing ENABLE low. During the power-down mode, internal power supply voltage VDD_SW is turned off and no DC power is available to any internal circuitry except the ENABLE circuitry. The main source of Sleep Mode operating current is from the ENABLE pin internal pull-up resistor (100k to VDD).
- Performs the Under-Voltage-Lock-Out (UVLO) function. Internal ports PWR_BD and PWR_GD are used to indicate whether VDD voltage is acceptable for reliable internal circuit operation. PWR_BD and PWR_GD are valid when VDD voltage is above 1.3V. VDD_P voltage is not monitored.
- Performs voltage and current bias generation. An internal 2.5V voltage regulator for precision voltage biasing is generated by a bandgap circuit. An internal precision current bias is generated through an external resistor R_I at pin I_R. This precision current bias is copied four times and distributed to four circuit blocks.

Output Drivers

- Performs buffering function for the signals A and B from the PWM block.
- Port PWR_BD is used to ensure pins AOUT and BOUT will stay low during power startup or when VDD voltage is below the UVLO threshold (about 2.8 V).
- Pins VDD_P and GND_P are used to isolate high-current power and ground from the low signal power and ground terminals (VDD, GND). This is done to reduce switching noise coupling.

Timing Diagrams and Wavforms

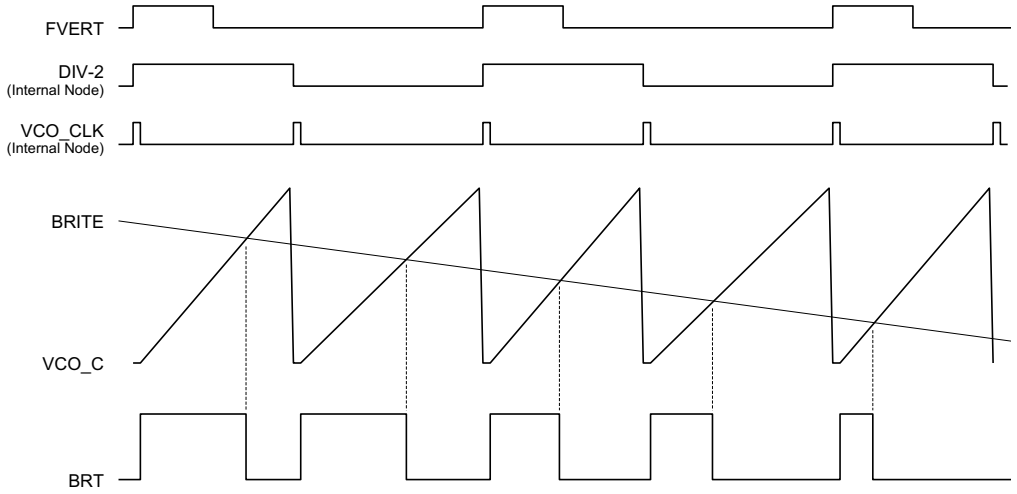


Figure 4: Digital Dimming Timing Diagram

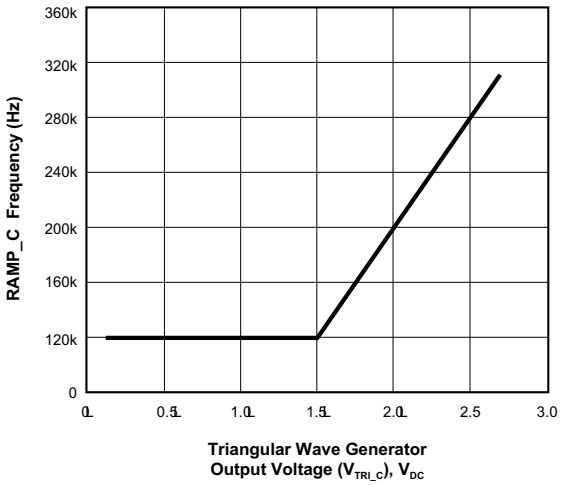


Figure 5: RAMP_C Frequency vs. V_{TRI_C}

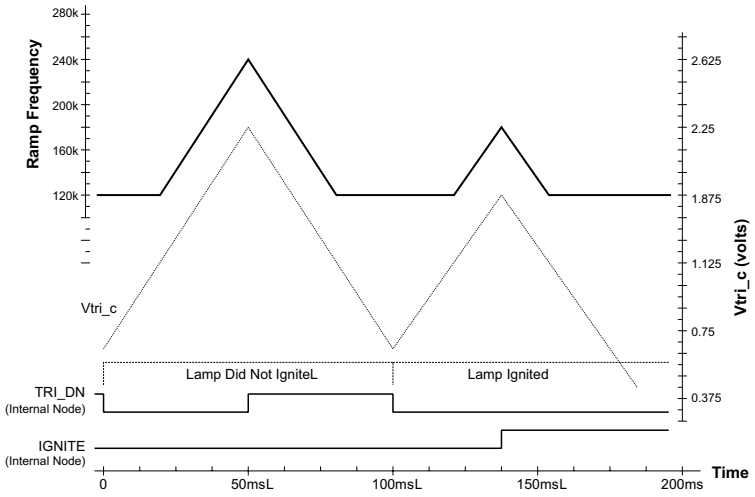


Figure 6: Lamp Ignition Timing Diagram

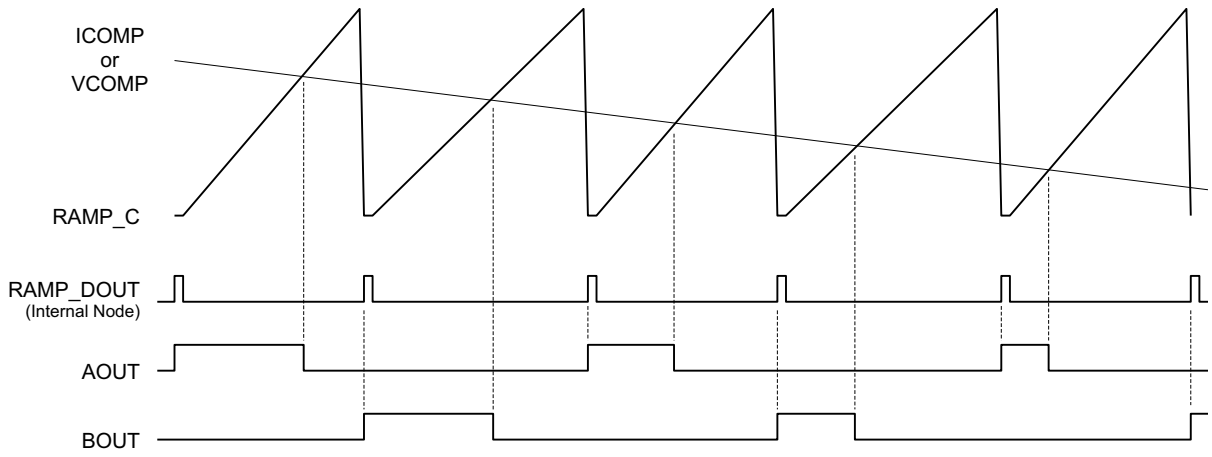
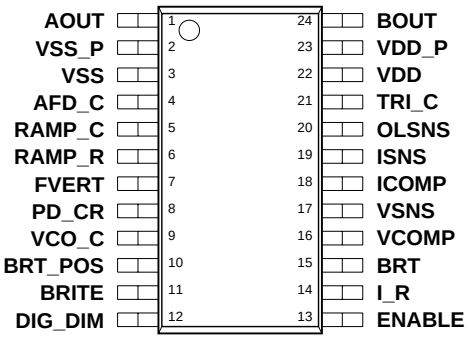


Figure 7: Direct Drive PWM Regulation TIming Diagram

4.2 FUNCTIONAL PIN DESCRIPTION

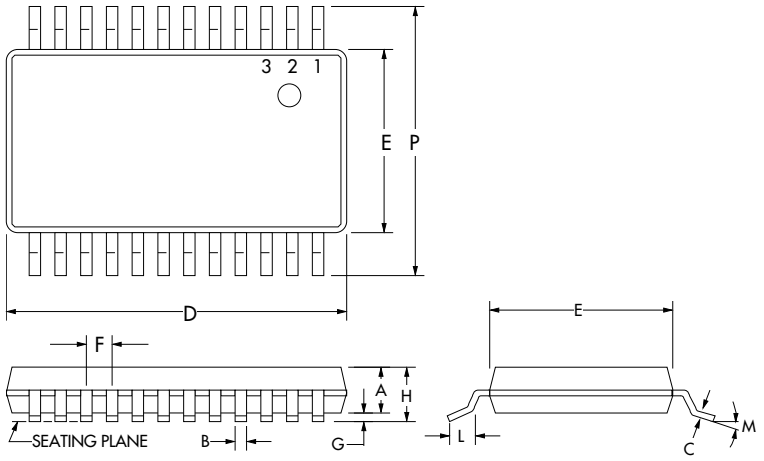
Pin Number	Pin Designator	Description
1	AOUT	Output driver A.
2	VSS_P	Power ground for output drivers only.
3	VSS	Signal ground.
4	AFD_C	Connects to an external cap, C_{AFD}. Forcing to ground or VDD will make the VCO oscillate at approximately 50% of the maximum VCO frequency. Forcing to VDD/2 will make the VCO oscillate at 2x the FVERT frequency.
5	RAMP_C	Connects to external capacitor C_{RAMP} for setting Direct Drive PWM operating frequency.
6	RAMP_R	Connects to external resistor R_{RAMP} for setting Direct Drive PWM operating frequency.
7	FVERT	Vertical frequency reference digital input. Has internal pull down.
8	PD_CR	Phase Detector Filter. Part of phase lock loop. Connects to external capacitor and resistor network.
9	VCO_C	Connects to external capacitor C_{VCO}.
10	BRT_POS	Brightness polarity control. Has internal pullup. Leave open or pull up to VDD for dimming brightness proportional to BRITE voltage, connect to ground for brightness inversely proportional to BRITE voltage.
11	BRITE	Analog voltage input for brightness control.
12	DIG_DIM	Digital Dimming Enable internal pullup. Leave open or pull up to VDD for operating in digital dimming mode. Connect to ground for analog dimming mode.
13	ENABLE	Chip Enable internal pullup. High enables the chip. Low disables.
14	I_R	Current Reference Resistor. External resistor to ground (Ri) determines internal reference currents.
15	BRT	Current Error Amplifier non-inverting input.
16	VCOMP	Voltage Error Amplifier output. Connects to external frequency compensation capacitor C_{VCOMP}. Controls soft-start timing. C_{VCOMP} not needed for amplifier stability.
17	VSNS	Voltage Error Amplifier inverting input.
18	ICOMP	Current Error Amplifier output. Connects to external frequency compensation capacitor C_{ICOMP}. C_{ICOMP} not needed for amplifier stability.
19	ISNS	Current Error Amplifier inverting input.
20	OLSNS	Open Lamp Sense Input. Lamp assumed ingnited if $V_{OLSNS} \geq 300mV$.
21	TRI_C	Connects to external capacitor C_{TRI} for setting strike frequency ramp slope.
22	VDD	VDD
23	VDD_P	Dedicated VDD for output buffers only.
24	BOUT	Output driver B.



PW PACKAGE
(Top View)

Figure 8: Pin Diagram

4.3 PACKAGE DIMENSIONS



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.85	0.95	0.033	0.037
B	0.19	0.3	0.007	0.012
C	0.09	0.2	0.0035	0.008
D	7.7	7.9	0.303	0.311
E	4.3	4.5	0.169	0.177
F	0.65 BSC		0.025 BSC	
G	0.05	0.15	0.002	0.005
H		1.1		0.0433
L	0.5	0.75	0.02	0.03
M	0	8	0	8
P	6.4 BSC		0.252 BSC	
*LC		0.1		0.004

* Lead Coplanarity

Note:

1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.15mm (.006") on any side. Lead dimension shall not include solder coverage.

Figure 9: PW (TSSOP) 24-pin Package Dimensions

4.4 BIAS & TIMING EQUATIONS REFERENCE

Equation 1: $I\_PD = I\_VCO = I\_RAMP = I\_TRI \frac{1.0V}{Ri}$ [A]

Where I_PD, I_VCO, I_RAMP and I_TRI are internal nodes. Capacitor charge currents flowing out of PD_CR, VCO_G, RAMP_C and TRI_C are various multiples of the current flowing in Ri. These multiples are taken into account in the following equations.

Equation 2: Triangular Wave Generator Frequency

$$F_{TRI} = \frac{1}{(30 \cdot Ri \cdot C_{TRI})} \text{ [Hz]}$$

Equation 3: Ramp Generator Frequency, F_{RAMP} in Hz

If $V_{TRI\_C} \le 1.5V$ then

$$F_{RAMP} = 0.72 \cdot \frac{(1 + VDD/20)}{(Ri \cdot C_{RAMP} + 0.5 \text{ sec})} = F_O$$

If $V_{TRI\_C} > 1.5V$ then

$$F_{RAMP} = (1 + 0.75 \cdot (V_{TRI\_C} - 1.5) \cdot (N - 1)) \cdot F_O$$

$$F_{RAMP\_MAX} = N \cdot F_O$$

where

$F_O = F_{RAMP}$ during run-mode (at V_{TRI_C} < 1.5V)

N = Maximum F_{RAMP} multiplier

Equation 4: N = Maximum Frequency Multiplier

$$R_{RAMP1} = \frac{VDD \cdot Ri}{4(N-2)}$$

$$R_{RAMP2} = \frac{VDD \cdot Ri}{\frac{8}{3}(N-1) \cdot VDD - 4 \cdot (N-2)}$$

Equation 5: Maximum VCO Frequency

$$F_{VCOMAX} = \frac{1}{(5 \cdot Ri \cdot C_{VCO})} \text{ [Hz]}$$

Equation 6: Maximum Phase Detector Output Current

$$I_{PD} = \frac{1}{10 \cdot Ri} \text{ [A]}$$

Equation 7: PLL PD High-Frequency Attenuation Capacitor

$$C_{PDC} = 0.1 \cdot C_{PD}$$

Equation 8: PLL Zero Time Constant

$$T_Z = R_{PD} \cdot C_{PD} \text{ [sec]}$$

Equation 9: PLL VCO Gain

$$K_{VCO} = 2 \cdot \frac{\pi}{(Ri \cdot C_{VCO})}$$

Equation 10: PLL Natural Frequency

$$W_N = (1/2) \cdot \sqrt{\frac{K_{VCO}}{(2 \cdot \pi \cdot N \cdot Ri \cdot C_{PD})}} \text{ [radian]}$$

$$W_N = \frac{1}{\left(2 \cdot Ri \cdot \sqrt{N \cdot C_{VCO} \cdot C_{PD}}\right)} \text{ [Hz]}$$

Equation 11: PLL Damping Factor

$$D_F = \left(\frac{T_Z}{2}\right) \cdot W_N$$

$D_F = 0.5 \cdot R_{PD} \cdot C_{PD} \cdot W_N$ [see Equation 8]

Equation 12: PLL Approximated Pull-In Time

$$T_P = \frac{(16 \cdot \pi)}{W_N} \text{ [sec]}$$

Equation 13: Auto-Frequency Detection Response Time

$$T_{D\_AFD} = 2{,}000{,}000 \cdot C_{AFD} \text{ [sec]}$$

Equation 14: Soft-Start Time

$$T_{SS} = 450{,}000 \cdot C_{VCOMP} \text{ [sec]}$$

Equation 15: Minimum Error Amp Bandwidth

$$BW_{EA\_MIN} = \frac{0.000048}{C_{ICOMP}} \text{ [Hz]}$$

5.0 DESIGNING INVERTER MODULES WITH THE LX1686

This section gives the design procedure for a typical inverter module similar to the Microsemi standard LXM1612-12-01. It is designed to operate from a single 10.8 to 13.2 volt power supply, and will drive a single lamp with a run voltage in the range of 550 to 750V_{RMS}. The inverter includes an on-board regulator to provide VDD for the LX1686, a zero power sleep mode circuit, and signal filtering on the BRITE input that will accept either DC voltages or a PWM logic input to control lamp current. Lamp current may be optionally controlled in either analog (amplitude modulated) or digital (duty cycle modulated) fashion. The schematic for this circuit is shown in Figure 10.

This design specifies an available Microsemi designed high voltage transformer. Please see Appendix A for information about designing custom transformers. Equations for calculating circuit component values are summarized in Section 4.5. Additional module variations follow this basic design.

Getting Started

First, select the bias current resistor for the LX1686. The value of R21 determines magnitude of four internal current sources that set timing parameters. These are phase detector slew rate; digital dimming burst oscillator frequency, triangle generator frequency, and main oscillator frequency. R21 is normally set around 40K ohms, but may be in the range of 20k to 60K. This design uses 43.2K 1%. While its value is not critical, R21 temperature coefficient should be very low to prevent parameter drift. Bias current is 1.00 volt divided by R21. Various ratios of this current will be sourced from pins 5, 8, 9, and 21. Note that this resistor affects all four functions stated, so it must be selected first.

Next decide if you will be using the analog or digital dimming method, and the polarity of the dimming signal. If you use digital dimming, connect pin 12 (DIG_DIM) to VDD. It may alternately be left open because it has an internal 100K pull-up to VDD. If you choose analog dimming mode, connect pin 12 to ground. This design has an optional jumper (R20) in the design to permit easily changing methods.

The LX1686 includes an amplifier that can be used to invert the sense of the BRITE pin. If pin 10 (BRITE_POS) is pulled up to VDD, lamp current will increase for increasing voltage on BRITE. If grounded, lamp current will increase for decreasing voltage on BRITE. This pin has an internal 100K pull-up as well, but may be terminated directly to VDD. This design also includes an optional jumper (R19) to permit easily reversing BRITE sense.

Now is a good time to consider filtering the IC power input pins. There are two VDD inputs, pin 22 (VDD) feeds all analog signals, and pin 23 (VDD_P) feeds only the output drive stage. These need to be filtered separately. We recommend 220nF ceramic capacitors on each pin (C2 And C3) although 100nF is sufficient if the trace layouts are very short and wide. VDD needs a 47 ohm resistor (R8) to help filter power stage switching transients from the analog control circuits. This is particularly important when using digital dimming, as any noise on the supply can act as an unwanted input at the BRITE pin and cause lamp current jitter. This will appear as lamp flicker.

C1 is added to reduce conducted emissions onto the power line. It should be a ceramic type with good high frequency characteristics, and must be located directly across the input connector power pins to be effective.

Generating An On-Board VDD Supply For The LX1686

The LX1686 can operate with VDD and VDD_P from 3.0 to 6.0V. If a supply in this range is not available, it can be generated on the inverter module. For best efficiency VDD should be high enough to fully enhance the FET (U2) at turn on. This design uses a 4.5 volt V_{GS} FET and sets VDD nominal at 5.3 volts to insure full enhancement under worst case component tolerances. If you are using less than a five volt supply, select a 2.7 volt V_{GS} FET for U2.

The VDD linear regulator must supply 7mA maximum operating current for the LX1686 plus another 5 to 10mA average for switching the FETs. Design for 17 mA to insure that worst case conditions are met.

A transistor switch circuit that is driven with the ENABLE input precedes the regulator. It removes VDD from the LX1686, eliminating its quiescent current drain when ENABLE is low. Remaining battery load is limited to leakage current of the three transistors and the filter capacitors.

Q1 and Q2 form a non-inverting high side switch that draws no current when the base of Q1 is less than 0.5 volts. R1 and R2, together with Q1 V_{BE} set input threshold to 2.0 volts. When Q1 turns on, Q2 saturates. R5 provides positive feedback to Q1 generating hysterisis to prevent partial turn on if input rise time is very slow. R6 and D1 establish a 6.2 volt reference that is buffered by emitter follower Q3. R7 is placed in series with Q3 collector to reduce its power dissipation. C2 is an X7R ceramic filter capacitor for VDD_P. R8 and C3, another X7R, filter switching noise from the LX1686 VDD input. Both C2 and C3 must be located so their connections to U1 use very short and wide traces.

$$V_{DD} = V_{D1} - Q1_{VBE} - R8 \cdot I_{VDD}$$

$$V_{DD} \cong 6.2 - 0.6 - 0.3 \qquad V_{DD} \cong 5.3V$$

Driving The ENABLE Input

In the example described directly above, ENABLE is connected to VDD so the LX1686 will be turned on when its power is applied. ENABLE may also be driven by a CMOS or TTL logic signal to cause the LX1686 to enter sleep mode. A low on this line is sleep and a high is active. If this later method is used, the switch circuit comprised of Q1 and Q2 is not needed. Instead, connect the open end of R6 to Vbat. Sleep current in this configuration will be approximately 1mA.

Logic Input Threshold Voltage

It is possible to have different voltages on VDD for the LX1686 and on the logic chip that drives ENABLE or other logic inputs such as FVERT and BRT_POS (as used in Figure 10). A common example is 5.3V on the LX1686 and 3.3V on its driver IC. Since logic threshold voltage for the LX1686 is VDD/2 + 0.6V, it will be necessary to provide a positive bias to the LX1686 inputs. Adding a 6.8K series resistor at the input terminal and a 10K pull-up to VDD at the LX1686 pin easily does this. R29 and R30 illustrate this circuit on the FVERT pin. Voltage on the FVERT pin will be 2.62V when the SYNC input is 0.8 volts and 3.93V when SYNC is at 3.0V. These values center the 3.3V FVERT threshold between worst case input levels from the driver.

Setting Main Oscillator Frequency

The main oscillator controls lamp current frequency. It is a linear ramp generator that runs at twice the frequency of the output stage. Two frequency limits must be programmed for this oscillator, F_{RAMP} and F_{RAMP_MAX}. When the inverter is operating normally with the lamp ignited, OLSNS will be greater than 300mV indicating lamp ignition.

This locks the oscillator at F_{RAMP}. F_{RAMP} is programmed by the values of R21 and C5. When the inverter is in 'strike mode' (lamp is not ignited) OLSNS will be less than 260mV, and oscillator frequency is placed under control of the voltage ramp on the TRI_C pin. As TRI_C voltage increases above 1.5 volts, frequency is slowly ramped to F_{RAMP_MAX}. The values of R13 and R14 determine F_{RAMP_MAX}. The equations below are written for a value N that is the ratio of maximum over minimum frequency. Most inverter designs should be set up for N = 3 to insure adequate strike voltage can be produced, e.g., open circuit resonance of the high voltage transformer and parasitic load capacitance can be reached during strike mode. N may be increased to as high as 5 for designs using very high turn's ratio transformers. These are generally needed for striking 1400Vrms or higher lamps from a very low input voltage such as a single cell Lithium-ion battery. It is a good idea to measure the resonant frequency of your transformer wired to its actual load before choosing 'N'. Units in the following equations are volts, ohms, farads, and Hertz.

$$F_{RAMP} = \frac{0.72\left(1+\frac{VDD}{20}\right)}{R21 \cdot C5 + 0.5 \cdot 10^{-6}}$$

$$C5 = \frac{0.72\left(1+\frac{VDD}{20}\right)}{R21(F_{RAMP})} - \frac{0.5 \cdot 10^{-6}}{R21}$$

$F_{RAMP\_MAX} = N \cdot F_O$, N = Maximum F_{RAMP} multiplier

$$R13 = \frac{VDD \cdot R21}{4\,(N-2)}$$

$$R14 = \frac{VDD \cdot R21}{\frac{8}{3}VDD\,(N-1) - 4\,(N-2)}$$

Using these equations to calculate values:

VDD = 5.3V (determined previously)

R21 = 43.2K (determined previously)

F_{RAMP} = 130KHz, N = 3 (assumed)

C5 = 152.36pF (Use 150pF, 5%, COG to allow for PCB trace capacitance and low T.C.)

R13 = 57.2K (Use 57.6K, 1% or 56K, 5%)

R14 = 9.44K (Use 9.53K, 1% or 10K, 5%)

Setting TRI_C Ramp Frequency

The signal at pin 21, TRI_C, controls the main oscillator frequency during the lamp striking process. TRI_C is low, near zero volts, when the lamp is operating. When in strike mode, TRI_C is a triangular waveform that varies between .75 and 2.25 volts. The frequency of the triangle wave is proportional to the value of C11, the capacitor on pin 21. Frequency should be in the range of 2 to 20Hz. For convenience, we use a 100nF X7R capacitor that gives an operating frequency of:

$$F_{TRI} = \frac{1}{30 \cdot R21 \cdot C11}$$

$$F_{TRI} = \frac{1}{30 \cdot 43.2K \cdot 0.1F} = 7.7Hz$$

$$C11 = \frac{1}{30 \cdot R21 \cdot F_{TRI}}$$

Driving The BRITE Input

The BRITE input connects to an inverting op amp (Av = -1) and a comparator. Depending on the state of BRT_POS, the comparator will be connected to either the input or the output of the op amp. In either case, the op amp output is connected to the BRITE pin through its feedback resistors. The resistors are each 50K ohms (See Figure 3 Block Diagram). Since the op amp will force its inverting input to be 1.5 volts independent of BRITE's voltage, the equivalent BRITE input circuit becomes 50K ohms terminated to a 1.5V power supply. Input current to the BRITE pin ranges from 0 to +/- 30µA, and flows into the pin for signals lower than 1.5V. In order to minimize this loading effect on dimming linearity and range, source impedance of the BRITE signal should be much lower than 50K. While op amp gain accuracy is excellent due to 1% matching of these two feedback resistors, their absolute values can vary up to +/- 30% including lot to lot process

variations and temperature coefficient of resistance. This needs to be considered in applications requiring extreme accuracy and repeatability of brightness control, and usually requires the BRITE input be driven with a low impedance op amp. In this design we use a simple 2K ohm RC low pass filter that gives performance suitable for a notebook computer display. This filter can convert a high frequency PWM signal to a DC voltage compatible with the BRITE pin, or pass a DC voltage directly from a potentiometer or DAC.

BRITE Pin DC Input Operating Voltage Range

The DC input operating voltage range for the BRITE pin is 0 to 3 volts if in analog dimming mode (DIG_DIM is low) and 0.5 to 2.5 volts if in digital dimming mode (DIG_DIM is high). The abbreviated digital dimming range insures the burst comparator can produce both 0% and 100% duty cycles by making the voltage ramp on its inverting input have top and bottom limits that can be over ridden by the BRITE input voltage of 0 to 3 volts. The top and bottom points of the ramp are set at 2.5 and 0.5V respectively by an internal 2% reference voltage to provide good accuracy and repeatability for the V_{BRITE} vs. lamp current transfer function. Dimming ratios of 100:1 are possible.

Pointers Using PWM Inputs For Brightness Control

Many microprocessors have PWM output channels available for controlling external analog functions. These channels may be programmed to output variable width pulses at various repetition rates. Since the LX1686 needs a DC control voltage at its bright input, it is necessary to change the PWM signal to DC with a low pass filter. In Figure 10, the BRITE filter has a time constant of 2K x 100nF = 200µs. This will not adequately filter a PWM input signal (If PWM frequency is less than 75 KHz). If using a PWMinput, increase the value of C9 to make its time constant with R15 atleast 20 times the period of the PWM pulses. For example, 100µFgenerates a 200ms time constant that will adequately filter 100Hzand above. If filtering is inadequate, ripple voltage on the BRITE pin will cause lamp current modulation at the PWM repetition rate, and ifripple frequency is lower than 90Hz, will appear as visible flicker.

Remember also, that DC voltage output from the filter is proportional to input duty cycle *and input voltage amplitude.* If BRITE signal amplitude is not constant, additional circuitry is needed to prevent its variations from changing the lamp current. A universal conditioning circuit is shown in Figure 13 that clamps any pulse amplitude above 2.5 volts while still passing a DC input without changing it. The circuit has 500K input impedance so it is more tolerant of high source impedance. Its large time constant integrator can filter PWM inputs as slow as 50Hz, but it uses low frequency op amps which limit maximum input frequency to 1 or 2KHz. High speed op amps can be substituted if higher PWM frequencies are desired.

The optional resistor divider, R16 and R17 (Figure 10) can be used to set a lower limit on BRITE voltage, even if the source voltage goes to ground. This can guarantee a minimum brightness level, and, in the case digital dimming is used, provide a hardware 'stop' that will keep the BRITE input far enough above the VCO valley voltage to prevent entering strike mode. This is discussed in more detail when we deal with the OLSNS input circuit.

Synchronizing The Digital Dimming Burst Rate

The LX1686 has a complete PLL on chip to permit an external signal to control burst rate. An AFD circuit (Auto Frequency Detect) automatically looks for a logic signal input on the FVERT pin. If one is detected, the PLL locks to it and generates an internal burst rate at exactly twice its frequency. Doubling burst frequency insures an ability to synchronize to low 50 and 60Hz frame rates while still having a burst rate above visual detection. Actually, the PLL can lock to any frequency between 40 and 200Hz. The polarity and duty cycle of FVERT may be anything as long as a minimum pulse width of 300ns is presented. Pulse polarity can even change on the fly without loosing phase lock. This is important in portable applications because the video sync signal can have different width and polarity in various programs. A classic case is during boot up on a notebook where DOS and Windows generate different V_{SYNC} polarity.

AFD Circuit Response Time

AFD circuit response time is controlled by C4. An internal current source alternately charges and discharges C4 with a square wave that is generated by dividing the signal at FVERT by two. If FVERT is present, the voltage at AFD_C will stabilize at VDD/2. If FVERT is static high or low, the voltage at AFD_C will stabilize at either VDD of VSS accordingly. Comparators sample this voltage to determine if a signal is present. Response time is a function of the current source amplitude set by R21 and the value of C4 as follows:

$$T_{D\text{-}AFD} = 50 \cdot R21 \cdot C4$$

$$C4 = \frac{T_{D-AFD}}{50 \cdot R21}$$

A 22nF X7R capacitor will result in about 0.48 second response, a good place to start.

Maximum VCO Frequency

Digital dimming burst frequency is the same as VCO frequency. Maximum VCO frequency (Fvco_max) must be designed for two times the maximum expected frequency on the FVERT pin, e.g., Fvco_max = 2 FVERTmax. If no signal is detected on FVERT, the VCO defaults to ½ its maximum design value.

This feature can be used to set nominal burst frequency when no synchronization input is used.

$$F_{VCO\_MAXI} = 2\,FVERT_{MAX} = \frac{1}{5 \cdot R21 \cdot C8}$$

For FVERT expected maximum equals 100Hz, F_{VCO_MAX} = 200Hz.

Then;

$$C8 = \frac{1}{5 \cdot R21 \cdot F_{VCO\_MAX}}$$

$$C8 = \frac{1}{5 \cdot 43.2K \cdot 200} = 23nF$$

The closest smaller standard value is 22nF, which gives actual maximum VCO frequency of 210Hz. If no input is placed on the FVERT pin, typical burst frequency is 210 / 2 = 105Hz. This is about as low as you should go to prevent visual detection of lamp current bursts. If you want to calculate C8 to provide a specific 'unsynchronized' burst frequency;

$$C8 = \frac{1}{5 \cdot R21 \cdot 2 \cdot F_{VCO\_TYPICAL}}$$

Assuming $F_{VCO\_TYPICAL}$ is 230Hz;

$$C8 = \frac{1}{5 \cdot 43.2K \cdot 2 \cdot 200} = 10nF$$

Compensating The Phase Detector

C6, C7, and R18 values determine phase detector pull-in time (time to lock to a new frequency) and damping factor. The phase detector amplifier is a Gm type and has a maximum output current, I_{PD} = 1 / 10 · R21. This current is in the range of 2µA, so low leakage ceramic capacitors must be used for C6 and C7 to prevent erratic operation. Pull-in time in the range of 0.1 to 1 second is usually acceptable. If too long, however, the lamp may flash on power up as the VCO changes from the initial default frequency to the lock frequency (remember, the VCO will default to F_{VCO_MAX} / 2 until PLL lock is achieved). The damping factor is usually set to 0.707 (critically damped).

Pull-in time:

$T_P = \frac{16 \cdot \pi}{W_N}$, where W_N is the natural PLL frequency.

$$W_N = \frac{1}{2 \cdot R21 \cdot \sqrt{10 \cdot C8 \cdot C6}}$$

$$T_P = 32 \cdot \pi \cdot R21 \cdot \sqrt{10 \cdot C8 \cdot C6}$$

$$C6 = \frac{T_P^{\,2}}{(32 \cdot \pi \cdot R21)^2 \cdot (10 \cdot C8)}$$

For Pull-in time of 0.7 seconds: C6 = 220nF

For Pull-in time of 0.5 seconds, C6 = 100nF

PLL Damping Factor

$D_F = \left(\frac{T_Z}{2}\right) \cdot W_N$, where T_Z is the PLL zero time constant,

$T_Z = R18 \cdot C6$

$$R18 = 4 \cdot D_F \cdot R21 \cdot \frac{\sqrt{10 \cdot C6 \cdot C8}}{C6}$$

For Damping factor = 0.707, C6 = 220nF, C8 = 10nF, and R21 = 43.2K,

R18 = 82K

High Frequency Attenuation Capacitor C7

This capacitor reduces high frequency gain of the loop.

$C7 = \frac{C6}{10}$ For C6 = 220nF, C7 = 22nF

If you are not using synchronized digital dimming do not install C4, C6, C7, and R18. Instead, connect pins 4 and 8 to analog ground.

Selecting U2, The Power FET

Drain to source voltage rating for U2 should be 3 to 4 times the maximum power supply voltage. In this push – pull topology, operating V_{DS} is twice V_{BAT} due to the dual primary winding on the high voltage transformer. Because these windings are impossible to perfectly match, especially with respect to leakage inductance, there will be an inductive spike at transistor turn off. Its amplitude is proportional the leakage inductance difference of the two winding halves. V_{GS} needs to be high enough to survive these spikes. Some design trade-offs are possible. V_{GS} can be increased to permit more imbalance in the transformer construction, or snubbers can be added on the transistor drains to suppress the transients. Snubbers generally dissipate power, and in doing so reduce efficiency. Another possibility is to select a FET having an adequate repetitive avalanche power rating to absorb transient energy without overheating. This will also reduce efficiency.

On state resistance of the FET should be less than 200 milli ohms for a typical 4 to 6 Watt load. It can be increased for lighter loads. Experience shows that reducing Rds_on below 100 milli ohms increases efficiency very little. For highest efficiency, it is better to select a FET with very low total gate charge. At 60 to 80KHz, gate losses can be larger than the I^2R losses of a 100 milli-ohm FET pair.

V_{GS} is an important selection parameter. The LX1686 drive voltage to the FET gates is equal to the VDDP supply. Select FET's that are fully enhanced at the minimum supply voltage. This design uses an on board generated VDDP that operates at 5.6V nominal to give the FET's a bit more drive.

AOUT And BOUT Connections

The 10K resistors (R10 and R12) to ground on these pins pull down the FET gates when input supply voltage is too low to guarantee the state of the LX1686 outputs. This typically occurs below 2.5V. If the supply is increased very slowly through the 1 to 2.5 volt levels, it is possible to inadvertently turn the FET's on at 100% duty. This could blow the input fuse or destroy the FET's. If slow power on cannot happen in your system, the 10K resistors may be omitted.

Thirty nine ohm resistors R9 and R11 are connected in series with the gates and work with FET input capacitance to slow down their transition time. This reduces high frequency emissions and helps control EMI. Care must be taken to *not* make R9 and 11 too high, as slowing transition time too much will cause the FET's to overheat. Power losses are highest during transitions since current and voltage are both high then. If you choose a different FET, re-optimize R9 and R11 values.

The High Current Power Stage

U2, T1 and C10 are the high current power stage components. Square wave switching currents pass through each of them. They must be designed for low resistance to minimize I^2R losses, and must be physically positioned close together with extremely short conductors to prevent ground noise from interfering with the BRITE input, and to minimize radiated and conducted emissions. Further PC layout should have separate power and signal ground paths. Analog signal ground should connect to power ground only at the negative end of C10.

C10 is a low ESR tantalum in this design. Always use D or E case parts because they have the lowest ESR. Ceramic capacitors in the 2 to 10µF range also work well but are more expensive.

Configuring The High Voltage Output

High voltage is delivered to the lamp through C14, a series DC Bypass capacitor. Use a $50V_{DC}$ or higher rated XR7 type capacitor. Maximum voltage appears across the capacitor when the output is shorted, because lamp current increases under short circuit conditions. The high voltage end of the lamp must be connected to this capacitor to maintain high efficiency. Actually the lamp itself is non-polarized, but when mounted in a panel, it takes on an important characteristic. One terminal will have a very short wire resulting in very low parasitic capacitance. The other's will be long, creating much higher parasitic capacitance. The concern is leakage currents flowing into this parasitic load, since they serve no good function, reduce efficiency, and complicate lamp current regulation. Since there is little voltage to flow parasitic current, the long wire is returned to the low voltage rectifier circuit.

The purpose of the ballast capacitor is to prevent any DC current in the lamp, as this drastically reduces its life, and to act as real impedance against the negative impedance of the lamp. Its value is chosen as high as possible to minimize voltage drop across it. Voltage across C14 is at a 90 degree phase shift with lamp voltage, so must be added vector wise to find total voltage required from the transformer. Note that with direct drive topology, it is not necessary to drop large voltages on the ballast capacitor, as is the case with Royer circuits.

One precaution: direct drive, as with all other known topologies, can experience a low frequency amplitude modulation of lamp current under certain conditions. This is caused by the negative resistance and extreme voltage dependency on temperature of the lamp operating in a current regulated closed loop. Check for modulation, usually in the 5 to 15KHz range while varying lamp current and power supply input voltage. Modulation can usually be eliminated by optimizing operating frequency.

High Voltage Feedback

Lamp voltage is divided across capacitors C16 and C17 and fed back to the LX1686 VSNS input through emitter follower Q5. R24 DC restores C17 to keep the waveform at Q5 base sinusoidal. Q5 acts as a rectifier and buffer, presenting a known fraction of peak lamp voltage to VSNS.

VSNS is the inverting input of the voltage error amplifier. Its characteristics are identical to, and its output is processed the same as the current error amplifier. Its non-inverting input is connected to a precision 1.25 volt DC reference. If the peak lamp voltage exceeds a preset limit by choosing the ratio of C16 and C17, AOUT and BOUT pulse widths will be reduced as needed to regulate peak lamp voltage.

Choose C16 in the range of 2 to 5pF, keeping it small to minimize leakage current and to keep unloaded resonant frequency below 300KHz so strike voltage is easily developed. Next choose C17 as a multiple of C16 so maximum peak voltage is equal to 1.25 volts plus Q5 V_{BE}. If more freedom from Q5 temperature variation is desired, add a 3.3K resistor in series with R23 and ground to form a voltage divider. Connect the resistor tap to VSNS. Now V_{PK} max will be 3.75V plus Q5 V_{BE}.

Microsemi has designed many inverters that use a PCB capacitor for C16. If space allows, this will save the relatively high cost of a low pico farad high voltage capacitor. Standard formulas for parallel plate capacitors apply, and we have found computer grade PCB materials to be a very acceptable dielectric. If you do this be sure to round all sharp corners and leave at least 3mm spacing between low and high voltage conductors to prevent arcing.

Short-Circuit Protection

Underwriters Laboratory requires maximum peak current, for even a single cycle, be limited to a specific value when any of the output terminals and ground are shorted with a 2K ohm resistor. This can be a problem when shorting either lamp terminal to ground because the current sensing mechanism in the control loop is shorted. Under this situation, the loop will put out maximum possible current, which will always exceed UL's requirements. Q4 and R22 are added to this design to meet UL requirements for a "limited current device". R22 is selected so the voltage across it will regulate maximum short circuit current through Q4 and into the VSNS circuit, just like high voltage is regulated.

Since R22 is on the inside leg of the transformer, a short at the connector will not disable its function. Set R22 empirically since total current in it consists of both parasitic currents and actual lamp currents. Parasitic currents should be measured on the actual LCD panel with a production level inverter installed.

Open Lamp Sensing

The open lamp sense circuit is a peak detector that monitors lamp current. When lamp current flows, the positive half cycles will charge C18 through R25. During negative half cycles C18 slowly discharges through R25 and R26. By keeping the ratio of R26 to R25 very high, a highly filtered peak voltage is presented to the OLSNS input pin. OLSNS is the input to a voltage comparator with positive threshold of 300mV and negative (low going) threshold of 260mV. When OLSN is < 260mV the lamp is considered not ignited since little or no current is

flowing through it. Component values are set up so a very small number of lamp current cycles (typically 6 or 8) will raise OLSNS above the 300mV level to indicate the lamp is ignited.

Setting proper component values gets tricky for digital dimming operation if very low brightness levels are expected. A fine line exists between the lamp being considered 'on and dim' rather than 'off'. The problem is that when the lamp is considered off, the LX1686 enters strike mode where it actually operates at a 10Hz, 50% duty cycle causing the lamp to flash at that rate! Preventing this undesirable situation requires the designer to carefully consider the worst case capability of the OLSNS detector compared to the minimum brightness setting. In other words, if the detector can reliably detect the presence of only 8 current cycles, don't allow the BRITE input voltage to request less than eight.

Reducing the value of R25 or C18 decreases delay time to detect OLSNS going high and will lower the number of detectable current cycles. Increasing the C18 / R26 discharge time constant permits the inverter to operate at a slower dimming burst rate.

Lamp Current Regulation Loop

Lamp current is rectified by the diodes in D2 (pin 1) and D3 (pin 2). D2 pin 2 is part of the OLSNS peak detector, and D3 pin 1 is a voltage clamp that prevents the common mode input range of the current error amplifier from being exceeded. The R/C network R28/C20 converts lamp current to a filtered DC voltage that is passed to the error amplifier at the ISNS pin. The filter time constant should be just large enough to prevent feedback voltage peaks from exceeding error amplifier input common mode voltage. R27 (Optional) on the outside of the rectifiers shunts some of the lamp current from the error amplifier and is selected to keep lamp light output constant over the input voltage range. C19 provides a low impedance ground path to parasitic RF currents during open circuit or strike conditions.

To adjust rms lamp current amplitude, adjust the values of R27 and R28. Increasing resistance decreases rms current. Typically the values of R27 and R28 can be equal with the following exceptions:

1) If inverter input voltage is fixed within ±5%, R27 may be omitted;

2) If input voltage varies widely, then R27 / R28 can be varied to achieve constant light output. Decreasing R28 while increasing R27 increases lamp current at high line.

Compensating The Error Amplifiers

Both error amps are unconditionally stable without external capacitors at their outputs. Compensation capacitors on these transconductance amplifier outputs are selected specifically to control the respective loop time constants.

The ideal current error amplifier compensation depends on whether using digital or analog dimming. With analog dimming, loop response can be quite slow, but for digital dimming it must be fast so lamp current gets to full amplitude with in 2 or 3 current cycles. If response is slower than this, light output at low brightness settings will not be satisfactory, exhibiting uneven light along the length of the tube. Uncompensated error amp response will allow overshoot on even the first current cycle after the BRITE input goes high. Enough compensation should be used to limit overshoot to the lamps maximum rated rms current.

The only other consideration for selecting C12 is to aid in controlling lamp current modulation as described in the section titled 'Configuring the high voltage output'.

Minimum Error amp bandwidth:

$$BW_{EA\_MIN} = \frac{48}{C12} \qquad \text{BW in Hz, C12 in } \mu F$$

Voltage error amplifier compensation should also be fast so that open circuit output voltage overshoot is controlled. The objects of this compensation is to slowly increase output voltage in the case of a cold turn-on and after each strike attempt while in strike mode. The compensation capacitor C13 is discharged to zero after each power down and between strike attempts.

Soft start time:

$$T_{SS} = 0.45 \cdot C13 \qquad T_{SS} \text{ in seconds, C13 in } \mu F$$

Lowest Cost Configuration

Figure 11 shows a similar inverter as described above (ref: Figure 10) designed for lowest cost. The transformer style has changed from a 6W topology to a 4W with a corresponding decrease in output voltage from nominally $650V_{RMS}$ to $550V_{RMS}$. The difference is in support circuitry. By using the system 5V supply and simplifying the digital dimming interface, a total of 27 components can be removed from the design of Figure 10.

The digital dimming feature is maintained, but is not synchronized by the LX1686. It is possible to synchronize the PWM brightness control signal on the system board, but many users do not require this be done. By examining Figure 11 and Figure 3, the LX1686 block diagram, it can be seen that the BRT_POS input is used to dynamically switch the burst comparators non-inverting input between VDD and ground. Since BRITE is connected to VDD, its compliment will be zero volts. Both of these levels exceed VCO_C ramps peak and valley voltages, so the comparators output follows its non-inverting input. As a result, the non-inverting input to the current error amplifier (pin BRT) sees the same 2.5V PWM signal that it would in the synchronized digital dimming mode illustrated in Figure 10.

Because the LX1686 operates on 5V, there is no need for the on-board voltage regulator. Removing the zero power sleep switch increases sleep current to 200µA plus current in R13, but this would not be a problem if the 5V system supply were switched off in sleep mode, a standard feature in note book computers.

This design assumes the ENABLE input and PWM input to BRT_POS are generated from 5 volt logic so their 'one' logic levels are compatible with the LX1686 input threshold voltages. If they are generated with 3.3 volt logic, it will be necessary to add the two resistor bias networks described for the FVERT pin in Figure 10.

Pull down resistors on the FET gates are omitted because the +5V supply will have a controlled rise and fall time. The 39 ohm EMI reduction resistors are removed, but C1, the EMI reduction capacitor is left in. The fuse has been omitted since an adequate fuse is assumed on the +5V supply.

This same circuit configuration may be used with a 3.3 volt supply. Replace U2 with V_{GS} = 2.7V FET, and change the tantalum filter capacitor to 220µF, 10V. You also need to make sure that lamp feed back peak voltages to ISNS and VSNS do not exceed 3.3 volts since this would prevent proper current and voltage regulation. Finally, the transformer turns ratio needs to be adjusted for the reduced input voltage.

Low Power Configuration

In Figure 12 find an example of a 1W single lamp inverter that is designed to work from a single cell Li-ion battery. In this configuration a +5V logic input of 10mA continuous is required to power the control IC. Since a 5V logic level supply is used the peak ISNS and VSNS feedback voltages allowed is greater then described above in a 3.3V only design.

This schematic is also an example of an analog only non burst mode inverter. The BRITE input can either be a DC voltage between 0 and 2.5V with 2.5V being full brightness, or a 2.5V logic level PWM signal greater than or equal to 50KHz. This particular design uses a lower profile FET and magnetics and is optimized for 290V ±15% lamps running at 3mA output current.

BRITE Input Signal Conditioning

Figure 13 shows a dual op-amp circuit that can be used as signal conditioning for the brightness control signal. It will condition a PWM logic input or a DC voltage as designed. Two functions are performed: First, any voltage exceeding 2V will be ignored, and second, a zero to 2+ volt input signal will be shifted up to guarantee the inverter will be at a well defined 'minimum brightness' with a zero volt input. This later feature also insures the inverter will not enter strike mode as a result of a low brightness input voltage. Minimum voltage at the LX1686 BRITE input (Pin 11) should be 0.73V. Maximum should be at least 2.58V.

Both amplifiers have voltage gain of minus one so there is no net gain or inversion through the circuit. The first amplifiers' purpose is to clamp any input signal above 2 volts so amplitude variation does not change lamp brightness. Refer to 'Pointers on using PWM inputs for brightness control' above. Since the LM324 output goes very near ground, output voltage will be essentially zero with two volts input. Further increases in input voltage cannot drive the output more negative, therefor the input is effectively clamped at plus two volts.

Setting the non-inverting input voltage of this amplifier determines the maximum unclamped input voltage. If a wider dynamic input range is wanted, increase voltage on the non-inverting input. Dynamic input range is 2 times non-inverting input voltage.

The second amplifier has an integrating capacitor across the feedback resistor, so it filters 50Hz PWM input pulses sufficiently to convert them to a DC level. This is needed by the BRITE input. The voltage on this amplifiers non-inverting input offsets the input signal in a positive direction to prevent BRITE voltage from going below the minimum for 2% duty cycle on lamp current. A 0.73V offset is needed, so 1.37V is placed on the non-inverting input. When the first amplifier output is at 2.0 volts, corresponding to BRITE INPUT = 0V, BRITE OUTPUT will be at 0.74V. Similarly, a zero volt output from the first stage gives 2.74 volts at the BRITE OUTPUT which guarantees 100% duty cycle (maximum brightness) can be achieved.

The low bandwidth LM324 limits maximum input repetition rate to about 1KHz. If higher input frequencies are used, replace it with a higher performance part.

A Broken Lamp Shut Down Circuit

Some applications such as automotive displays, require the inverter to shut off for personal safety reasons if the lamp fails to strike in a reasonable time. The circuit of Figure 14 will accomplish this. It utilizes the fact that signal TRI_C is always above 0.7 volts when the lamp is in strike mode, and at zero volts when the lamp is ignited. This signal enables the first comparator output to go high if the lamp is not ignited, allowing the 330K resistor to charge the 10µF capacitor. After about 3 seconds, the 3.5V threshold of comparator two is reached, driving its output low. This pulls down the VCOMP pin on the LX1686, forcing output pulses at AOUT and BOUT to turn off. The capacitor is reset by bringing ENABLE or the 5V supply low.

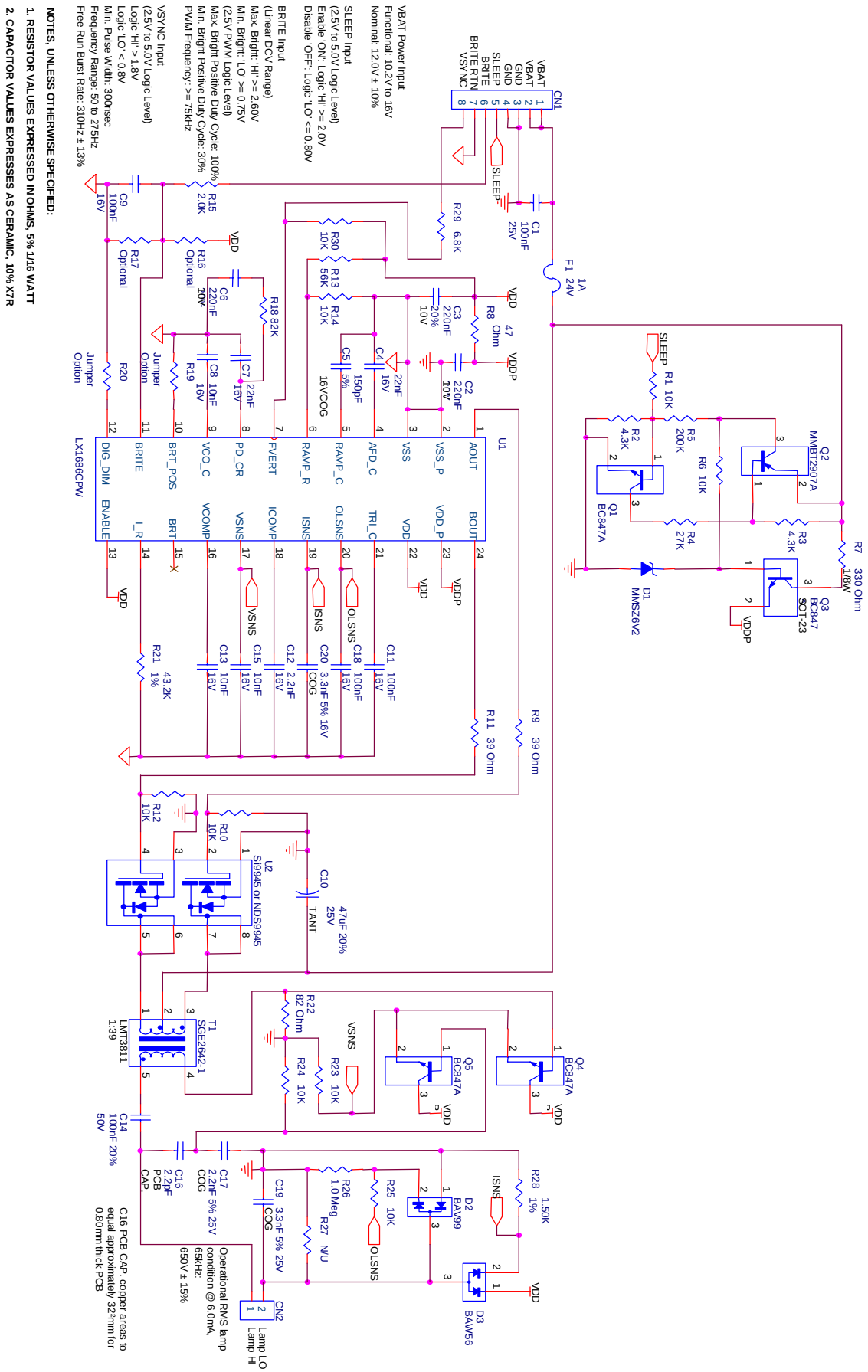


Figure 10: Standard LXM1612-12 Digital Single Lamp Inverter

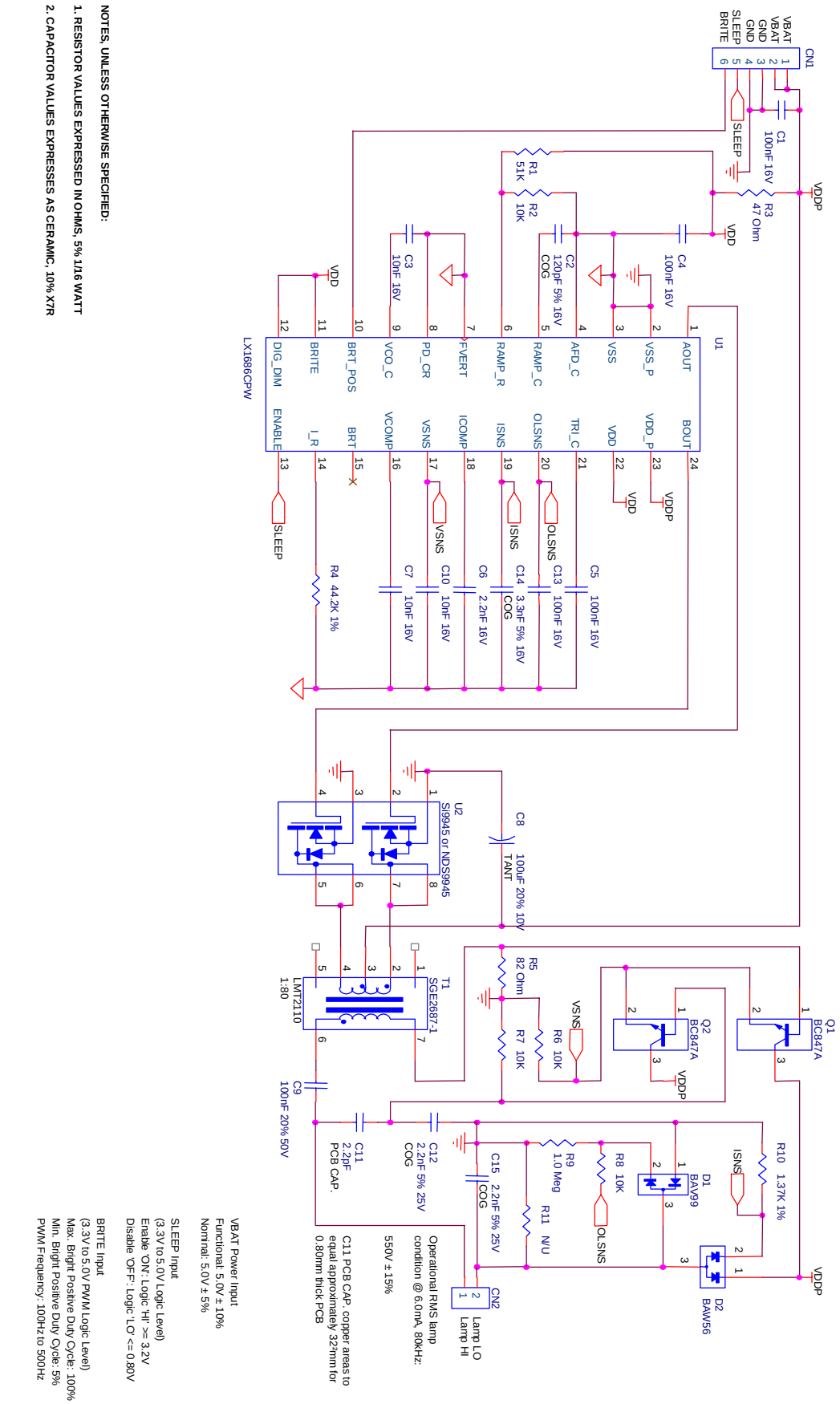


Figure 11: Low Cost Direct PWM Input, Single Lamp Inverter

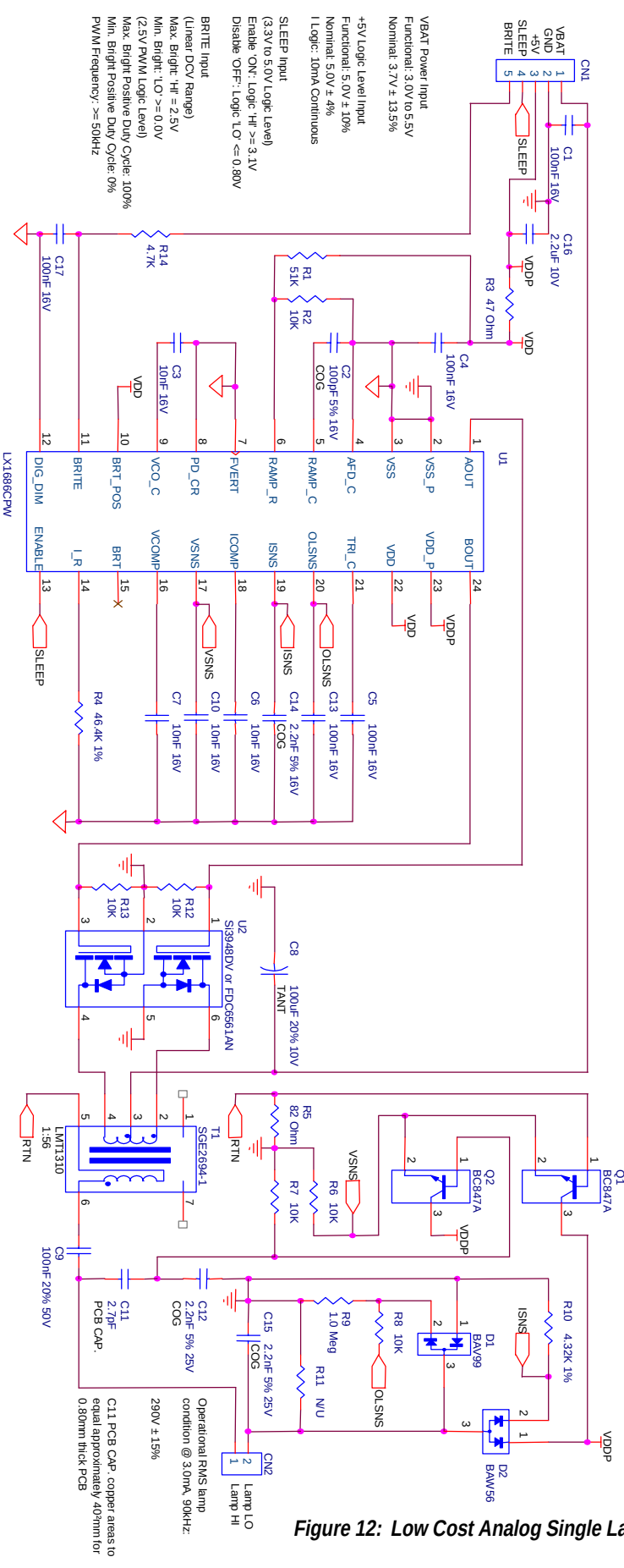


Figure 12: Low Cost Analog Single Lamp Inverter

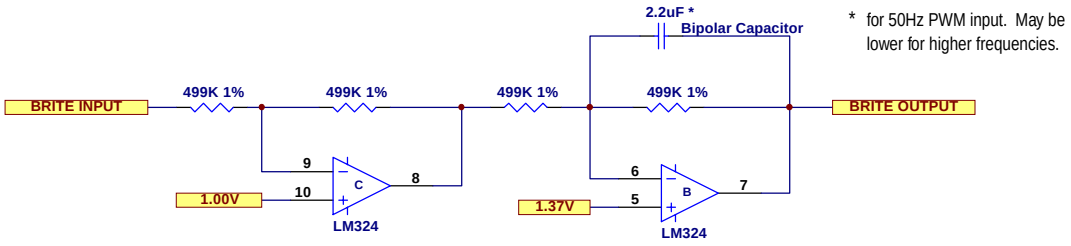


Figure 13: Brite Input Conditioning Circuit

Clamps and filters PWM BRITE inputs making lamp brightness insensitive to input pulse amplitude, and shifts 0 to 2V DC inputs to match LX1686 levels.

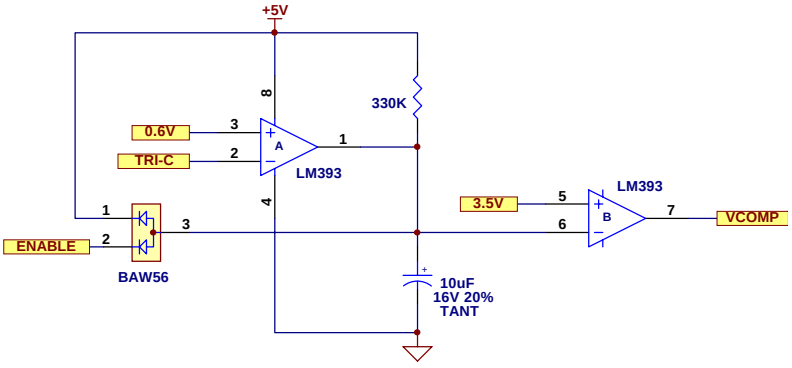


Figure 14: Open Circuit Time Out

Shuts off inverter after attempting to strike the lamp for more than 3 seconds.

6.0 TRANSFORMER DESIGN and SELECTION CRITERIA

Bifilar-Wound Primary

The transformer must have a bifilar-wound primary so that the leakage inductance of each half of the primary is approximately equal. Leakage inductance of the two halves must be within 5%. The purpose is to balance the energy released each time the FET switch is opened. If the leakages are equal, the smallest possible voltage spike is imposed upon the FET switch. When unequal, the voltage spikes are higher causing high-voltage stress from drain to source of the FETs.

Leakage Inductance

The leakage inductance must also be sufficient to limit the inrush-peak current that the FET must withstand. Loosely coupled designs offer the best option for this required characteristic. Designs which have closely coupled primary and secondary typically have very low leakage inductance. Typically, the leakage should be sufficient to limit the slew rate of the switching current such that the maximum required primary current is reached in 1/4 of the total switching period. Most sector-wound high voltage transformers in this power class have sufficient leakage inductance to limit the peak current to acceptable levels. Excessive leakage will limit the output current ability of the transformer, but is seldom encountered in practice.

Open Circuit Series Resonance

During lamp strike mode operation of the LX1686 controller, the switching frequency is swept from its “base” operating frequency to a maximum of about three times this base frequency. For example, if the base operating frequency is set to 60kHz, during lamp strike mode the switching frequency will sweep from 60 to 180kHz. The transformer must exhibit additional “gain” at the higher frequencies so it will supply a high enough output voltage to strike the lamp. It is best to program the controller’s swept range to match the transformer’s characteristic when installed on the inverter. This enables the strike voltage to be available for the maximum duration.

Open circuit (lamp not ignited) resonance of the transformer must be within the frequency range of the sweep. The series resonant circuit is composed of the leakage inductance, the secondary winding capacitance, and load capacitance. Since the reactances cancel at resonant frequency, maximum current is obtained. This maximum current produces the maximum voltage across the load.

Load capacitance includes a capacitive voltage divider used in the over-voltage protection scheme that typically adds 2-5pF. The lamp high-lead capacitance-to-ground also adds 1-3pF. Ensure that these capacitances are taken into account when evaluating a design.

Sufficient "Q" at Resonance

The strike voltage developed at resonance must be sufficient to ensure lamp ignition. Typically, strike voltage is about twice (2X) the run voltage at low temperature. It generally increases as the CCFL ages. "Q" of the resonant circuit must be high enough that the required "magnification factor" is achieved. The higher the L/C ratio, the higher the "Q". Thus, minimizing the lumped secondary capacitance maximizes Q and strike voltage. All standard information regarding resonant circuit behavior and simplified transformer equivalent circuits is directly applicable to this topology. Most sector-wound high voltage transformers we have evaluated have series resonances in the range of 90 - 200kHz when installed on the inverter. Please refer to transformer design discussion and equations.

Transformer Turns Ratio

Calculation of the required turns ratio involves the estimation of two critical factors:

1. The minimum input voltage available to the primary winding and,

2. The maximum output voltage required from the secondary winding.

Estimating Minimum Primary Voltage

The minimum input voltage is obtained from the value of the lowest supply voltage, the maximum resistive voltage drop of the wiring from the supply to the inverter and the maximum voltage loss on the inverter from the input connector to the primary. The primary winding resistance itself must also be considered.

Example:

for V_{IN} 15V with Tolerance ±5%:

$V_{MIN} = V_{IN} \cdot 0.95 = 14.25V$

Wiring Voltage Drop:

for #22 AWG wire, resistance at 20°C is 0.0162 Ohms per foot. Two wires (+V_{IN} & Power Ground) of 18 inch Length are used for a total length of 36 inches or 3 feet. At 20°C

R_{WIRE} = Length · Resistance = 0.049 Ohms

In order to estimate the current flowing through the wiring, you must know the required output power of the inverter and its efficiency. Assume a worst-case efficiency of 75% & an output power of 4 Watts.

$$P_{IN} = \left(\frac{1}{Eff}\right) \cdot P_{OUT} = 5.333\ W$$

$$I_{IN} = \frac{P_{IN}}{V_{IN}} = 0.374\ A$$

$V_{WIREDROP} = I_{IN} \cdot R_{WIRE} = 0.018V$

Next, we must estimate the voltage loss on the inverter itself. The losses here are the resistance of the copper traces, the "$R_{DS\ ON}$" of the FET switch and the resistance of the primary winding of the transformer. The copper trace resistance is small enough to be neglected. The "$R_{DS\ ON}$" of the FET can be estimated from its datasheet; it is a function of the gate drive voltage. The resistance of the primary winding will not be known at this point but a rough estimate will suffice. It must be remembered that the primary is a center-tapped configuration and therefore each switching cycle "sees" 1/2 the total primary resistance.

for $R_{DS\ ON}$ = 0.075 Ohms & $R_{PRI\ EST}$ = 0.500 Ohms:

$R_{PRI\ HALF} = 0.5\ Ohms \cdot R_{PRI\ EST} = 0.25\ Ohms$

$R_{TOTAL} = R_{DS\ ON} + R_{PRI\ HALF} = 0.325\ Ohms$

$V_{FET\ XF\ DROP} = I_{IN} \cdot R_{TOTAL} = 0.122V$

$V_{PRIMARY} = V_{MIN} - V_{WIRE\ DROP} - V_{FET\ XF\ DROP} = 14.11V$

This value of $V_{PRIMARY}$ is the peak voltage of the PWM square wave that will be applied alternately to each half of the primary. It is not an exact known value, but rather an estimate with which to predict the required turns ratio of the first pass design. Now the maximum required voltage of the secondary must be estimated.

Estimating Maximum Secondary Running Voltage*

The output section is composed of a ballast capacitor, a voltage divider capacitance (used for open circuit protection), the parasitic lamp high-lead capacitance to ground, the lamp itself and the parasitic capacitance of the ignited lamp to ground.

The ballast capacitance used in this topology is generally 220pF. The voltage divider capacitance is generally 4pF. Lamp wiring capacitance to ground of the high lead is typically 2-3pF for high quality voltage wire of short length (measure it if in question). The ignited lamp has a capacitance to ground that may be determined empirically by measuring the panel ground return current and the lamp's operating voltage simultaneously. Knowing the operating frequency of the drive voltage you can calculate the capacitive resistance value of this parasitic and then "back-calculate" for the capacitance. Most quality 14 inch (diagonal) displays we have seen are close to 20pF. Make the measurement if the data is not available from the panel supplier.

$C_{BAL} = 220 \cdot 10^{-12}$ $C_{DIV} = 4 \cdot 10^{-12}$ $C_{WIRING} = 3 \cdot 10^{-12}$ $C_{LAMP} = 20 \cdot 10^{-12}$
(all values in Farads)

The operating frequency of the inverter must now be known to complete the estimate. Most CCFL inverters are designed to operate in the range of 50 to 100kHz. For this example, 65kHz will be used. The ballast capacitor is connected to the output high terminal (series) with the remaining capacitors appearing in parallel with the lamp. Thus, the voltage developed across the ballast capacitor is a function of the lamp and the capacitor (divider, wiring and lamp) currents at the operating frequency. The lamp voltage appears across these three capacitances; this enables us to easily calculate the magnitude of this "parasitic" current.

$C_{EQ} = C_{DIV} + C_{WIRING} + C_{LAMP} = 27pF$ with f = 65KHz

$$X_{CEQ} = \frac{1}{(2 \cdot \pi \cdot f \cdot C_{EQ})} = 90k\Omega$$

Now the lamp operating voltage must be known. Lamp voltage increases over time. For example, a lamp listed as 550 V typical at 7.5 mA might have an initial production tolerance of ±10% which would translate to an initial maximum of 605V .

At "end-of-life" for a given number of hours, this might be as high as 760 V (example only!). For our example, we will use a lamp voltage of 850 V. The current that will flow through the lumped capacitance that is across the lamp would be:

$$I_{CEQ} = \frac{V_{LAMPMAX}}{X_{CEQ}} = 0.009\ A$$

If the lamp is to be driven at 7.5 mA and is considered to be mainly resistive in nature, we may now add (in quadrature due to the 90° phase relationship) the capacitive current for this to arrive at the total magnitude of the current flowing through the ballast capacitor which must be supplied by the transformer secondary.

$$I_{TOTAL} = \sqrt{I_{LAMP}{}^2 + I_{CEQ}{}^2} = 0.012\ A$$

Since we know the operating frequency, the ballast capacitance and the magnitude of the current through this capacitance, we can now determine the magnitude of the voltage across the ballast.

$$X_{CBAL} = \frac{1}{(2 \cdot \pi \cdot f \cdot C_{BAL})} = 1.113 \cdot 10^4$$

$$V_{CBAL} = I_{TOTAL} \cdot X_{CBAL} = 133\,V$$

The last item to be addressed is the voltage drop of the secondary resistance when delivering the required current. Most CCFL inverter output transformers in the 3 to 8 Watt power range have secondary winding resistances in the range of 300 to 800 Ohms. We will assume 500 Ohms here.

$$V_{SEC\ DROP} = R_{SEC} \cdot I_{TOTAL} = 6\ V$$

Added to the lamp voltage (linearly as the two are considered "in phase") gives total resistive component which can be added in quadrature (assumed 90° out of phase with capacitive voltage) to the ballast capacitor's voltage to give the total required output voltage. Knowing this, we can estimate the required turns ratio of the transformer.

$$V_{TOTAL} = \sqrt{(V_{LAMPMAX} + V_{SECDROP})^2 + V_{CBAL}{}^2}$$

$$V_{PRIMARY} = 14.11 \qquad V_{SECONDARY} = V_{TOTAL} = 866\ V$$

Turns Ratio

$$\text{Turns Ratio: } N = \frac{V_{SECONDARY}}{V_{PRIMARY}} = 61.37$$

The primary voltage used in these calculations was applied to 1/2 of the primary. Therefore, the ratio of TOTAL primary turns to TOTAL secondary turns is 1/2 the "N" above. The primary to secondary turns ratio is therefore:

$$N_{PRI\ SEC} = 0.5N = 30.68$$

Required Number of Secondary Turns

At this point in the design process, you should have some idea of the core geometry and size required for your application. From the core constants provided by the core manufacturer, you will need the "Ae" or effective core cross sectional area. Knowing the voltage to be supplied by the secondary and assuming it will be closer to a sine wave than a triangular wave, we can estimate the peak flux density required to support this voltage. We will use a core with an effective cross-sectional area of 0.092 square centimeters for this example.

For most applications involving a relatively aggressive (i.e. small) size, the flux density is in the neighborhood of 2000 Gauss (B_{PK}= 2000). Utilizing the common expression for peak flux density generated by a sinusoidal voltage impressed upon a coil of "N" turns around a core of "Ae" cross-section, the required number of turns to meet this flux density "limit" would be:

$$N_{SEC} = \frac{V_{SECONDARY} \cdot 10^8}{B_{PK} \cdot 4.44 \cdot f \cdot Ae} = 1631$$

Required Number of Primary Turns

Now that the turns ratio and number of secondary turns have been estimated, simply divide the number of secondary turns by the turns ratio to arrive at the number of primary turns. Since the primary is to be center-tapped for the push-pull topology, we will need to round down to the nearest even integer number of turns. If you choose, you can round up, since there may be enough margin in the estimates performed thus far to support the subsequent required maximum secondary voltage. Another choice is to alter the secondary turns count based upon the rounded number of primary turns.

$$N_{SEC} = 1631 \qquad N_{PRI\ SEC} = 30.68$$

$$N_{PRI} = \frac{N_{SEC}}{N_{PRISEC}} = 53.2$$

Depending on your choice of rounding, the primary could be 52 or 54 turns using the data supplied for this example. If you chose 5 then you could subsequently recalculate the secondary based upon this primary turns count:

$$N_{SEC\ 52TPRI} = 52 \cdot N_{PRI\ SEC} = 1.591 \cdot 10^3$$

and for 54 turns:

$$N_{SEC\ 54TPRI} = 54 \cdot N_{PRI\ SEC} = 1.652 \cdot 10^3$$

Determination of Primary Wire Gauge

Based upon your particular bobbin (coil-former) selection, you will have a maximum winding width and height for the bobbin used. It is important to remember that the winding must be such that an even number of layers must be wound to bring the center-tap back to the

primary terminations (pins). All bobbins we have worked with for CCFL transformer construction have the primary terminations on one end of the bobbin. This means that the total number of layers must be in multiples of 2 to meet the termination requirements.

This restriction limits the number of choices in terms of wire gauge selection and primary winding volume utilization. For instance: If the primary sector height is 0.040 inches and the design requires 4 layer construction, then the maximum layer height would be 0.010 inches. Referring to a standard wire chart of sizes and choosing "single" insulation build magnet-wire, #31 AWG (max. diameter of 0.010 inches) would just fit. In reality, you would probably want to go up one gauge (down one size) to #32 AWG (max. dia. of 0.0091) to account for the bowing out of the wire as it is wound around the bobbin.

Working with the available width of the primary sector, you must determine if the required number of turns will fit distributed among 4 layers (or however many layers are required). If the sector width is 0.125 inches, for example, then the maximum number of turns per layer is the width divided by the wire diameter. In practice, it will be somewhat less as some space will inevitably be wasted due to winding technique or slight bends in the wire itself. This is generally referred to as a "space factor" and might reduce the available width use by 10% (i.e. a 90% space factor). Also, on the first and third layer, the entry of the wires into the bobbin will reduce the theoretical turns count by 1 turn on each of those layers. This is accounted for in the calculation of primary turns based on size, below.

Example:

$H_{SECTOR} = 0.040$ Layers = 4

$$H_{LAYER} = \frac{H_{SECTOR}}{Layers} = 0.01$$

$W_{SECTOR} = 0.125$ Choose wire size: $Dia_{AWG32} = 0.0091$

Turns per layer: $$TPL = \frac{W_{SECTOR}}{Dia_{AWG32}} = 13.736$$

$Turns_{PRI} = ((Layers - 2) \cdot TPL) + (2 \cdot (TPL - 1)) = 52.945$

Apply your desired "space factor" (SF): SF = 0.90

$Turns_{CORRECTED} = Turns_{PRI} \cdot SF = 47.651$

It is obvious that the desired 52 or 54 turn winding would not fit. Thus, the recommendation would be to go up a wire gauge (drop a wire size). AWG#33 single insulation build has a maximum diameter of 0.081 inches. Let's check if it fits:

$Dia_{AWG33} = 0.0081$ $$TPL = \frac{W_{SECTOR}}{Dia_{AWG33}} = 15.432$$

$Turns_{PRI} = ((Layers - 2) \cdot TPL) + (2 \cdot (TPL - 1)) = 59.728$

Apply your desired "space factor" (SF): SF = 0.90

$Turns_{CORRECTED} = Turns_{PRI} \cdot SF = 53.75$

The choice of primary turns is now best made in favor of the 52 turn center-tapped winding wound in four layers of AWG#33 single insulation build. As calculated earlier, this puts the required number of secondary turns at 1591. This will result in a slightly higher flux density than the example outlined. This should be of little consequence, but it is up to the designer to evaluate all the trade-offs made in the design process.

The final step in this procedure is to determine the secondary winding constraints and apply these limits to the selection of wire gauge. The differences in method are subtle. The secondary will most likely be "random" wound as, even with traversing wire-guides, the secondary windings will "wander" a bit. The copper loss of the secondary is usually small so the selection of wire gauge depends on the limits of the transformer manufacturer's capabilities.

Number of secondary sectors: $Sectors_{SEC}$

Width of each sector: $W_{SEC\ SECT} = 0.08$

$W_{TOTAL} = W_{SEC\ SECT} \cdot Sectors_{SEC} = 0.4$

Choose a wire gauge; this can be done by an acceptable current density or by choosing what will fit in the space allotted. You will still have to evaluate the implications of your selection electronically and mechanically. Current density limits vary so widely that we suggest you use what you are comfortable with based upon your own design experience. Consider, though, that the heat path from the inside of the winding to the outside is generally short in CCFL inverter transformers. This enables operation at higher current densities.

Assumed Current Density Limitation: 500 circular mils per Ampere

$CD_{LIM} = 500$ $I_{TOTAL} = 0.012$

Pick a wire-gauge that would fit your limit (i.e. AWG#43, 5.84 circular mils or $CM_{AWG43} = 5.84$)

$$CD_{ACTUAL} = \frac{CM_{AWG43}}{I_{TOTAL}} = 486.6\,cm/A$$

This is a higher current density than the limit set because there is less cross-sectional area of copper available for each Ampere of current flowing. Now determine if this gauge will fit in the space allotted:

$Dia_{AWG43T} = 0.0031$ $$TPL = \frac{W_{TOTAL}}{Dia_{AWG43T}} = 129.032$$

$$Layers = \frac{N_{SEC52TPRI}}{TPL} = 12.326$$

$Build = Layers \cdot Dia_{AWG43T} = 0.038$

Assuming the secondary sectors are of the same height as the primary (0.040 inches), the build just calculated (0.038) will probably not fit when the "space factor" is accounted for. The recommendation would be to go up a wire gauge (down in size) to AWG#44.

$$Dia_{AWG43T} = 0.0029 \qquad TPL = \frac{W_{TOTAL}}{Dia_{AWG44T}} = 137.931$$

$$Layers = \frac{N_{SEC52TPRI}}{TPL} = 11.531$$

$$Build = Layers \cdot Dia_{AWG43T} = 0.036$$

$$Build_{90\%SF} = 1.1 \cdot Build = 0.039$$

It appears this will fit.

Conclusion of Winding Analysis

The intent of all of the above was to arrive at a "first-pass" design for a given amount of winding space. The turns ratio and total number of secondary turns are such that a maximum flux density will not be exceeded when the transformer is required to supply the maximum output voltage set by the operating conditions of the inverter. The assumptions made are to be varied by the designer as are the acceptable limits of flux density, current density and space factor of the windings. Insulation build of the wire sizes chosen are a matter of acceptable voltage stresses and winding capacitance.