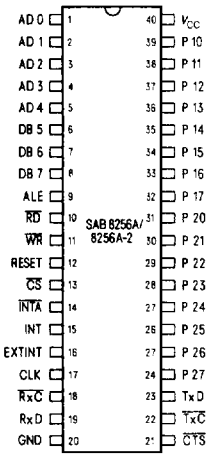
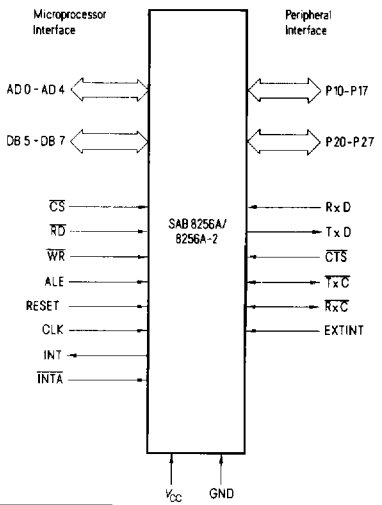
SAB 8256A, SAB 8256A-2 Programmable Multifunction UART (MUART)

- SAB 8256A is compatible with processors up to 3 MHz system clock (e. g. SAB 8085A, SAB 8048, SAB 8051).
  SAB 8256A-2 is compatible with processors up to 8 MHz system clock (e.g. SAB 8085A-2, SAB 8086 - minimum mode, SAB 80186).
- Full-duplex asynchronous serial interface with programmable 5–8 data bits, 0.75–2 stop bits, parity generation and checking.
- Internal baud rate generator programmable for 50–19, 200 Baud; 0–1 Megabaud possible with external baud rate clock.
- Interrupt controller with 8 priority levels; each level independently maskable, programmable for normal and fully nested operation with SAB 8085 and SAB 8086 processor families.
- Five programmable 8-bit counter/timers, internal or external clock, four are cascadable to two 16-bit counter/timers.
- Two 8-bit I/O ports, bit programmable for input/output, handshake mode supported.
- 40-pin dual-in-line plastic package (P-DIP-40)

Pin Configuration
P-DIP-40



Logic Symbol



SAB 8256A integrates four of the most often used peripheral functions in a microcomputer system into a 40-pin dual-in-line plastic package (P-DIP-40): serial interface, parallel interface, timer/counter and interrupt controller. It is primarily suited for systems like SAB 8048, SAB 8051, SAB 8085, SAB 8086, SAB 8088, SAB 80186 and SAB 80188 which have a multiplexed bus. With some additional circuitry, the SAB 8256A can also be used with other processors. All the functions of SAB 8256A are programmable by software, leading to a great flexibility in system design.

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Pin Description and Functions

Symbol	Pin	Input (I) Output (O)	Functions
AD0–AD4, DB5–DB7	1–5 6–8	I/O	**Interface to Multiplexed Address/Data Bus** Bidirectional lines to 8 data bits and 5 least significant address bits which are latched internally on the falling edge of ALE.
ALE	9	I	**Adress Latch Enable** The five least significant address bits and $\overline{CS}$ are latched on the falling edge of ALE into an internal register.
$\overline{RD}$	10	I	**Read Control** The microprocessor reads data from the chip when this signal is low.
$\overline{WR}$	11	I	**Write Control** The microprocessor writes data into the chip with a low on this pin.
RESET	12	I	**Reset** A high on this pin forces the chip to its initial state. The chip remains in this state until control information is written into the chip.
$\overline{CS}$	13	I	**Chip Select** A low on this pin during ALE enables the bus interface of the chip. Neither read nor write operations are possible without this enable. The signal has no effect on the internal operation of the chip.
$\overline{INTA}$	14	I	**Interrupt Acknowledge** When this signal is low, the microprocessor informs the chip that an interrupt request is being serviced.
INT	15	O	**Interrupt Request** The chip demands interrupt service from the microprocessor with a high on this output.
EXTINT	16	I	**External Interrupt** An external source can request interrupt service through this input. The source can be either a peripheral or another SAB 8256A with its INT pin as the signal source. The input is level sensitive (high). The request must be held high until the processor acknowledges it.
CLK	17	I	**System Clock** Clock on this input is the reference clock for the timers, baud rate generator and various other functions.

Symbol	Pin	Input (I) Output (O)	Functions
$\overline{R \times C}$	18	I/O	**Receive Clock** If this pin is programmed as an output, it provides a low-to-high transition at the sampling point of each received data bit (excluding the framing bits). When programmed as an input, an externally generated receive clock must be connected to this pin. At DC, its frequency can range up to 1.024 MHz matching the receiver baud rate. The internal baud rate generator is disabled if this pin is used as input.
R×D	19	I	**Receive Data** Input for serial data, which is converted to parallel format while discarding the framing bits and then is made available for the processor.
$\overline{CTS}$	21	I	**Clear to Send** This input enables the serial transmitter. If 1, 1.5 or 2 stop bits are selected, $\overline{CTS}$ is level sensitive. As long as $\overline{CTS}$ is low, any character loaded into the transmitter buffer register will be transmitted serially. For continuous transmission, this input must be tied to low. A single negative going pulse causes the transmission of a single character previously loaded into the transmitter buffer register. If the transmitter buffer is empty, this pulse will be ignored. If this pulse occurs during the transmission of a character up to the time where 0.5 of the first (or the only) stop bit is sent out, it will be ignored. If it occurs afterwards, but before the end of the stop bits the next character will be transmitted immediately following the current one. If $\overline{CTS}$ is still high when the transmitter register is sending the last stop bit, the transmitter will enter its idle state until the next high-to-low transition on $\overline{CTS}$ occurs. If 0.75 stop bits is chosen, $\overline{CTS}$ input is edge sensitive. A negative edge on $\overline{CTS}$ results in the immediate transmission of the next character. The length of the stop bits is determined by the time interval between the beginning of the first stop bit and the next negative edge on $\overline{CTS}$. A high-to-low transition has no effect if the transmitter buffer is empty or if the time interval between the beginning of the stop bit and next negative edge is less than 0.75 bit. A high or a low level or a low-to-high transition has no effect on the transmitter for the 0.75 stop bit mode.
$\overline{T \times C}$	22	I/O	**Transmit Clock** The function of this pin can be programmed in 3 configurations. As an output it delivers the transmit clock corresponding to the baud rate. If programmed as an input, an external clock of 32 or 64 times the baud rate that is common to transmitter and receiver, or a 1× clock matching the baud rate which is used for the transmitter only, can be tied to this pin. The maximum frequency is 1.024 MHz. Thus, baud rates ranging from 0 to 16 Kbaud (64×) or from 0 to 32 Kbaud (32×) or from 0 to 1.024 Mbaud (1×) are possible. The internal baud rate generator is disabled if $\overline{T \times C}$ is selected as input.

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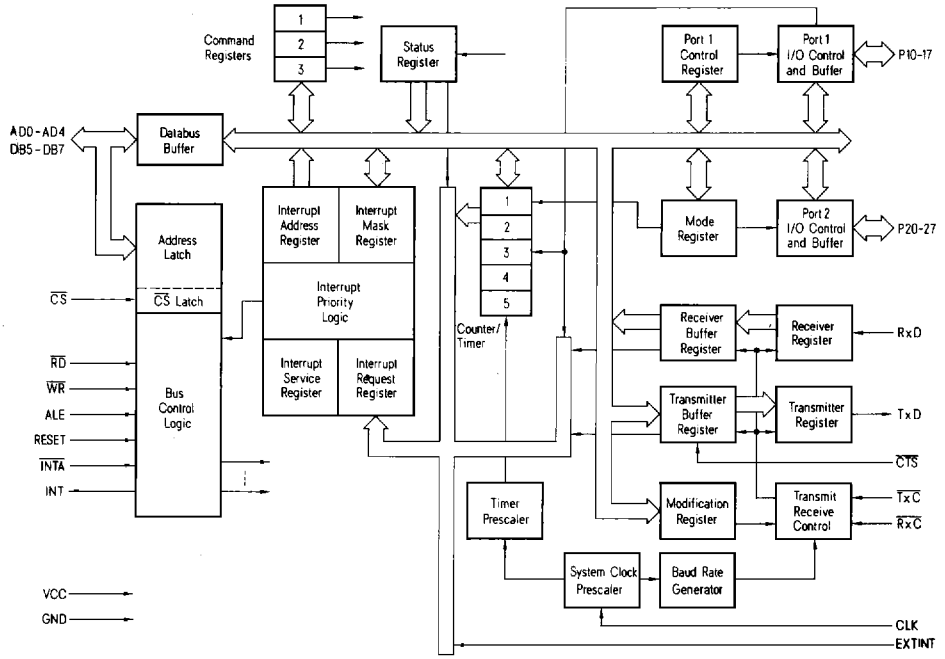
Symbol	Pin	Input (I) Output (O)	Functions
T×D	23	O	**Transmit Data** Serial data output. The parallel data received from the processor and the framing bits added by the SAB 8256A are sent out serially over this output when the transmitter is enabled by the $\overline{CTS}$ signal.
P27–P20	24–31	I/O	**Parallel I/O Port 2** The eight general purpose I/O pins of parallel port 2 can be configured in sets of four pins (nibbles) as inputs or outputs or 8 bit I/O with handshake (control signals at port 1). In the nibble mode the output signals are latched whereas the input signals are not. In the handshake mode both inputs and outputs are latched.
P17–P10	32–39	I/O	**Parallel I/O Port 1** Each one of these 8 pins can be programmed as input or output. Alternatively these pins can serve as control pins which extends considerably the functional spectrum of the chip. The pins are assigned to special functions implicitly by programming. All outputs are latched whereas inputs are not.
V_{CC}	40	–	**Power Supply** (+5 V)
GND	20	–	**Ground** (0 V)

Block Diagram



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Functional Description

Bus Interface

The bus interface unit, consisting of bus drivers, address latches and bus control logic, interfaces the SAB 8256A to the data, address and control buses of a microcomputer system. The chip is selected by the $\overline{CS}$ signal, which is latched into the chip along with address lines AD0–AD4 by the ALE signal. $\overline{WR}$ and $\overline{RD}$ signals are used to write data into and read data from SAB 8256A.
Signals INT und $\overline{INTA}$ are used to handle interrupt protocol with the processor.
RESET signal resets the chip to its initial state.

Counter/Timers

Five programmable counter/timers can be used in several modes. Each can be used as an 8-bit timer while two can alternatively serve as counters. Counter/timer 2 and timer 4 as well as counter/timers and timer 5 can be cascaded to 16-bit counter/timers. All counter/timers function as binary down-counters with a programmable initial value and generate an interrupt request on their 1 to 0 transition. An internal register is provided for the initial count of timer 5 and with an external trigger pulse it is possible to reload the initial value into timer 5 (also for cascaded counter/timer 3 and timer 5).
A common clock source with a frequency of either 1 KHz or 16 KHz is available for the timers. In addition, for counters 2, 3 and the cascaded counters, an external clock source can be provided through two pins of part 1.

Asynchronous Serial Interface

For double buffered full-duplex operations both transmitter and receiver have two registers. The received data (5 to 8 data bits, programmable) is assembled to parallel format in the receiver register, the framing bits (Start, Stop, and Parity) are stripped off and stored into the receiver buffer register. The data to be transmitted is first loaded into the transmitter buffer register and then sent out through the transmitter register.
Controlling the $\overline{CTS}$ signal, single characters on character strings can be transmitted. Baud rate clock (50 to 19,200 Baud) is generated on the chip which is common to both the receiver and the transmitter. It is also possible to provide an external baud rate clock (common or separate for receiver and transmitter) to provide baud rates from 0 to 1.024 Mbaud.

Parallel Interface

The parallel interface consists of two 8-bit ports programmable as inputs or outputs. Each pin of port 1 can be programmed separately as an input or an output. They can also be used as control pins. Port 2 can be programmed as input or output in two 4-bit groups. Port 2 can also be used as an 8-bit input or output port with handshake signals.

Assignment of Control Signals to Port 1

Pins Port 1	P17	P16	P15	P14	P13	P12	P11	P10
Control Function	External interrupt input	Break-In detect input	Trigger input for timer 5 (cascaded counter/ timer 3+5)	Output of the clock of the internal baudrate generator	Clock input for counter 3	Clock input for counter 2	Handshake Control Signals for Port 2	

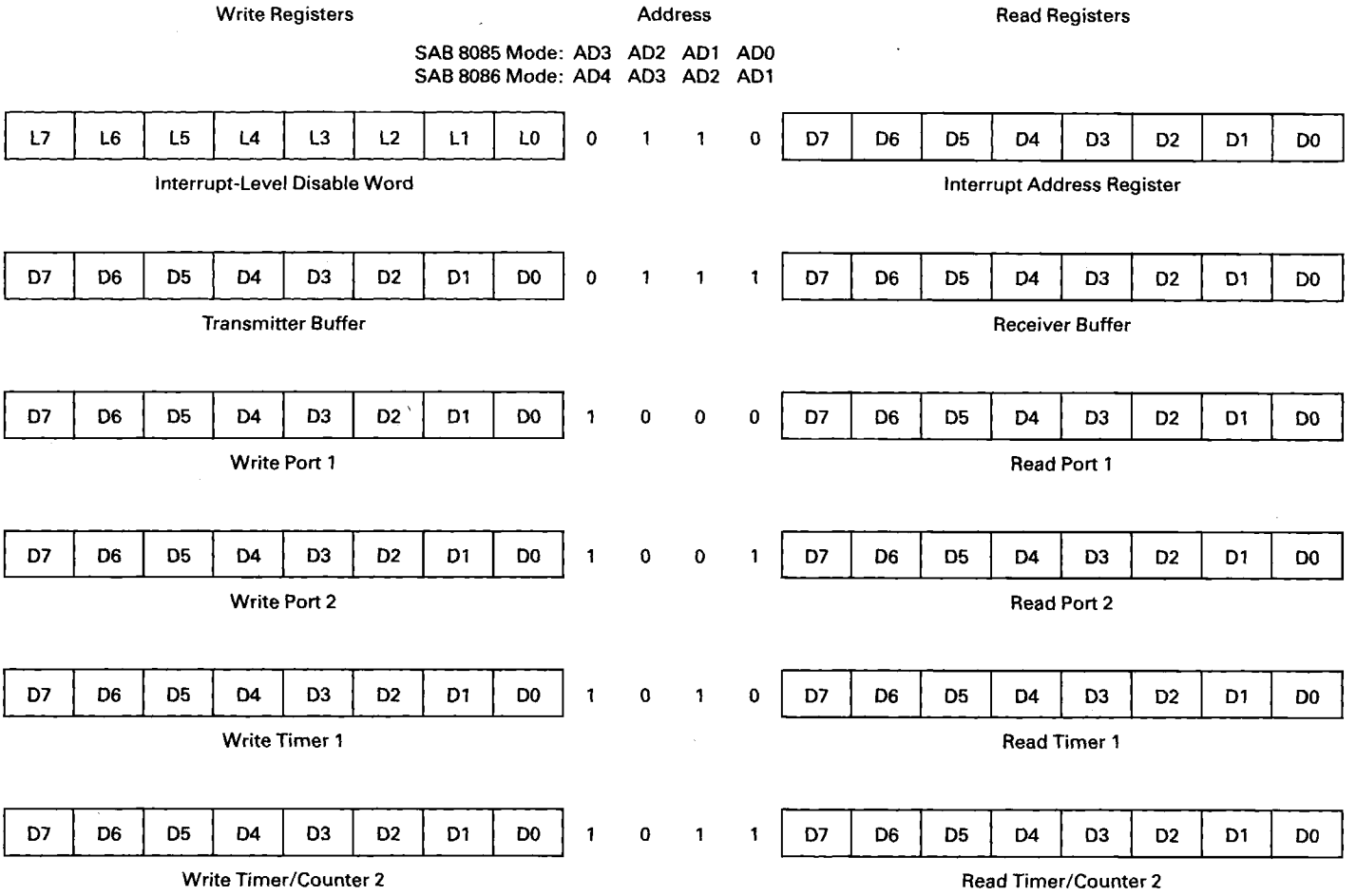
Interrupt Controller

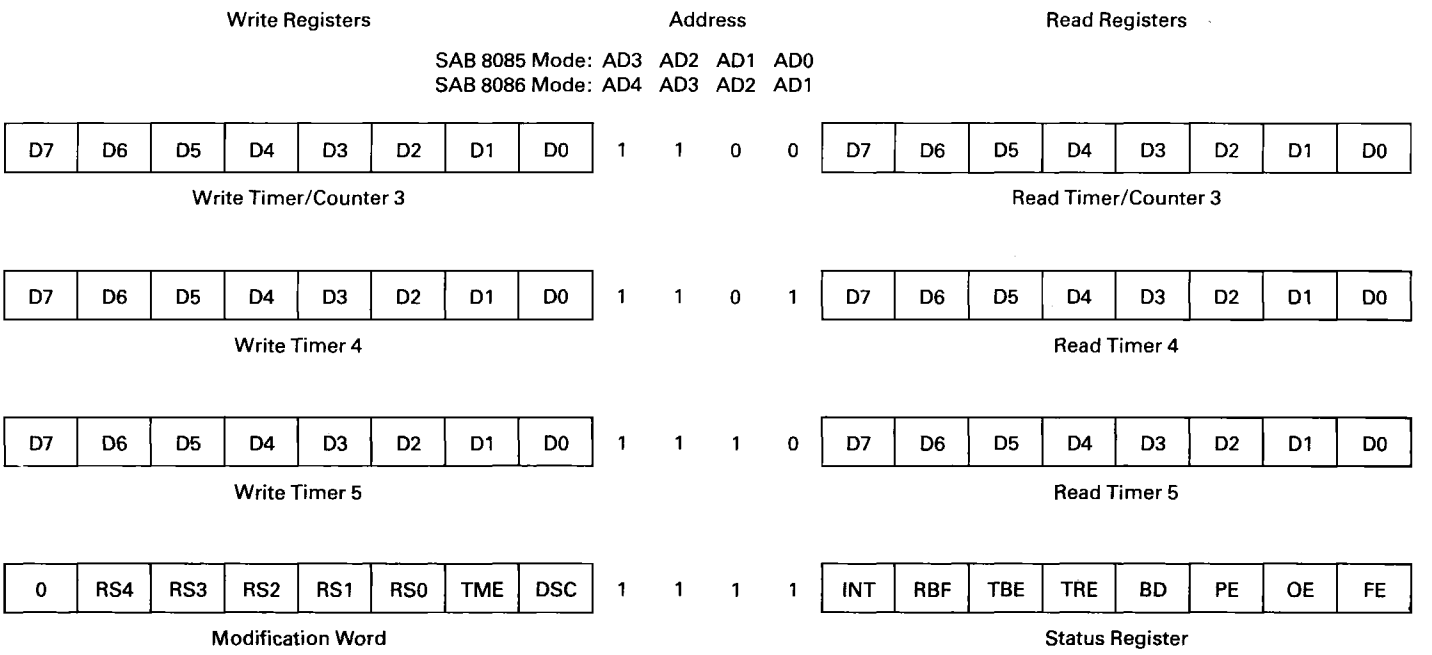
The interrupt controller manages 12 interrupt sources (10 internal and 2 external) on 8 priority levels. Normal (every interrupt request immediately recognized) and "fully nested" (recognition based on priority) mode are supported.
The interrupt controller supports various methods of connecting SAB 8256A to the processor. Firstly, the true interrupt mode (using INT and $\overline{\text{INTA}}$ signals for interrupt protocol), secondly, a combination of polling and interrupt (using INT and interrupt address registers). The interrupt protocols of SAB 8048, SAB 8085A, SAB 8086, SAB 8088, SAB 80186 and SAB 80188 are directly supported.

Programming the SAB 8256A

The functional characteristics of SAB 8256A can be programmed by writing appropriate control information into it. It is specially designed for ease of programming. Thus, it is possible to alter individual bits in certain registers like e.g. the Interrupt Mask Register and Command Register 3. All functions of SAB 8256A can be easily used because each unit (e.g. counter/timer, serial interface) has specially assigned registers which can be directly read or written.

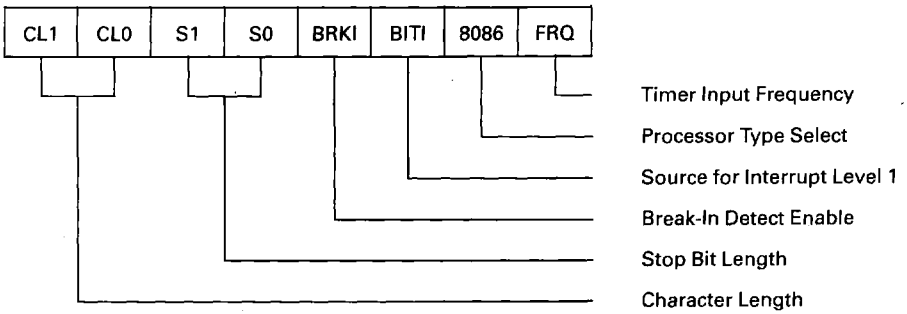
Write Registers								Address				Read Registers							
								SAB 8085 Mode: AD3	AD2	AD1	AD0								
								SAB 8086 Mode: AD4	AD3	AD2	AD1								
CL1	CL0	S1	S0	BRKI	BITI	8086	FRQ	0	0	0	0	CL1	CL0	S1	S0	BRKI	BITI	8086	FRQ
Command Word 1												Command Register 1							
PEN	EP	C1	C0	B3	B2	B1	B0	0	0	0	1	PEN	EP	C1	C0	B3	B2	B1	B0
Command Word 2												Command Register 2							
SET	R×E	IAE	NIE	END	SBRK	TBRK	SRES	0	0	1	0	0	R×E	IAE	NIE	0	SBRK	TBRK	0
Command Word 3												Command Register 3							
T35	T24	T5C	CT3	CT2	P2C2	P2C1	P2C0	0	0	1	1	T35	T24	T5C	CT3	CT2	P2C2	P2C1	P2C0
Mode Word												Mode Register							
P17	P16	P15	P14	P13	P12	P11	P10	0	1	0	0	P17	P16	P15	P14	P13	P12	P11	P10
Port 1 Control Word												Port 1 Control Register							
L7	L6	L5	L4	L3	L2	L1	L0	0	1	0	1	L7	L6	L5	L4	L3	L2	L1	L0
Interrupt-Level Enable Word												Interrupt Mask Register							


Write Registers
Address
Read Registers
SAB 8085 Mode: AD3 AD2 AD1 AD0
SAB 8086 Mode: AD4 AD3 AD2 AD1
L7 L6 L5 L4 L3 L2 L1 L0 0 1 1 0 D7 D6 D5 D4 D3 D2 D1 D0
Interrupt-Level Disable Word
Interrupt Address Register
D7 D6 D5 D4 D3 D2 D1 D0 0 1 1 1 D7 D6 D5 D4 D3 D2 D1 D0
Transmitter Buffer
Receiver Buffer
D7 D6 D5 D4 D3 D2 D1 D0 1 0 0 0 D7 D6 D5 D4 D3 D2 D1 D0
Write Port 1
Read Port 1
D7 D6 D5 D4 D3 D2 D1 D0 1 0 0 1 D7 D6 D5 D4 D3 D2 D1 D0
Write Port 2
Read Port 2
D7 D6 D5 D4 D3 D2 D1 D0 1 0 1 0 D7 D6 D5 D4 D3 D2 D1 D0
Write Timer 1
Read Timer 1
D7 D6 D5 D4 D3 D2 D1 D0 1 0 1 1 D7 D6 D5 D4 D3 D2 D1 D0
Write Timer/Counter 2
Read Timer/Counter 2

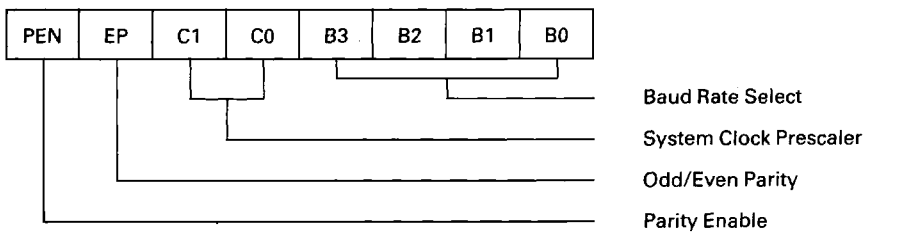

Write Registers
Address
Read Registers
SAB 8085 Mode: AD3 AD2 AD1 AD0
SAB 8086 Mode: AD4 AD3 AD2 AD1
D7 D6 D5 D4 D3 D2 D1 D0
1 1 0 0
Write Timer/Counter 3
Read Timer/Counter 3
1 1 0 1
Write Timer 4
Read Timer 4
1 1 1 0
Write Timer 5
Read Timer 5
0 RS4 RS3 RS2 RS1 RS0 TME DSC
1 1 1 1
Modification Word
INT RBF TBE TRE BD PE OE FE
Status Register

Programming

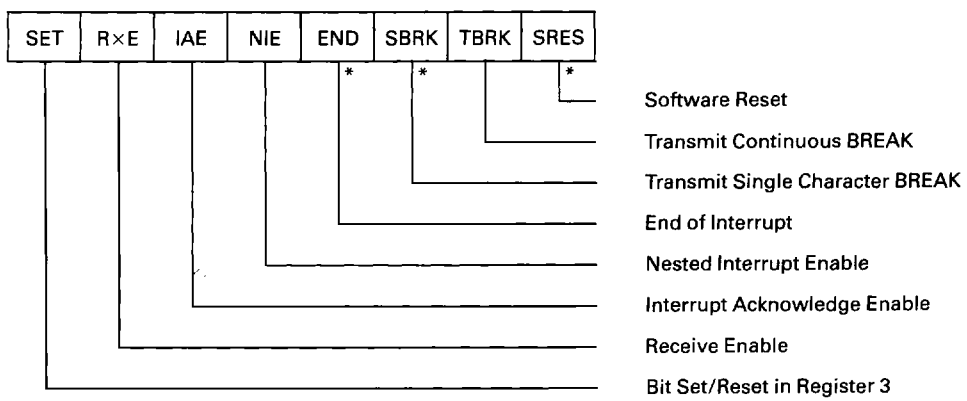
Command Word 1



Command Word 2



Command Word 3



*) These bits can only be set, they are reset at the end of the operation.

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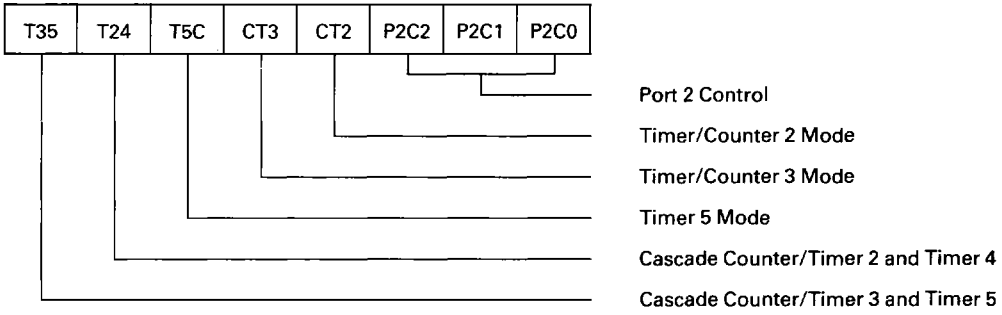
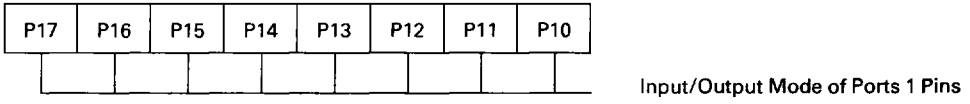
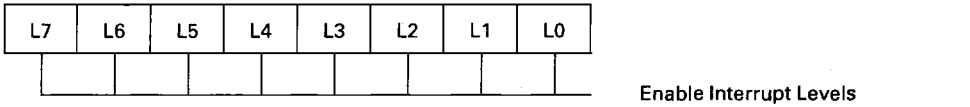
Mode Word



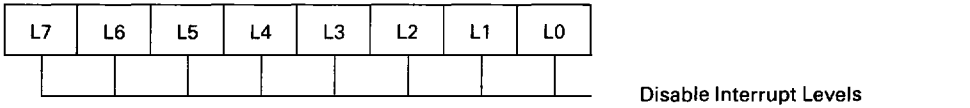
Port 1 Control World



Interrupt-Level Enable Word

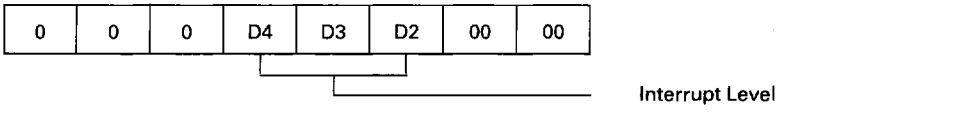


Interrupt-Level Disable Word



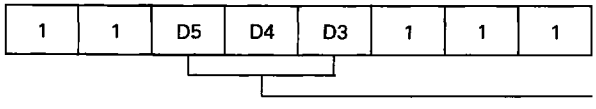
Determination of Interrupt Level

Reading the Interrupt Address Register

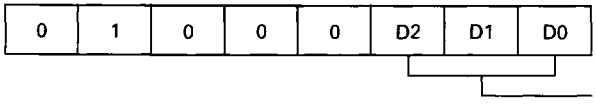


Response to $\overline{INTA}$

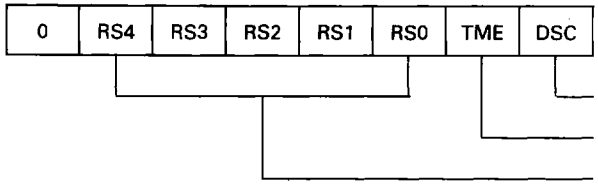
SAB 8085-Mode (RST-instruction in response to $\overline{INTA}$)



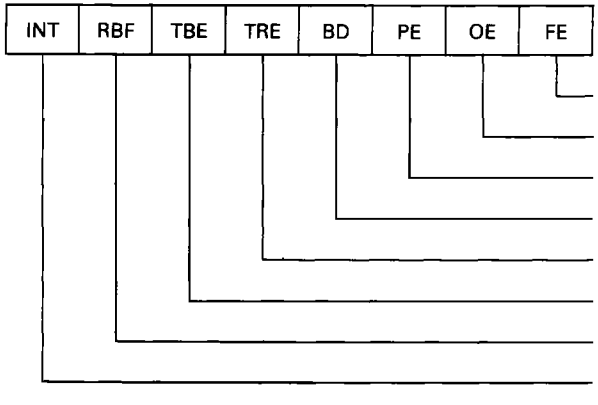
SAB 8086-Mode (Interrupt Vector in response to second $\overline{INTA}$)



Modification Word



Status Register



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Absolute Maximum Ratings

Ambient temperature under bias	0 to 70°C
Storage temperature	−65 to +150°C
Voltage on any pin with respect to ground	−0.5 to +7 V
Power dissipation	1 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V
(if not otherwise specified)

Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
Input low voltage	V_{IL}	−0.5	0.8	V	–
Input high voltage	V_{IH}	2.0	V_{CC}+0.5	V	–
Output low voltage	V_{OL}	–	0.45	V	I_{OL} = 2.5 mA
Output high voltage	V_{OH}	2.4	–	V	I_{OH} = −400 µA
Input leakage	I_{IL}	–	±10	µA	V_{IN} = 0 V to V_{CC}
Output leakage current	I_{LO}	–	±10	µA	V_{OUT} = 0 V to V_{CC}
V_{CC} supply current	I_{CC}	–	190	mA	–

Capacitance [1]

Parameter	Symbol	Limit value (max.)	Unit	Test conditions
Input capacitance	C_{IN}	10	pF	f_C = 1 MHz Unmeasured pins returned to GND
I/O capacitance	$C_{I/O}$	20	pF	

[1] This parameter is periodically sampled and not 100% tested.

AC Characteristics

T_A = 0 to 70°C; V_{CC} = +5 V ± 5%; V_{SS} = 0 V

Test Conditions

Capacitive load C_L = 150 pF

The timings are with respect to the following levels:

H-level: 2.0 V
L-level: 0.8 V
Rise and fall times: 20 ns

The timings are valid for an internal clock of 1.024 MHz.

Parameter	Symbol	Limit values				Unit	Test conditions
		SAB 8256A		SAB 8256A-2			
		min.	max.	min.	max.		
$\overline{STB}\downarrow$ to $\overline{IBF}\downarrow$	t_{AC}	–	300	–	300	ns	–
$\overline{ACK}$ pulse width	t_{ACK}	t_{ADP}	–	t_{ADP}	–	–	–
Address stable to data valid	t_{AD}	–	400	–	230	ns	–
$\overline{ACK}\uparrow$ to $\overline{OBF}\downarrow$	t_{ADP}	–	300	–	300	ns	–
$\overline{OBF}\downarrow$ to $\overline{ACK}\downarrow$	t_{AED}	0	–	0	–	ns	–
$\overline{ACK}\uparrow$ to INT $\uparrow$	t_{AI}	–	1.5 t_{CY}	–	1.5 t_{CY}	–	–
Address stable to ALE $\downarrow$	t_{AL}	50	–	30	–	ns	–
$\overline{RD}$ and $\overline{WR}$ pulse widths	t_{CC}	300	–	200	–	ns	–
$\overline{RD}\uparrow$ or $\overline{WR}\uparrow$ to next ALE $\uparrow$	t_{CL}	50	–	25	–	ns	–
Counter input cycle time (P12, P13,)	t_{CPI}	2.2	–	2.2	–	µs	–
$\overline{CS}$ stable to ALE $\downarrow$	t_{CSL}	60	–	10	–	ns	–
$\overline{CTS}$ pulse width for single character transmission	t_{CTS}	[1]	–	[1]	–	–	–
System clock period	t_{CY}	300	–	195	–	ns	–
$\overline{STB}\uparrow$ to INT $\uparrow$	t_{DEI}	–	1.5 t_{CY}	–	1.5 t_{CY}	–	–
EXTINT $\uparrow$ to INT $\uparrow$	t_{DEX}	–	200	–	200	ns	–
$\overline{STB}\uparrow$ to P2 data stable	t_{DH}	10	–	10	–	ns	–
Interrupt request on P17 to INT $\uparrow$	t_{DPI}	–	1.5 t_{CY}	–	1.5 t_{CY}	–	–
P2 data stable before $\overline{STB}\downarrow$	t_{DSI}	10	–	10	–	ns	–
$\overline{T\times C}\downarrow$ to T×D data valid	t_{DTX}	–	300	–	300	ns	–
Data valid before $\overline{WR}\uparrow$	t_{DW}	250	–	150	–	ns	–
EXTINT $\downarrow$ after $\overline{INTA}\uparrow$ or $\overline{RD}\uparrow$	t_{HEA}	30	–	30	–	ns	–
INT $\downarrow$ after $\overline{INTA}\uparrow$ or $\overline{RD}\uparrow$	t_{HIA}	–	300	–	300	ns	–
$\overline{CS}$ and address valid after ALE $\downarrow$	t_{LA}	50	–	20	–	ns	–
ALE $\downarrow$ to $\overline{RD}\downarrow$ or $\overline{WR}\downarrow$	t_{LC}	60	–	20	–	ns	–
ALE pulse width	t_{LL}	100	–	50	–	ns	–

Notes see next page.

Parameter	Symbol	Limit values				Unit	Test conditions
		SAB 8256A		SAB 8256A-2			
		min.	max.	min.	max.		
Pulse width of interrupt request on P17	t_{PI}	1.1	–	1.1	–	µs	–
Counter 5 load (P15↓) before next clock pulse on P13 ↑	t_{PP}	1.1	–	1.1	–	µs	–
P1, P2 data stable before $\overline{RD}$ ↓	t_{PR}	300	–	300	–	ns	–
Data valid after $\overline{RD}$ ↓	t_{RD}	–	200	–	150	ns	–
$\overline{RD}$ ↓ to data drivers active	t_{RDE}	10	100	10	50	ns	–
Data bus float after $\overline{RD}$ ↑	t_{RDF}	10	100	10	50	ns	–
RESET pulse width	t_{RES}	300	–	300	–	ns	–
$\overline{RD}$ ↑ to $\overline{IBF}$ ↑	t_{RI}	–	300	–	300	ns	–
P1, P2 data hold after $\overline{RD}$ ↑	t_{RP}	50	–	50	–	ns	–
Data bit start to $\overline{R \times C}$ ↓	t_{RRD}	300	[2]	150	[2]	ns	[3]
$\overline{RD}$ ↑ or $\overline{WR}$ ↑ to next $\overline{RD}$ ↓ or $\overline{WR}$ ↓	t_{RV}	300	–	150	–	ns	$\overline{CS}$=low
Serial clock period (32×, 64×)	t_{SCY}	975	–	975	–	ns	–
Serial clock high (32×, 64×)	t_{SPD}	350	–	350	–	ns	–
Serial clock low (32×, 64×)	t_{SPW}	350	–	350	–	ns	–
Strobe pulse width	t_{STB}	t_{AC}	–	t_{AC}	–	–	–
Serial clock period (1×)	t_{TCY}	975	–	975	–	ns	–
Serial clock high (1×)	t_{TPD}	350	–	350	–	ns	–
Load pulse for counter 5 (P15)-high	t_{TIH}	1.1	–	1.1	–	µs	–
Load pulse for counter 5 (P15)-low	t_{TIL}	1.1	–	1.1	–	µs	–
Counter input ↑ (P12, P13) to INT ↑ at terminal count	t_{TPI}	–	2.5	–	2.5	µs	–
Serial clock low (1)	t_{TPW}	350	–	350	–	ns	–
Time between 2 read cycles onto the same counter/timer	t_{TRV}	1.1	–	1.1	–	µs	–
Data hold after $\overline{WR}$ ↑	t_{WD}	40	–	30	–	ns	–
P1, P2 data valid after $\overline{WR}$ ↑	t_{WP}	–	300	–	300	ns	–
Count clock (P12, P13) high	t_{WPH}	1.1	–	1.1	–	µs	–
Count clock (P12, P13) low	t_{WPL}	1.1	–	1.1	–	µs	–
$\overline{OBF}$ ↑ after $\overline{WR}$ ↓	t_{WPO}	–	300	–	300	ns	–
Clock fall time	t_f	–	30	–	30	ns	–
Clock high	$t_{\Phi H}$	105	–	65	–	ns	–
Clock low	$t_{\Phi L}$	105	–	65	–	ns	–
Clock rise time	t_r	–	30	–	30	ns	–

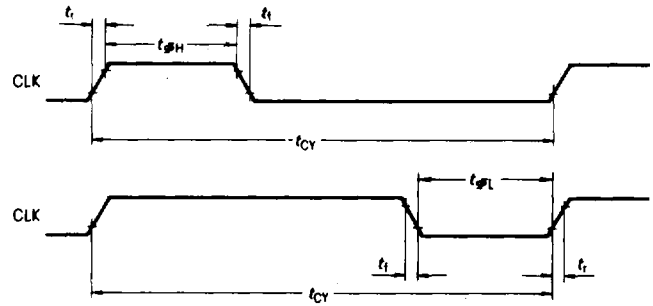
[1] 1/32 bit length with transmitter clock with a baud rate factor of 32 or 64. 100 ns when baud rate factor = 1

[2] 300 ns + (1/32 bit length)

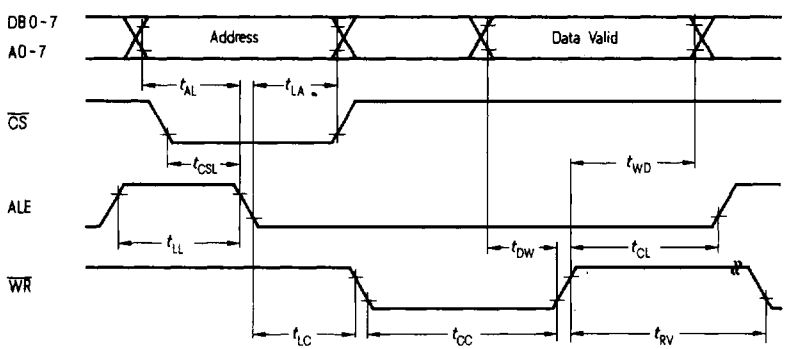
[3] Sampling time at bit center

Waveforms

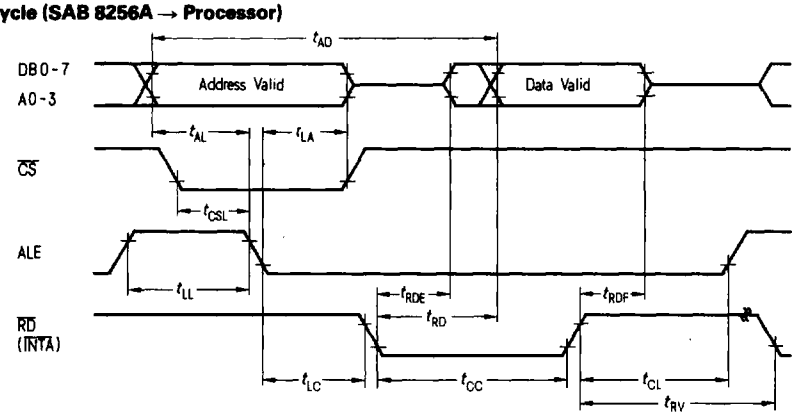
System Clock



Write Cycle (Processor → SAB 8256A)

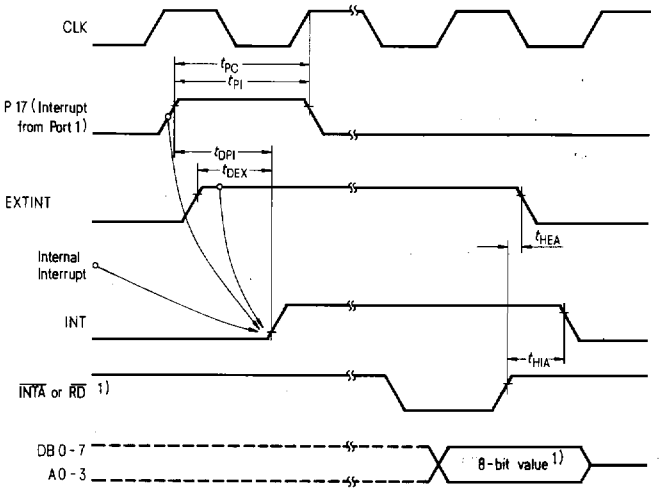


Read Cycle (SAB 8256A → Processor)

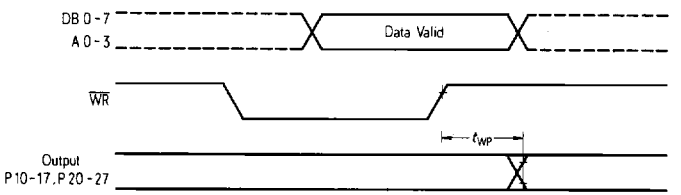


4

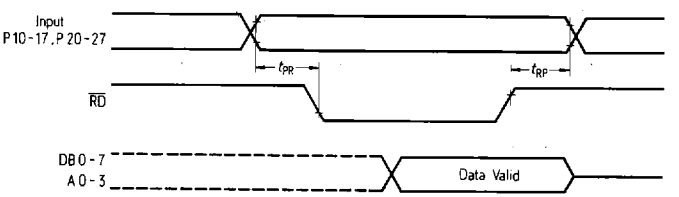
Interrupt Timings



Basic Output from Port 1 and Port 2

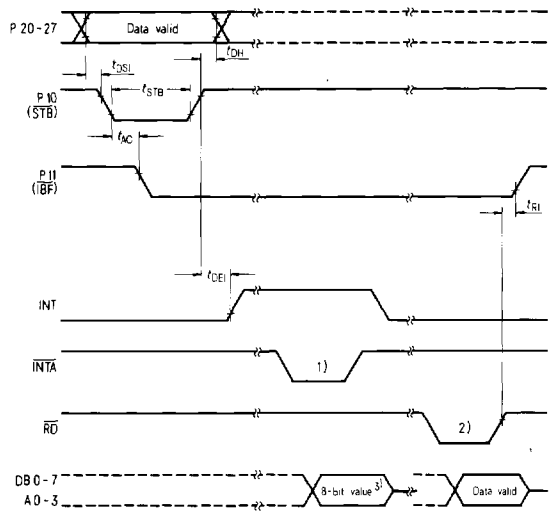


Basic Input from Port 1 and Port 2

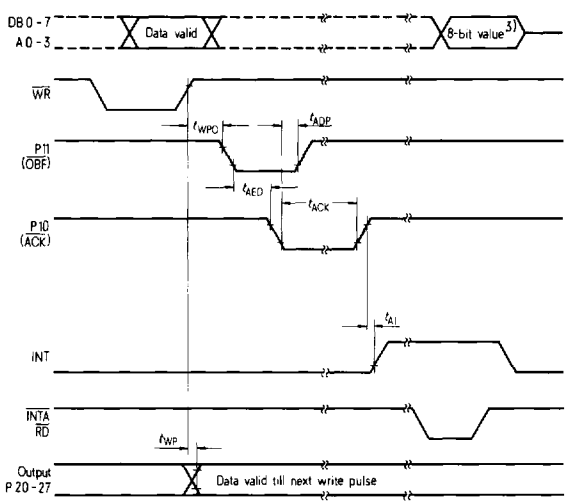


1) If INTA is enabled, RST instruction is output on INTA (SAB 8085 mode) or interrupt vector is output on second INTA (SAB 8086 mode) otherwise, interrupt address is output on a read address register operation.

Input from Port 2 in Handshake Mode (Control Signals from Port 1)



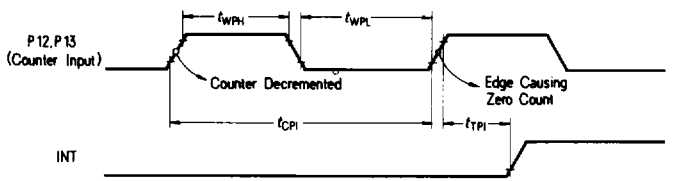
Output from Port 2 in Handshake Mode (Control Signals from Port 1)



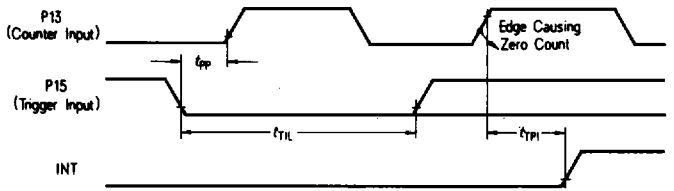
1) Instead of $\overline{INTA}$, $\overline{RD}$ can serve as interrupt acknowledge (reading the interrupt address register).
2) Read from channel 2.
3) If $\overline{INTA}$ is enabled, RST instruction is output on $\overline{INTA}$ (SAB 8085 mode) or interrupt vector is output on second $\overline{INTA}$ (8086 mode). Otherwise, interrupt address is output on a read address register operation.

4

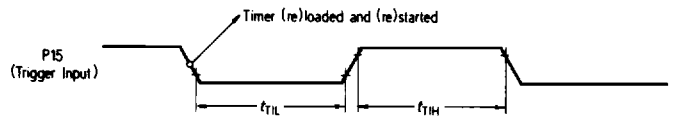
Count Pulse Timings and Zero-Crossing of Counter



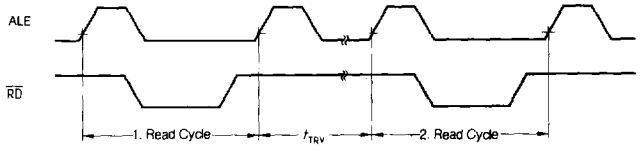
Loading Timer 5 (or Cascaded Counter/Timer 3 and 5) and Zero-Crossing of Counters (Cascaded Counter/Timer 3 and 5)



Trigger Pulse for Timer 5 (Cascaded Event Counter/Timer 3 and 5)

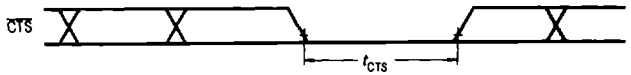


Reading Event Counters/Timers

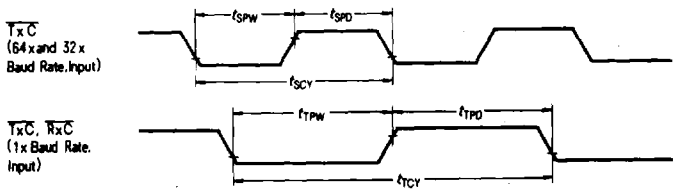


Reset Timing

CTS for Single Character Transmission

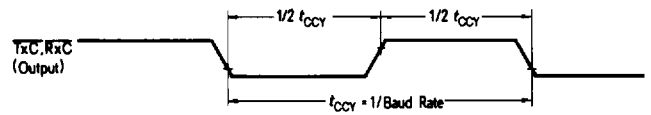


External Baud Rate Clock for Serial Interface

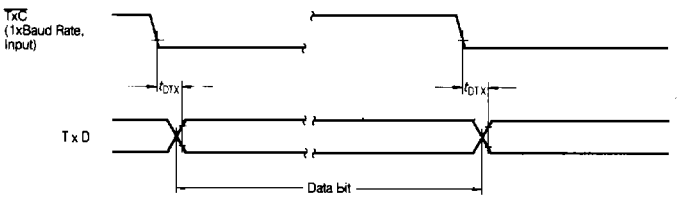


4

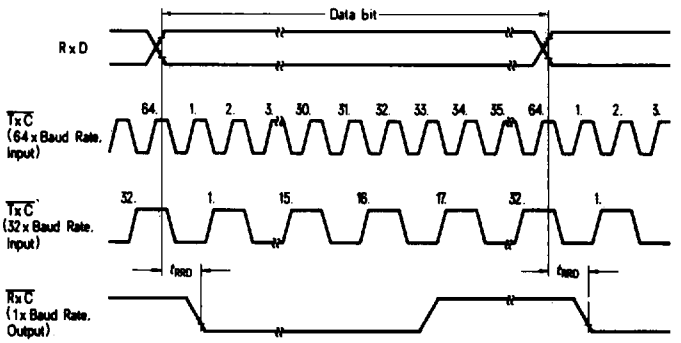
Transmitter and Receiver Clock from Internal Clock Source



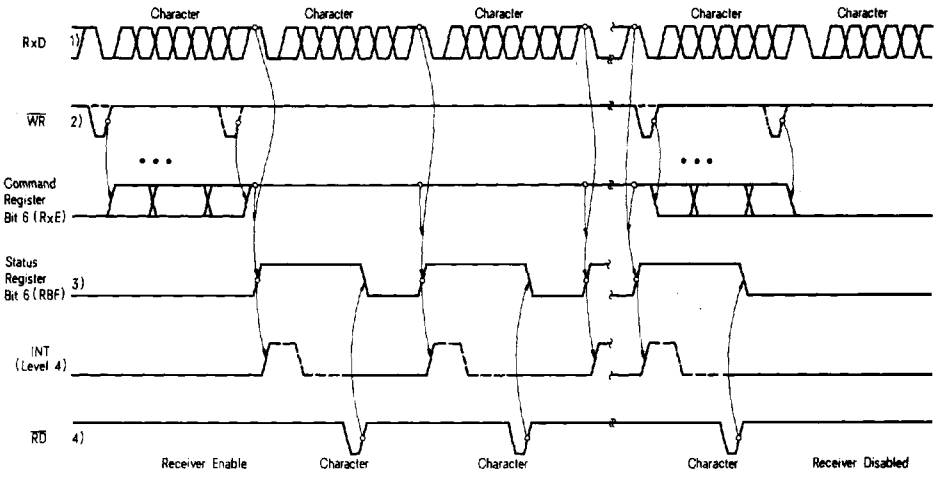
Data Bit Output on Serial Interface



Data Bit Input on Serial Interface



Continuous Reception of Characters on Serial Interface without Error Conditions

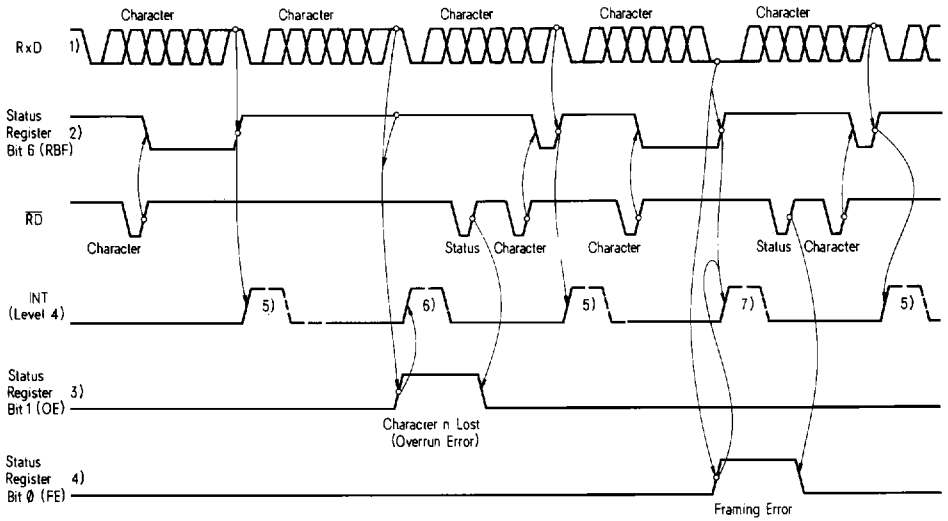


1) Character format for this example: 6 data bits with parity bit and one stop bit.
2) Set or reset bit 6 of command register 3 (enable receiver)
3) Receiver buffer loaded
4) Read receiver buffer register
5) Receiver is active even though no data is sent or status bit set.

No status bits are altered when $\overline{RD}$ is active.

4

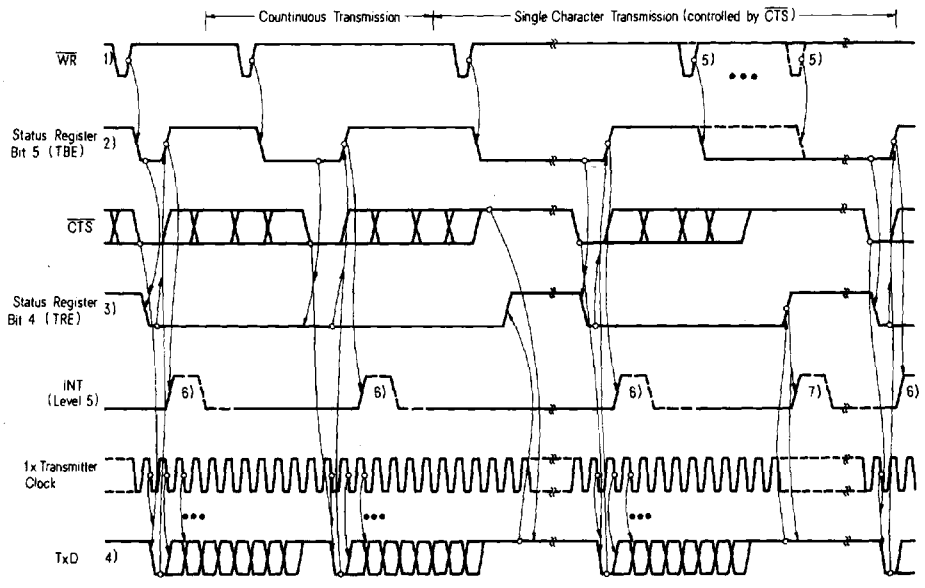
Error Conditions during Reception of Characters on the Serial Interface



1) Character format for this example: 6 data bits without parity and one stop bit
2) Receiver buffer register loaded
3) Overrun error
4) Framing error
5) Interrupt from receiver buffer register loading
6) Interrupt from overrun error
7) Interrupt from framing error and loading receiver buffer register

No status bits are altered when $\overline{RD}$ is active.

Transmission of Characters on Serial Interface



1) Load transmitter buffer register
2) Transmitter buffer register is empty
3) Transmitter register is empty
4) Character format for this example: 7 data bits with parity bit and 2 stop bits
5) Loading of transmitter buffer register must be completed before $\overline{CTS}$ goes low
6) Interrupt due to transmitter buffer register empty
7) Interrupt due to transmitter register empty

No status bits are altered when $\overline{RD}$ is active.

4