Part Number:EP952

Overview

EP952 is a Low Power HDMI (High Definition Multimedia Interface) transmitter. The chip is compliant with HDMI Rev 1.4 and HDCP Rev 1.4 specifications. The chip converts input video data in RGB or YUV format and audio data in IIS or SPDIF format into HDMI differential signals. The chip supports 8-bit video upto 1080p in HDMI mode. The chip also supports 3D video. The chip supports highly flexible digital video input in a muxed 12-bits mode or non-muxed 24-bit mode input. In both modes, the chip supports single or dual edge clocking.

Features

•HDMI Specification 1.4 Compliant
•Integrated HDCP encryption engine which is compliant with HDCP Rev 1.4 specification for transmitting protected content
•Integrated on-chip HDCP Keys (Optional)
•Wide TMDS Clock Frequency Range: 25MHz – 165MHz in HDMI mode
•Support 8-bit video upto 1080p in HDMI mode
•Support 3D video
•Support IIS and SPDIF (LPCM or compressed) audio types
•Support auto-send for DVI, ADO, ACR (Audio Clock Regeneration) and General Control packets.
•Support 1 Generic Data Packet buffer
•Flexible digital video input: muxed 12-bit and non-muxed 24-bit mode in RGB or YUV, embedded sync or separate sync
•Support 1 port of SPDIF audio input (without the need for system clock) and 2 channels of IIS audio inputs
•Supports audio down sampling at 1/2, 1/3 or 1/4 sampling rate for both SPDIF and IIS
•Supports CCIR YUV422 format input
•On-chip YUV422 to YUV444 conversion and YUV444 to YUV422 conversion
•On-chip YUV to RGB and RGB to YUB conversion in ITU-R BT.601 and 709 color space
•Register Programmable Single/Dual Edge Clocking Mode
•IIC Slave Programming Interface
•Programmable DE generation
•Supports x2, x4 and x8 Pixel Repetition
•Supports input De-Skewing
•Supports Receiver Hot Plug Detection
•Downward compatible with DVI 1.0
•Supports Power Down Mode
•3.3V and 1.8V power required

Block Diagram

Figure 2-1 Block Diagram