OKI Semiconductor

This version: Nov. 1997
Previous version: Mar. 1996

MSM5298A

68-DOT COMMON DRIVER

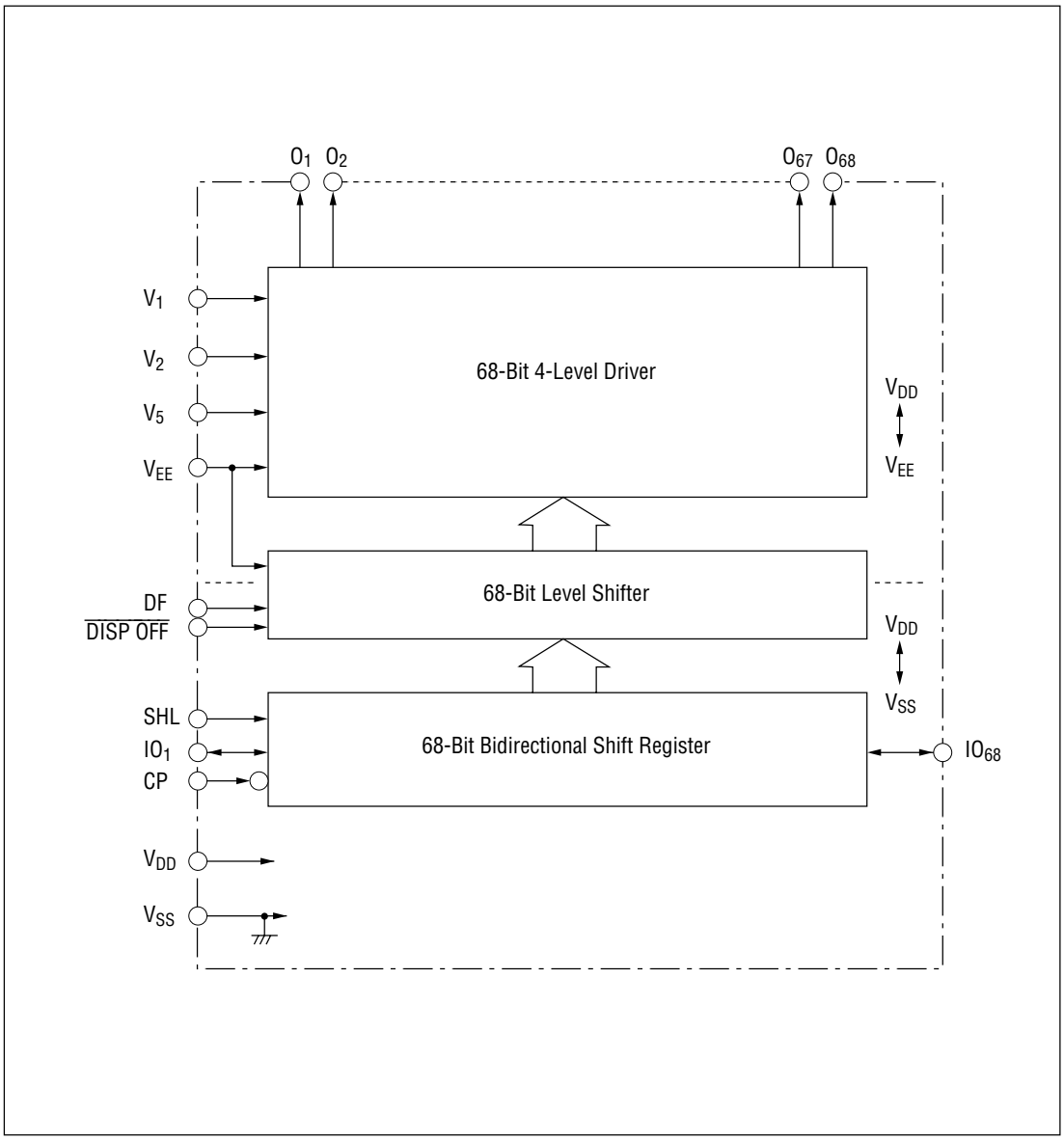
GENERAL DESCRIPTION

The MSM5298A is a dot matrix LCD common driver LSI which is fabricated using low power CMOS metal gate technology. This LSI consists of 68-bit bidirectional shift register, 68-bit level shifter and 68-bit 4-level driver.
This LSI has 68 output pins to be connected to the LCD. By connecting two or more MSM5298As in series, this LSI is applicable to a wide LCD panel.

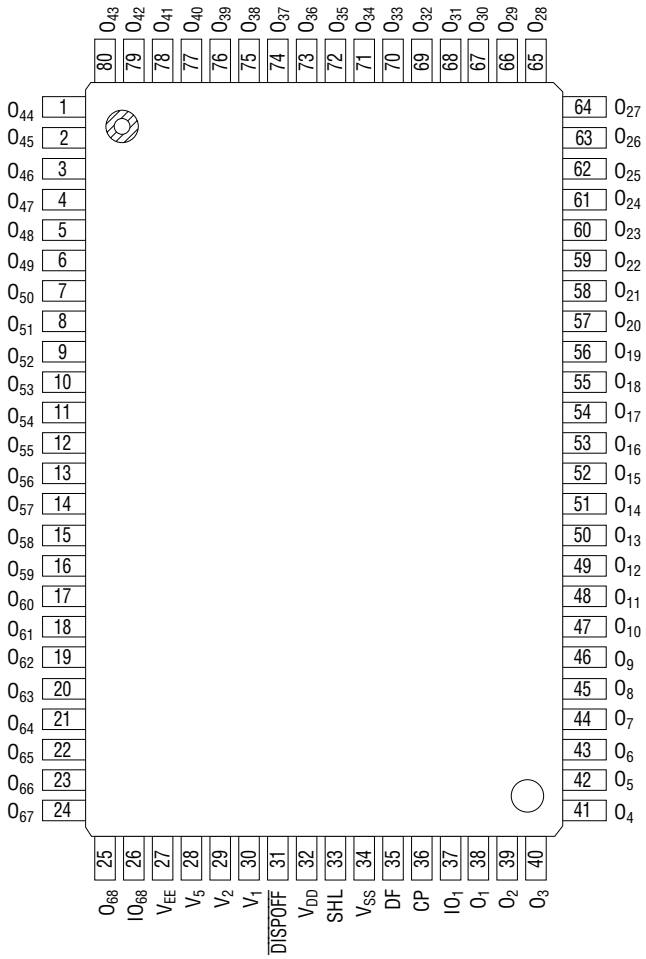
FEATURES

- Supply voltage : 4.5 to 5.5V
- LCD driving voltage : 8 to 28V
- Applicable LCD duty : 1/64 to 1/256
- Applicable segment driver : MSM5299A (80 outputs), MSM5299C (80 outputs)
- Package options:
  80-pin plastic QFP (QFP80-P-1420-0.80-K) (Product name : MSM5298AGS-K)
  80-pin plastic QFP (QFP80-P-1420-0.80-BK) (Product name : MSM5298AGS-BK)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



80-Pin Plastic QFP

Note: The abbreviated part number "M5298A" is imprinted on the package surface.

ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage (1)	V_{DD}	Ta = 25°C	–0.3 to +6	V
Supply Voltage (2)	V_{LCD}	Ta = 25°C, V_{DD}–V_{EE} *1	0 to +30	V
Input Voltage	V_I	Ta = 25°C	–0.3 to V_{DD} +0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

*1 $V_{DD} \geq V_1 > V_2 > V_5 > V_{EE}$

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0 V)

Parameter	Symbol	Condition	Range	Unit
Supply Voltage (1)	V_{DD}	—	4.5 to 5.5	V
Supply Voltage (2)	V_{LCD}	V_{DD}–V_{EE} *1	8 to 28	V
Operating Temperature	T_{op}	—	–20 to +85	°C

*1 $V_{DD} \geq V_1 > V_2 > V_5 > V_{EE}$

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 5V±10%, Ta = –20 to +85°C)

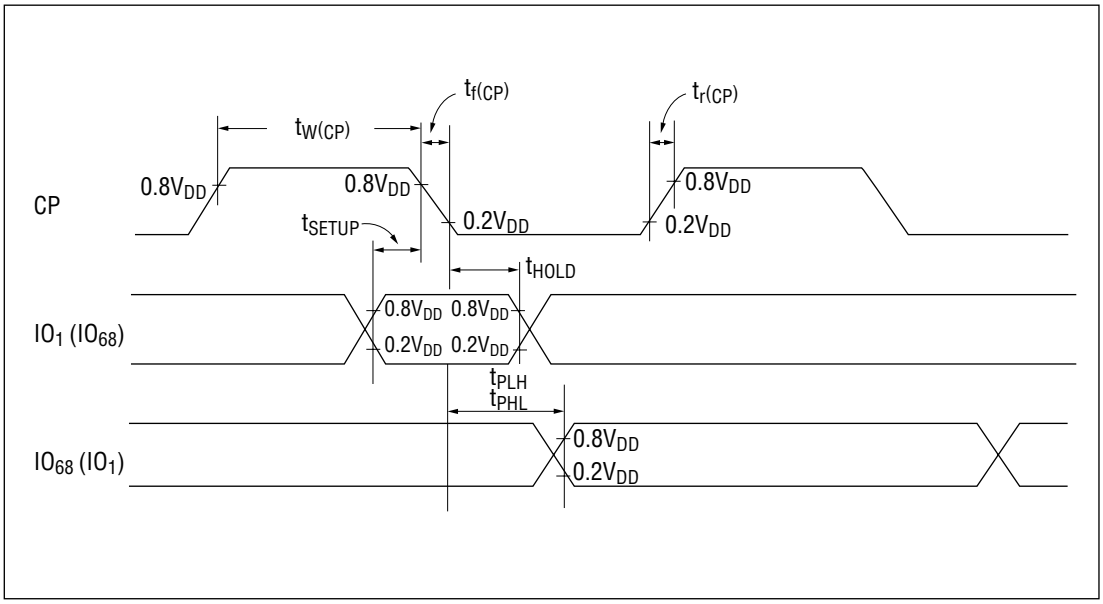
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH} *1	—	0.8V_{DD}	—	V_{DD}	V
"L" Input Voltage	V_{IL} *1	—	V_{SS}	—	0.2V_{DD}	V
"H" Input Current	I_{IH} *1	V_I = V_{DD}, V_{DD} = 5.5V	—	—	1	µA
"L" Input Current	I_{IL} *1	V_I= 0V, V_{DD} = 5.5V	—	—	–1	µA
"H" Output Voltage	V_{OH} *2	I_O= –0.4mA, V_{DD} = 4.5V	V_{DD} – 0.4	—	—	V
"L" Output Voltage	V_{OL} *2	I_O= 0.4mA, V_{DD} = 4.5V	—	—	0.4	V
ON Resistance	R_{ON} *4	V_{DD} – V_{EE} = 23V, V_{DD} = 4.5V $\lvert V_N - V_O \rvert$ = 0.25V *3	—	1.5	3	kΩ
Supply Current	I_{DD}	f_{CP} = 14kHz, V_{DD} = 5.5V V_{DD} – V_{EE} = 23V, No load	—	—	100	µA
Input Capacitance	C_I	f = 1MHz	—	5	—	pF

*1 Applicable to CP, IO_1, IO_{68}, SHL, DF, $\overline{DISP\ OFF}$.
*2 Applicable to IO_1, IO_{68}.
*3 V_N = V_{DD} to V_{EE}, $V_2 = \frac{1}{15}(V_{DD} - V_{EE})$, $V_5 = \frac{14}{15}(V_{DD} - V_{EE})$, $V_{DD} = V_1$
*4 Applicable to O_1 to O_{68}.

Switching Characteristics

(V_{DD} = 5V±10%, Ta = –20 to +85°C, C_L = 15pF)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" , "L" Propagation Delay Time	t_{PLH} t_{PHL}	—	—	—	250	ns
Clock Frequency	f_{CP}	—	—	—	1	MHz
Clock Pulse Width	$t_{W(CP)}$	—	125	—	—	ns
Data Setup Time $IO_1(IO_{68})\rightarrow CP$	t_{SETUP}	—	100	—	—	ns
Data Hold Time $CP\rightarrow IO_1(IO_{68})$	t_{HOLD}	—	100	—	—	ns
Clock Pulse Rise/Fall Time	$t_{r(CP)}$ $t_{f(CP)}$	—	—	—	50	ns



FUNCTIONAL DESCRIPTION

Pin Functional Description

- **IO_1, IO_{68}, SHL**

  IO_1 and IO_{68} are 68-bit bidirectional shift register input/output pins. The shifting direction is selected by the SHL pin. Refer to the table below.

SHL	Shifting direction	IO_1/IO_{68}	Input/ output	Description
L	$O_1 \rightarrow O_{68}$	IO_1	Input	The scanning data from the LCD controller LSI is input into IO_1 synchronized with the clock pulse.* 1
		IO_{68}	Output	Shift register contents output pin. The data which is input into IO_1 is output from IO_{68} with 68 bit's delay, synchronized with the clock pulse.
H	$O_{68} \rightarrow O_1$	IO_{68}	Input	The scanning data from the LCD controller LSI is input into IO_{68} synchronized with the clock pulse.* 1
		IO_1	Output	Shift register contents output pin. The data which is input into IO_{68} is output from IO_1 with 68 bit's delay, synchronized with the clock pulse.

*1 The combination of the scanning data, IO_1 or IO_{68}, and the LCD driving output, O_1 to O_{68}, is shown in the table below.

IO_1, IO_{68}	LCD driving output
"H"	Select level (V_1, V_{EE})
"L"	Non-select level (V_2, V_5)

- **CP**

  Clock pulse input pin for 68-bit bidirectional shift register. The data is shifted to 68-bit bidirectional shift register at the falling edge of the clock pulse.

- **DF**

  Alternate signal input pin for LCD driving.

- **V_{DD}, V_{SS}**

  Supply voltage pins. V_{DD} should be 4.5 to 5.5V. V_{SS} is a ground pin. (V_{SS} = 0V).

- **$\overline{\text{DISP OFF}}$**

  Control input pin for display data output level (O_1 to O_{68}). V_1 level is output from O_1 to O_{68} pin during "L" level input. Refer to Truth Table.

- **V_1, V_2, V_5, V_{EE}**
  Bias supply voltage pins to drive the LCD. The V_1 pin can be separated from the V_{DD} pin.

- **O_1 - O_{68}**
  Display data output pins which correspond to each bit of the 68-bit bidirectional shift register. One of the four levels, V_1, V_2, V_5 and V_{EE}, is selected based on the combination of the latched data level and DF signal. (Refer to Truth Table.)
  Connect these outputs to the common side of the LCD panel.

Truth Table

DF	Shift register data	$\overline{\text{DISP OFF}}$	Driver output level (O_1 to O_{68})
L	L	H	V_2
L	H	H	V_{EE}
H	L	H	V_5
H	H	H	V_1
X	X	L	V_1

X : Don't care

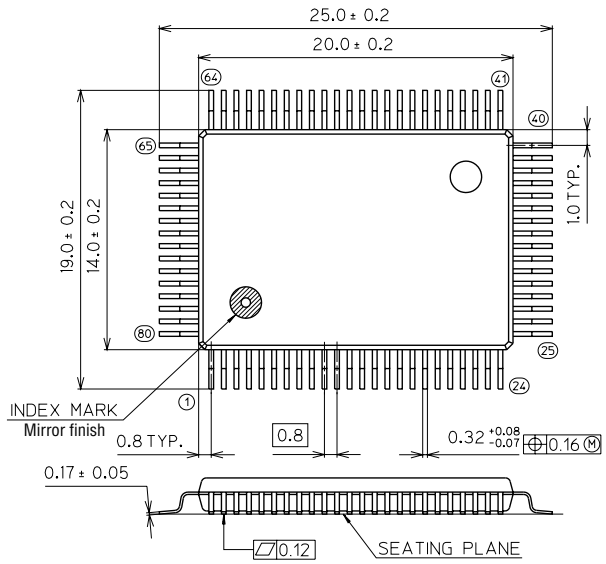
NOTES ON USE (when turning the power ON or OFF)

The LCD drivers of this IC require a high voltage. For this reason, if a high voltage is applied to the LCD drivers with the logic power supply floating, excess current flows. This may damage the IC.
Be sure to follow the sequence below when turning the power ON or OFF.
Power ON : Logic circuits ON → LCD drivers ON, or both ON at a time
Power OFF : LCD drivers OFF → logic circuits OFF, or both OFF at a time

PACKAGE DIMENSIONS

(Unit : mm)

QFP80-P-1420-0.80-K



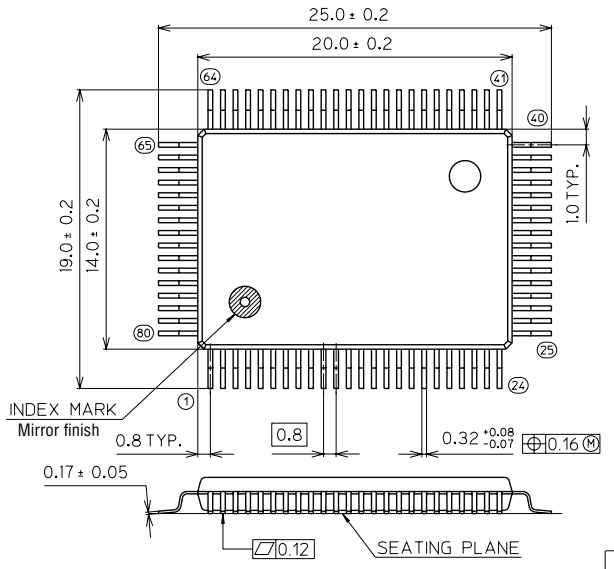
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.27 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFP80-P-1420-0.80-BK



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.27 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).