M223-40

EPSON

Application Manual

Real Time Clock Module
RTC-4513

SEIKO EPSON CORP.

CONTENTS

Serial Interface Real Time Clock Module

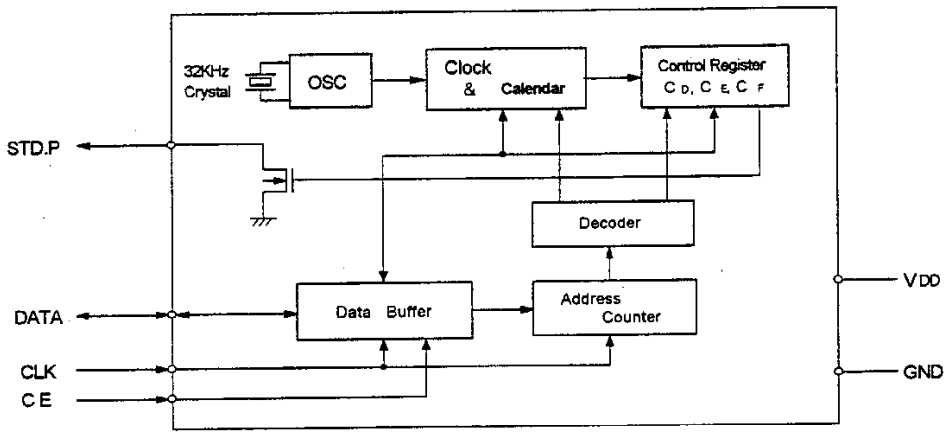
RTC - 4513

- Built-in frequency adjusted 32-kHz quartz crystal
- Serial interface controllable by three signal lines
- Four types of fixed-period interrupts (or cyclic waveform output)
- Automatic leap year compensation
- Software 30-second adjustment function
- Wide operating voltage range (2.7 - 5.5 V)
- Wide data preservation range (2.0 - 5.5 V)
- Low power consumption
- Compact SOP-14 package ideal for high integration applications

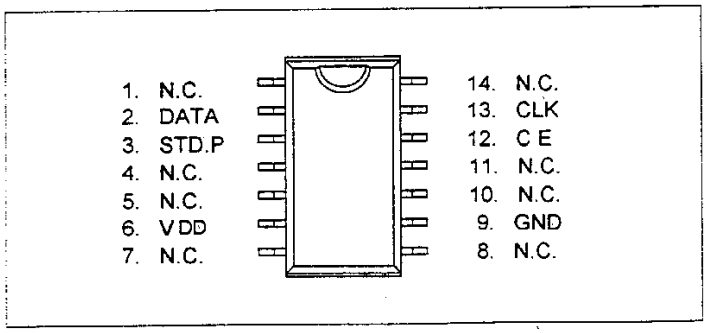
■ Overview

The RTC-4513 is a serial interface real time clock with integrated quartz oscillator. It provides a wide array of features, including clock and calender functions, as well as fixed-period interrupts, 30-second adjustment, automatic leap year compensation, and oscillation stop detection. The serial interface can be controlled by three signal lines, to keep the number of ports on the system side to a minimum. The SOP-14 package is well suited for highly integrated installations where space is at a premium, such as in portable phones, handheld terminals and many other compact electronic devices.

■ Block Diagram



■ Pin Assignment



■ Pin Functions

Signal	Pin no.	I/O	Function
DATA	2	Bidirectional	This pin serves for write mode/read mode selection, address write, and data read/write operations. After activation by the chip enable (CE) input, the write mode/read mode setting in the 8-bit input data determines whether this pin operates as a high- impedance input pin or output pin.
STD.P	3	Output	This pin operates as fixed-cycle open-drain output for the N channel, or as interrupt output for the CPU. The fixed-cycle output serves for verification of the reference signal or the oscillation frequency. Selection of fixed-cycle or interrupt output is performed by writing the INT/STND bit. The output of this pin cannot be inhibited by the CE signal.
V_{DD}	6		Connect to the positive side of the power supply. The voltage must be 2.7 - 5.5 V during normal operation and at least 2.0 V during battery backup operation.
GND	9		Connect to the negative (grounded) side of the power supply.
C E	12	Input	Chip enable input. When the input is High, the chip is selected. When the input is Low, the DATA pin is at high impedance, and the DATA and CLK ports are inhibited internally, to cut off through-current.
CLK	13	Input	Shift clock input. At the rising edge of this signal, data are read (write mode) or output (read mode).
N.C.	1,4,5,7,8, 10,11,14	—	These pins are internally not connected, but to assure stable oscillation, connect them externally.

※ Be sure to connect a bypass capacitor of at least 0.1 μF between VDD and GND.

■ Specifications

1. Absolute Maximum Ratings

Item	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta=25℃	−0.3~7.0	V
Input voltage	V_I		GND-0.3~V_{DD}+0.3	
Output voltage	V_O		GND-0.3~V_{DD}+0.3	
Storage temperature	T_{STG}	—	−55~+125	℃

2. Operation Ratings

Item	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	—	2.7~5.5	V
Clock power supply voltage	V_{CLK}	—	2.0~5.5	V
Operating temperature	T_{OPR}	—	−40~+85	℃

3. Frequency Ratings

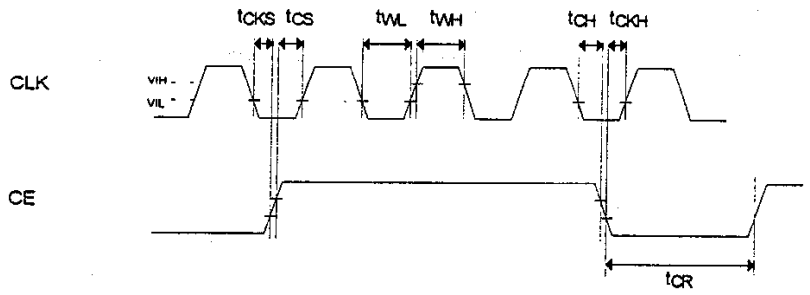
Item	Symbol	Condition	Rating	Unit
Frequency tolerance	Δf/fo	Ta=25℃,VDD=3.0V	0±25	ppm
Temperature-dependent frequency deviation		−10～70℃ 25℃Standard	+10 / −120	ppm
Voltage-dependent frequency deviation		Ta=25℃, VDD=2.0～5.5V	±5 (TYP.)	ppm/V

4. DC Ratings (VDD=2.7V to 5.5V Ta=-40 to 85℃)

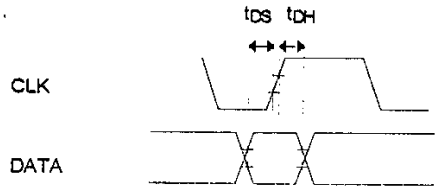
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit	Applicable pins
High input voltage	VIH	—	0.8VDD	—	—	V	Input pins
Low input voltage	VIL	—	—	—	0.2VDD	V	Input pins
Input leak (1)	ILK1	VI=VDD/GND	—	—	1/-1	μA	CE,CLK
Input leak (2)	ILK2	VI=VDD/GND	—	—	10/-10	μA	DATA
Low output voltage (1)	VOL1	Io=1mA	—	—	0.2VDD	V	DATA
High output voltage	VOH	Io=−400μA	0.8VDD	—	—	V	DATA
Low output voltage (2)	VOL2	DATA=1mA	—	—	0.2VDD	V	STD.P
OFF leak current	IOFLK	VI=VDD/0V	—	—	10	μA	STD.P
Current consumption (1)	IDD1	VDD=5V,VI(CE)=0V	—	10	20	μA	VDD
Current consumption (2)	IDD2	VDD=3V,VI(CE)=0V	—	2.5	5.0	μA	VDD
Current consumption (3)	IDD3	VDD=2V,VI(CE)=0V	—	1	2.0	μA	VDD

5. AC (Pulse) Ratings (V_{DD}=2.7 to 5.5V, Ta=-40 to 85°C)

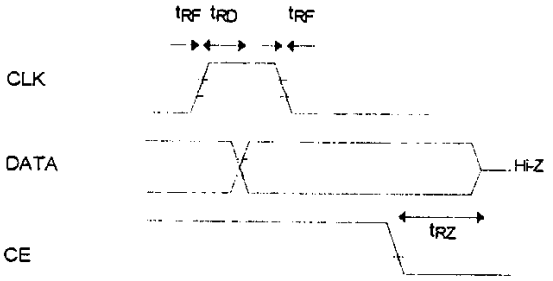
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CLK H pulse width	t_{WH}	—	300	—	—	ns
CLK L pulse width	t_{WL}	—	300	—	—	ns
CE setup time	t_{CS}	—	150	—	—	ns
CE hold time	t_{CH}	—	200	—	—	ns
CE recovery time	t_{CR}	—	300	—	—	ns
CLK setup time	t_{CKS}	—	20	—	—	ns
CLK hold time	t_{CKH}	—	20	—	—	ns
Write data setup time	t_{DS}	—	50	—	—	ns
Write data hold time	t_{DH}	—	50	—	—	ns
Read data delay time	t_{RD}	CL=50pF	—	—	250	ns
Output disable delay time	t_{RZ}	—	—	—	100	ns
Input rise time/fall time	t_{RF}	—	—	—	20	ns



WRITE MODE



READ MODE



Registers

1. Register Table

Address	Register name	D3 (MSB)	D2	D1	D0 (LSB)	Count range	Remarks
0	S_1	s8	s4	s2	s1	0~9	1-second digit register
1	S_{10}	fo	s40	s20	s10	0~5	10-second digit register
2	MI_1	mi8	mi4	mi2	mi1	0~9	1-minute digit register
3	MI_{10}	fr	mi40	mi20	mi10	0~5	10-minute digit register
4	H_1	h8	h4	h2	h1	0~9	1-hour digit register
5	H_{10}	fr	PM/AM	h20	h10	0~1,2	10-hour digit register
6	D_1	d8	d4	d2	d1	0~9	1-day digit register
7	D_{10}	fr	*	d20	d10	0~3	10-day digit register
8	MO_1	mo8	mo4	mo2	mo1	0~9	1-month digit register
9	MO_{10}	fr	*	*	mo10	0~1	10-month digit register
A	Y_1	0 y8	0 y4	1 y2	0 y1	0~9	1-year digit register
B	Y_{10}	y80	y40	y20	y10	0~9	v10-year digit register
C	W	fr	w4	w2	w1	0~6	Day-of-the-week register
D	C_D	30ADJ.	IRQ-F	CAL/HW	HOLD	–	Control register D
E	C_E	t1	t0	INT/STND	MASK	–	Control register E
F	C_F	TEST	24/12	STOP	RESET	–	Control register F

= 1992

- The relation between register bit 0/1 and input/output is positive logic. 0 = Low; 1 = High.
- The count is in BCD code. For example, if the 1-year digit register (Y1) is (y8, y4, y2, y1) = (0,0,1,0), the register indicates the "2" of "1992".
- Bits marked with * can be freely written to and used as RAM.
- A write instruction for the IRQ-F bit is not executed. This bit is set to "1" when the digit increment specified by t1,t0 is executed. The setting is maintained until the CD register has been read, and then returns to "0".
- The fo (OSC FLAG) bit records any oscillation interruption. It is used to monitor for low battery voltage. The bit can be cleared by setting it to "0". (Setting the bit externally to "1" is also possible.)
- The fr (READ FLAG) bit is set to "0" when the CE input becomes Low. If the 1-second digit register has been incremented while CE is High, the bit becomes "1". This allows testing for a second-increment while the clock register is being used. If the bit is "1", the clock register must be read again.
- The PM/AM bit is "1" for PM and "0" for AM.

2. Register Description

2.1 Clock/Calendar Register

(S1,S10,MI1,MI10,H1,H10,D1,D10,MO1,MO10,Y1,Y10,W)

- The register abbreviations stand for Second1, Second10, Minute1, Minute10, Hour1, Hour10, Day1, Day10, Month1, Month10, Year1, Year10, and Weekday. The notation is in BCD code, using numeric weighting.

- The registers are positive-logic registers. For example, (S8,S4,S2,S1) = 1001 means "9 seconds". Bits marked with * in the register table can be freely written to and used as RAM.

- Do not set impossible values to prevent the possibility of clock malfunction.

- Relation between PM/AM,h_{20},h_{10}

a) 12-hour notation

Possible time settings are 12 a.m. to 11 a.m., and 12 p.m. to 11 p.m.
The h20 bit cannot be written and is fixed to "0".
The clock does not increment the h20 bit.

24-hour notation

Possible time settings are 0 to 23.
A write attempt to the PM/AM bit is disregarded, and the bit will always read "0".

- Y_1,Y_{10} and leap years

Automatic leap year compensation is provided for the Gregorian calender and for Japanese-era years of the current era (Heisei). If an impossible date below 31 has been set for the day of the month, the settings as shown in the example below will be established as soon as the day-of-the-month increment pulse is generated.

Examples

Setting: February 29, 1993 ↓ November 31 ↓

Correction: March 1, 1993 December 1

- W register

For this register, count-up from 0 to 6 is performed. The table below shows an example for bit weighting.

W4	W2	W1	Day of the week
0	0	0	Monday
0	0	1	Tuesday
0	1	0	Wednesday
0	1	1	Thursday
1	0	0	Friday
1	0	1	Saturday
1	1	0	Sunday

- fo flag

This bit records any oscillation interruption. It is used to monitor for low battery voltage. "1" means oscillation interruption. The bit can be cleared by setting it to "0". It is also possible to externally set the bit to "1", but this should be avoided.

- fr flag

This bit indicates an incrementation while the CE input is High. When the bit becomes "1", the seconds have been incremented, which means that the clock register must be read again. The bit is cleared when CE becomes Low.

2.2 Control Registers

●CD register

Address	Register	D3	D2	D1	D0	
D	CD	30ADJ.	IRQ-F	CAL/HW	HOLD	Control register D

· 30-second ADJ (30-second adjustment) bit

When this bit is written to, the seconds are reset to 00 of the current minute if currently less than 30, or to 00 of next minute if currently 30 or more. For 125 microseconds after writing this bit, the bit is held at "1" and the inte registers S1 through W cannot be written to. After this interval, the bit is automatically reset to "0". Confirm that bit has reverted to "0" before attempting to write to the internal registers S1 through W.

Note that if "1" is written to the RESET bit before the 30-second ADJ bit has reverted to "0", 30-sec adjustment is not performed, and the 30-second ADJ bit is cleared to "0".

· IRQ-F

With the increment timing of the t1, t0 combination, i.e. the CE register bit, the IRQ-F bit is set to "1", and the STI output changes to Low. If this occurs when the INT/STND bit is "1", the setting is maintained until the CD regis reading is completed. Then the IRQ-F bit is reset to "0" and the STD.P output is set to high impedance. If the abc event occurs when the INT/STND bit is "0", the IRQ-F bit is reset to "0" and the STD.P output is set to h impedance after CD register reading is completed or after approx. 7.8 ms have elapsed.

The combination of t1, t0 determines four increment possibilities: 64 Hz/1 second/1 minute/1 hour.

· CAL/HW

When this bit is "1": clock range is seconds to 10 years, and weekdays

When this bit is "0": clock range is seconds to 10 hours, and weekdays

When the bit is "0", the six registers D1 to Y10 can be used as 4-bit RAM. The bits marked with * and the fr flag the D10 and MO10 registers can also be used separately as RAM.

· HOLD

This bit stops the 1-second digit incrementation. The clock continues to run, and the first incrementation after HOI was set to "1" is compensated for when the hold condition is released (+1 second). The bit is cleared by writing "0".

●CE register

Address	Register	D3	D2	D1	D0	
E	CE	t1	to	INT/STND	MASK	Control register E

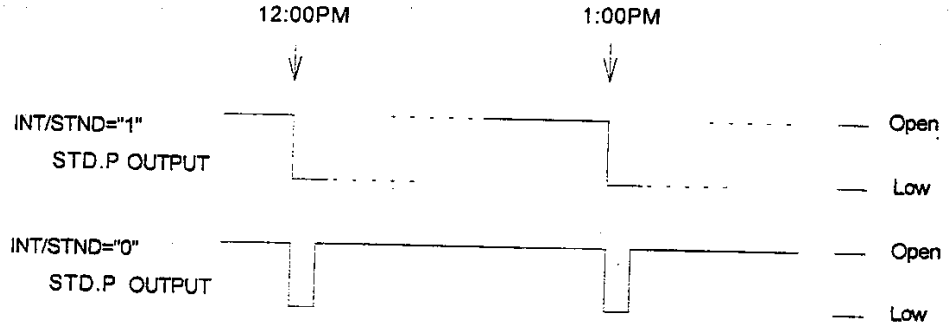
• t1,to

Set the timing of the interrupt cycle mode or fixed-period waveform mode.

t1	to	Period
0	0	1/64 s
0	1	1 second
1	0	1 minute
1	1	1 hour

INT/STND bit = "1": interrupt cycle mode
INT/STND bit = "0": fixed-period cycle mode

Example t1="1",to="1",MASK="0"

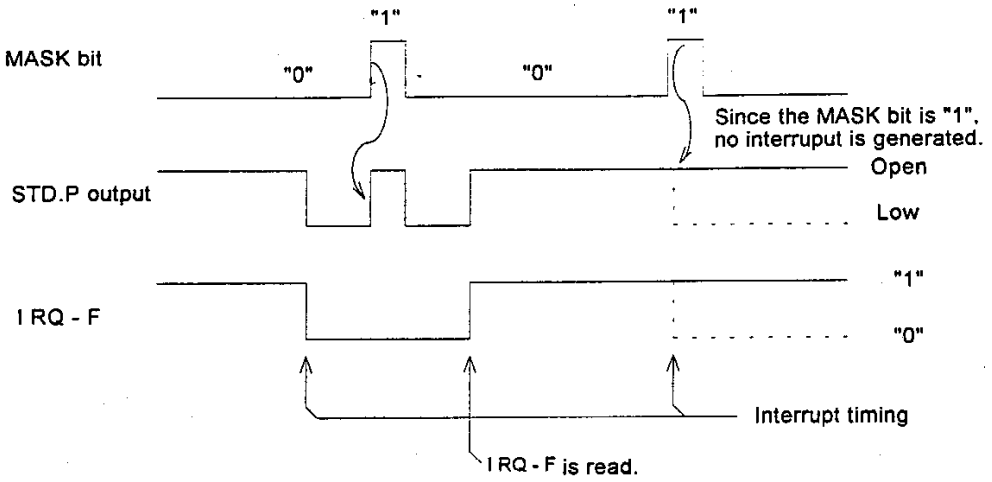


The fixed-period Low level cycle is 7.8 ms.
Because the 30-second adjustment could cause an incrementation, at the setting (t1,t0) = (1,0), (1,1) the STD.P output can become Low. If INT/STND = "0", the Low condition is maintained for up to 9.8 ms after the 30- second adjustment clear interval (after the 30-second ADJ flag has reverted to "0").
When the interrupt cycle is either 1 second, 1 minute, or 1 hour. If the HOLD bit is used to write S1 - MI10, and if there was an incrementation, the interrupt timing as determined by the incrementation is written to the S1 - MI10 registers and will cause the STD.P output to be Low after the hold condition is released (IRQ-F becomes "1").
Except for the above case, writing the S1 - H1 registers has no effect on the STD.P output.

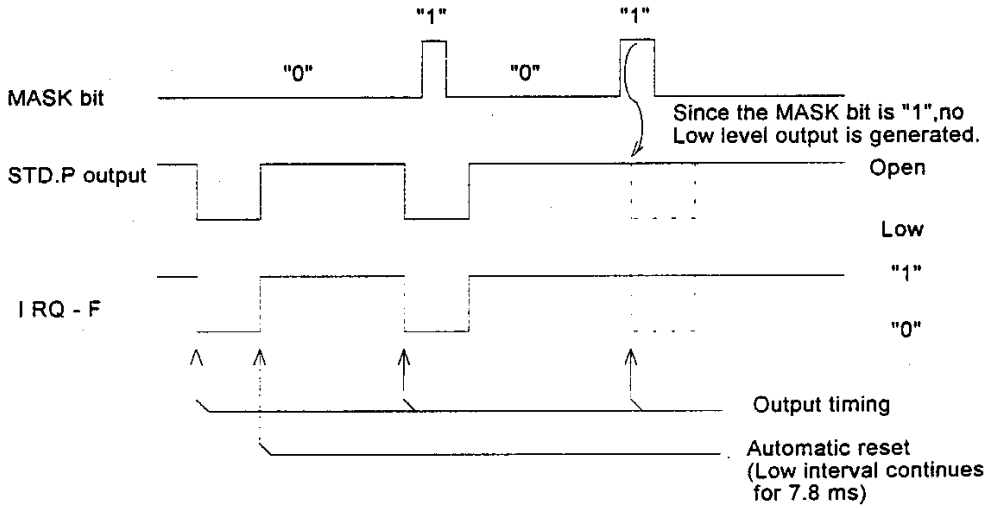
• INT/STND (interrupt/standard waveform) selection bit
When this bit is "1", the "1" status of the IRQ-F bit and the Low condition of the STD.P output are maintained until the IRQ-F (CD register) has been read.
When this bit is "0", the IRQ-F bit reverts to "0" after 7.8 ms or earlier if the IRQ-F bit is read before that. The Low level condition of the STD.P output reverts to high impedance after 7.8 ms.

• MASK
When this bit is "1", IRQ-F cannot be "1" and the STD.P output is open.

Interrupt cycle mode (INT/STND = 1)



Fixed-cycle mode (INT/STND = 0)



If the IRQ-F bit is read, the bit is reset to "0" at that point. The STD.P output becomes Low for 7.8 ms and then is open.

●CF register

Address	Register	D3	D2	D1	D0	
F	CF	TEST	24/12	STOP	RESET	Control register F

- TEST
  This test bit is used by Epson for internal purposes. It must be set to "0" by the user. The bit is cleared by setting CE to Low.

- 24/12
  Selection bit for 12-hour or 24-hour notation. "1" means 24-hour and "0" means 12-hour notation. When this bit is changed, data above H1 can become unstable and must be reset.

- STOP
  When this bit is set to "1", the clock stops. When the bit is set to "0", the clock resumes operation.

- RESET
  When this bit is set to "1", the seconds are reset to zero and the clock stops. The TEST bit is forced to "0". When the bit is set to "0", the clock resumes operation. When writing "0" to this bit, take care not to inadvertently set the TEST bit in the same register to "1".

■ Usage

●Function outline

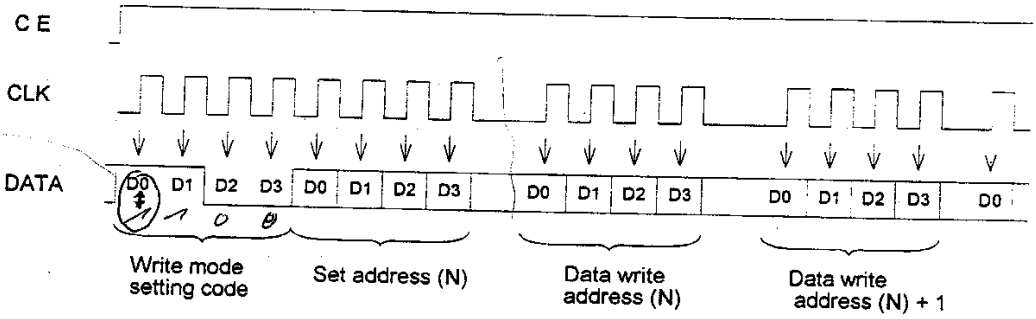
Read and write operations are carried out in 4-bit units after setting the CE input to High. If the CE input is set to Lo while a 4-bit input data block is incomplete, this input is disregarded. (Previous data remain valid.) Both read an write operations are performed in LSB-FIRST order.

[Write operation]

1)After setting the CE input to High, make the first 4-bit block "3" to indicate write mode, and use the next 4-bit block t specify the address.

2) The following 4-bit block is written to the specified address. Then the address is automatically incremented, an subsequent 4-bit blocks are written to subsequent addresses.

3)The address incrementation is cyclic. After address F has been written, the selection returns to address 0.

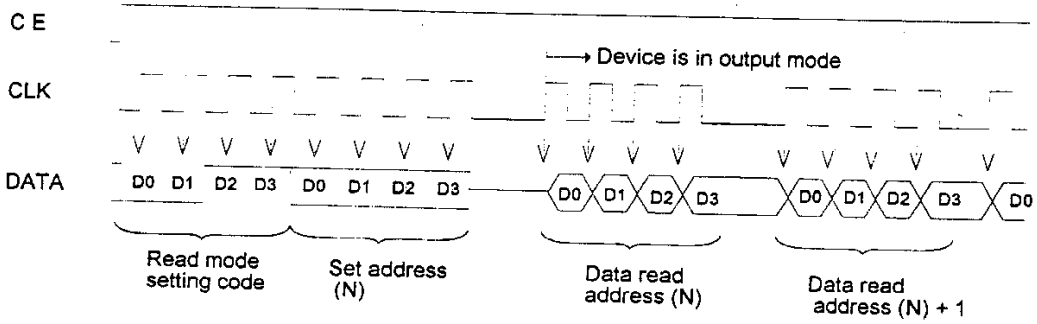


[Read operation]

1)After setting the CE input to High, make the first 4-bit block "C" to indicate read mode, and use the next 4-bit block tc specify the address.

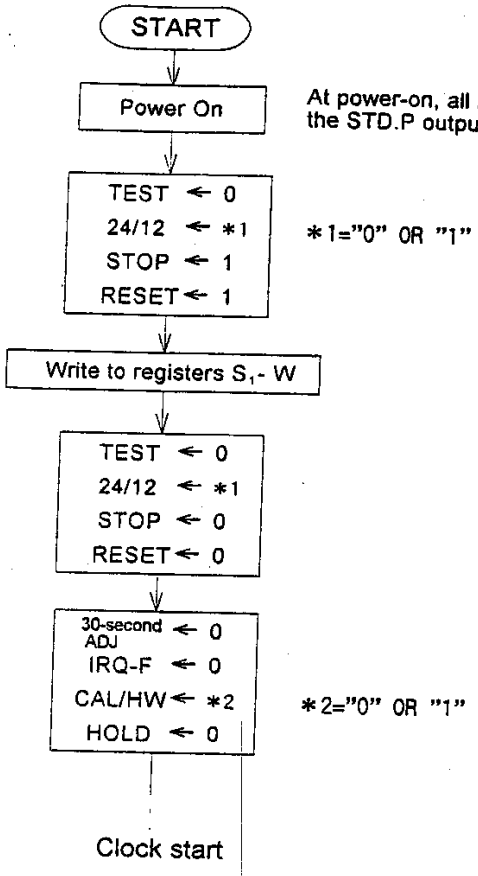
2)Read the 4-bit block in the specified address. Then the address is automatically incremented, and 4-bit blocks in subsequent addresses can be read.

3)The address incrementation is cyclic. After address F has been read, the selection returns to address 0.

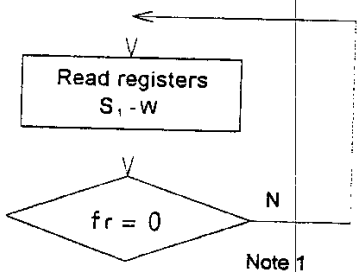


If the mode setting code is set to something other than "C" or "3", subsequent data are disregarded and the DATA port remains in the input mode.

●Power-on procedure



●Reading registers S1–W



Note 1

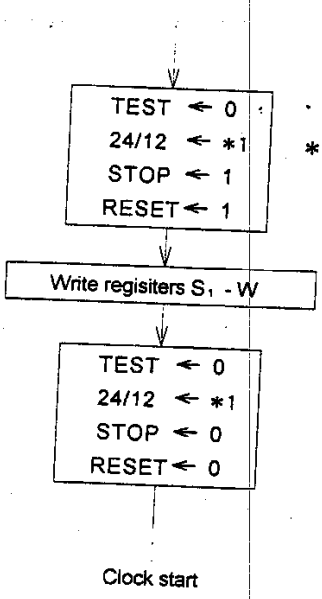
If C_D, C_E, C_F or registers S_1 - W are used as RAM, the data can be read without using fr

Note 2

It is sufficient to perform fr check for the last read digit only.

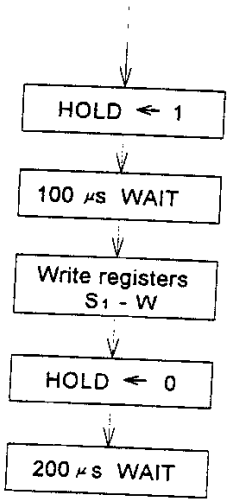
●Writing registers S1 - W

Method 1: No preservation of second data



*1="0" OR "1"

Method 2: Preservation of second data (for changeover to summer time)

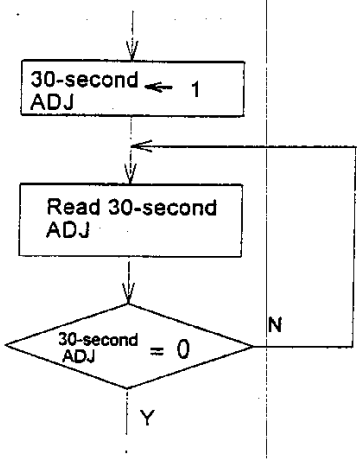


This procedure must be performed within 1 second.

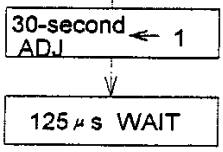
Otherwise the seconds are lost.

●Writing the 30-second ADJ bit

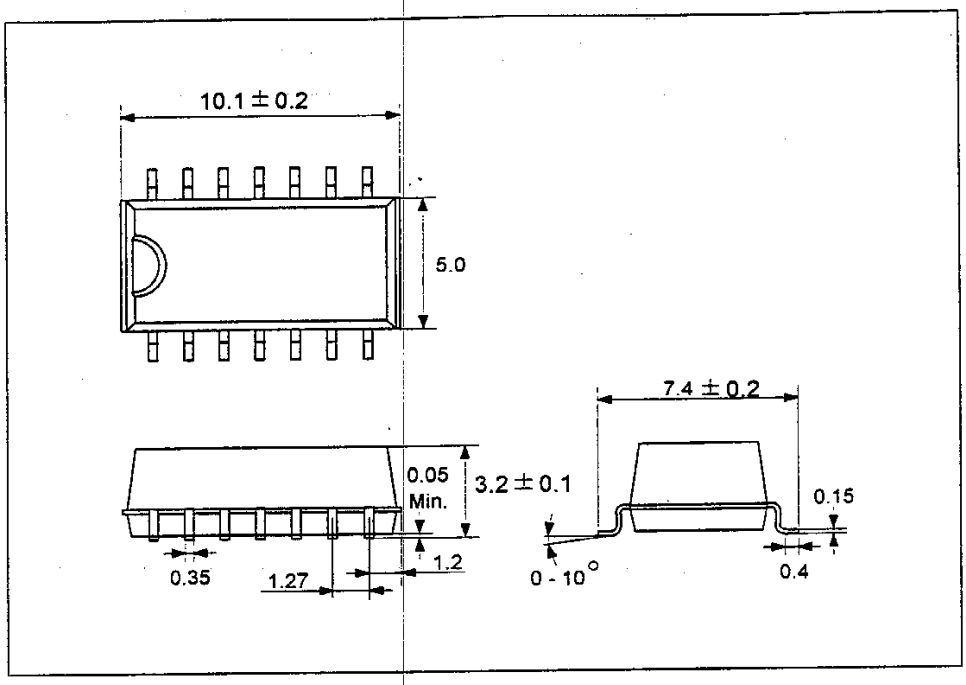
Method 1



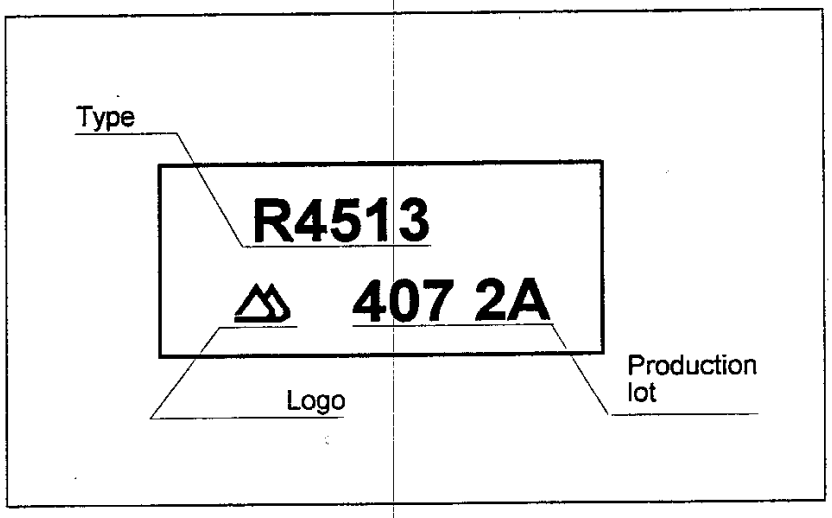
Method 2



External Dimensions



Marking Layout



Note:
The above illustration is a general representation of the content and positioning of information on the chip.
It is not a detailed specification of the actual typeface, size or positioning.

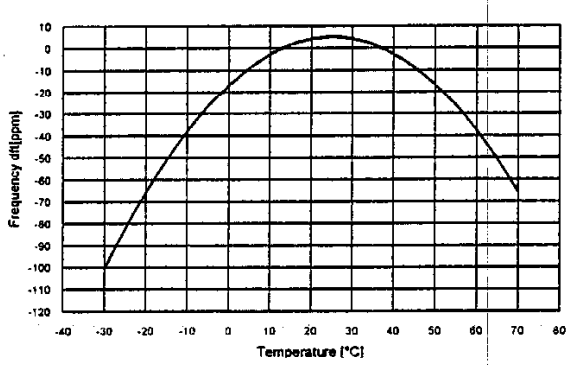
Reference data

(1) Temperature-dependent frequency deviation (typical)

θ_T = 25°C TYP.

α = -0.035ppm/°C^2

TYP.



Determining the frequency stability (clock accuracy)

1. The temperature-dependent frequency deviation can be approximated according to the following equation.

$$\Delta f_T(ppm) = \alpha (\theta_T - \theta_X)^2$$

Δf_T(ppm)	:	Frequency deviation at target temperature
α(ppm/°C^2)	:	Secondary temperature coefficient (-0.035 ±0.005ppm/ °C^2)
θ_T(°C)	:	Peak temperature (25°C±5°C)
θ_X(°C)	:	Target temperature

2. To determine the overall clock accuracy, add the temperature-dependent frequency deviation and the voltage-dependent frequency deviation.

$$\Delta f/f(ppm) = \Delta f/f_0 + \Delta f_T + \Delta f_V$$

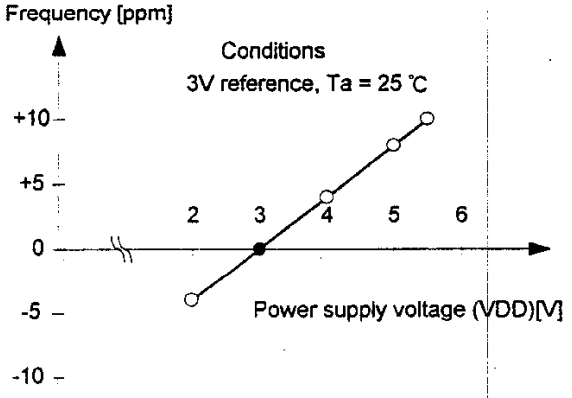
$\Delta f/f$ (ppm)	:	Clock accuracy at target temperature and target voltage (frequency stability)
$\Delta f/f_0$(ppm)	:	Frequency tolerance
Δf_T (ppm)	:	Frequency deviation at target temperature
Δf_V (ppm)	:	Frequency deviation at target voltage

3. Determining the daily deviation

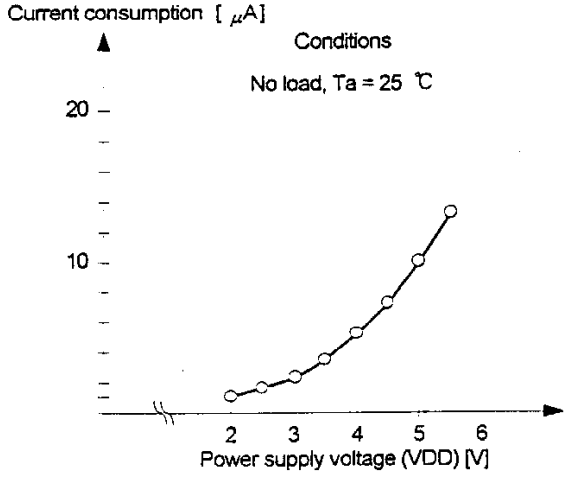
Daily deviation= $\Delta f/f \times 10^{-6} \times 86400$ (seconds)

At 11.574 ppm, the daily clock error is about one second per day.

(2) Voltage-dependent frequency deviation (typical)



(3) Current consumption vs. voltage (typical)



Note:

These data show average values for a sample lot.
For rated values, see the specifications on page 3.