MC74AC573, MC74ACT573

Octal Buffer/Line Driver with 3-State Outputs

The MC74AC573/74ACT573 is a high–speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable (OE) inputs.

The MC74AC573/74ACT573 is functionally identical to the MC74AC373/74ACT373 but has inputs and outputs on opposite sides.

- Inputs and Outputs on Opposite Sides of Package Allowing Easy Interface with Microprocessors
- Useful as Input or Output Port for Microprocessors
- Functionally Identical to MC74AC373/74ACT373
- 3–State Outputs for Bus Interfacing
- Outputs Source/Sink 24 mA
- ′ACT573 Has TTL Compatible Inputs

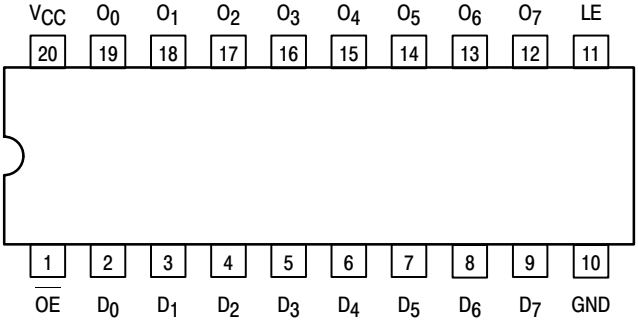


Figure 1. Pinout 20–Lead Packages Conductors
(Top View)

PIN ASSIGNMENT

PIN	FUNCTION
D_0–D_7	Data Inputs
LE	Latch Enable Input
OE	3–State Output Enable Input
O_0–O_7	3–State Latch Outputs

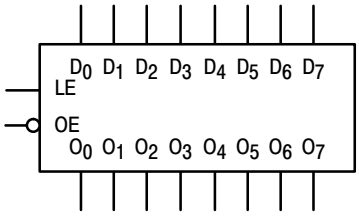
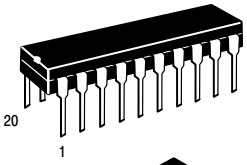


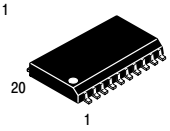
Figure 2. Logic Symbol

ON Semiconductor™

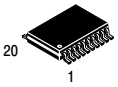
http://onsemi.com



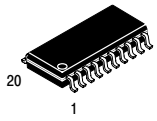
PDIP–20
N SUFFIX
CASE 738



SO–20
DW SUFFIX
CASE 751



TSSOP–20
DT SUFFIX
CASE 948E



EIAJ–20
M SUFFIX
CASE 967

ORDERING INFORMATION

Device	Package	Shipping
MC74AC573N	PDIP–20	18 Units/Rail
MC74ACT573N	PDIP–20	18 Units/Rail
MC74AC573DW	SOIC–20	38 Units/Rail
MC74AC573DWR2	SOIC–20	1000 Tape & Reel
MC74ACT573DW	SOIC–20	38 Units/Rail
MC74ACT573DWR2	SOIC–20	1000 Tape & Reel
MC74AC573DT	TSSOP–20	75 Units/Rail
MC74AC573DTR2	TSSOP–20	2500 Tape & Reel
MC74ACT573DT	TSSOP–20	75 Units/Rail
MC74ACT573DTR2	TSSOP–20	2500 Tape & Reel
MC74AC573M	EIAJ–20	40 Units/Rail
MC74AC573MEL	EIAJ–20	2000 Tape & Reel
MC74ACT573M	EIAJ–20	40 Units/Rail
MC74ACT573MEL	EIAJ–20	2000 Tape & Reel

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 8 of this data sheet.

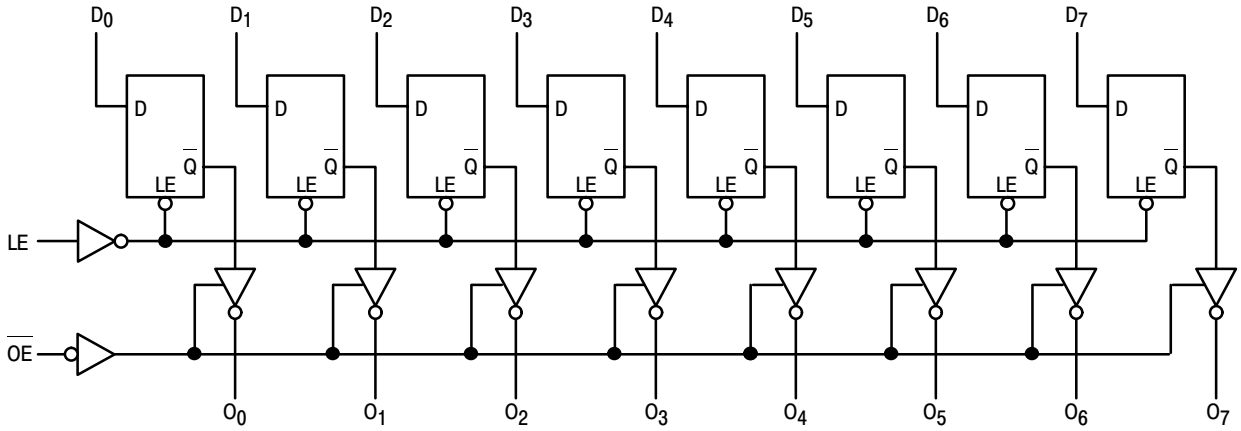
TRUTH TABLE

Inputs			Outputs
$\overline{OE}$	LE	D_n	O_n
L	H	H	H
L	H	L	H
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before LOW–to–HIGH Transition of Clock

FUNCTIONAL DESCRIPTION

The MC74AC573/74ACT574 contains eight D–type latches with 3–state output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH–to–LOW transition of LE. The 3–state buffers are controlled by the Output Enable ($\overline{OE}$) input. When OE is LOW, the buffers are enabled. When OE is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.



NOTE: That this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 3. Logic Diagram

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	–0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	–0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	–0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Sink/Source Current, per Pin	±50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	±50	mA
T_{stg}	Storage Temperature	–65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.