M74HC375P/FP/DP

DUAL 2-BIT TRANSPARENT LATCH

DESCRIPTION

The M74HC375 is a semiconductor integrated circuit consisting of four bistable latches with outputs Q and $\overline{Q}$.

FEATURES

- High-speed: 14ns typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 10μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

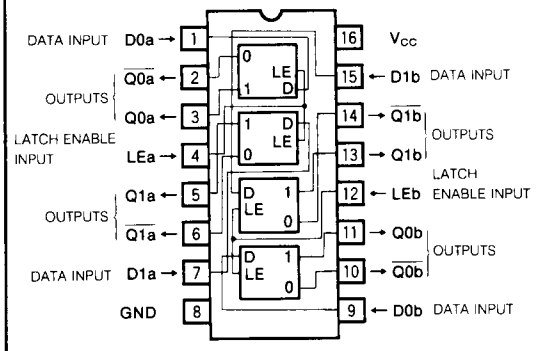
Use of silicon gate technology allows the M74HC375 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS375.

The use of buffered outputs improves the input-to output transfer characteristics and minimizes output impedance variations with respect to input voltage variations.

The M74HC375 has four D-type latches, and is provided with enable inputs LE common to two circuits each. When LE is high, the infromation from the data input D will appear in the outputs Q and $\overline{Q}$. When the D signal changes, the signal that appears in outputs Q and $\overline{Q}$ also will change. When LE changes from high to low, the status of D immediately before the change will be latched will LE is low, Q and $\overline{Q}$ will not change even if D changes.

A unit, the M74HC75, having the same functions and electrical characteristics as the M74HC375 is also available.

PIN CONFIGURATION (TOP VIEW)



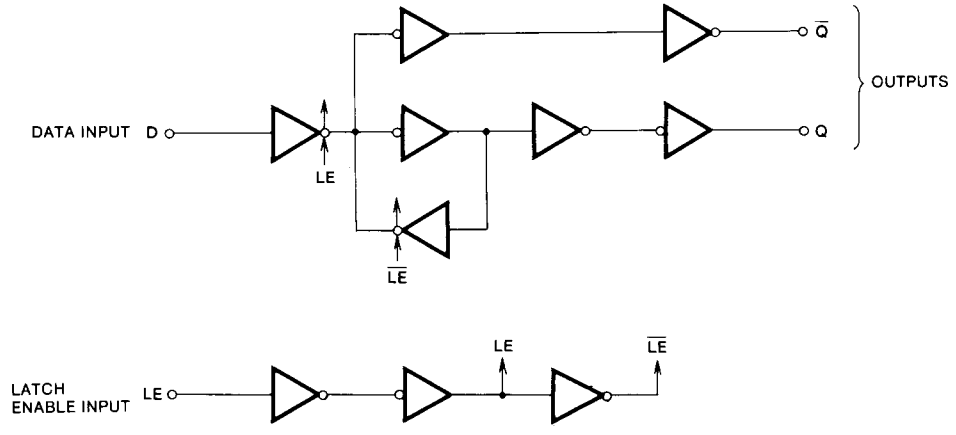
16P4
Outline 16P2N
16P2P

FUNCTION TABLE (Note 1)

Inputs		Outputs	
LE	D	Q	$\overline{Q}$
H	H	H	L
H	L	L	H
L	X	Q^0	$\overline{Q}^0$

Note 1 : Q^0, $\overline{Q}^0$: Output state Q, $\overline{Q}$ before input condition is set
X : Irrelevant

LOGIC DIAGRAM (EACH LATCH)



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC375FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC375DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Topr	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40∼+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level outnput voltage	V_I = V_{IH}, V_{IL} I_{OH} = −20μA	2.0	1.9			1.9		V
			4.5	4.4			4.4		
			6.0	5.9			5.9		
		I_{OH} = −4.0mA	4.5	4.18			4.13		
		I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level outnput voltage	V_I = V_{IH}, V_{IL} I_{OL} = 20μA	2.0			0.1		0.1	V
			4.5			0.1		0.1	
			6.0			0.1		0.1	
		I_{OL} = 4.0mA	4.5			0.26		0.33	
		I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA	6.0			2.0		20.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 15pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − Q)				23	ns
t_{PHL}					23	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − $\overline{Q}$)				20	ns
t_{PHL}					20	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (LE − Q)				27	ns
t_{PHL}					27	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (LE − $\overline{Q}$)				23	ns
t_{PHL}					23	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

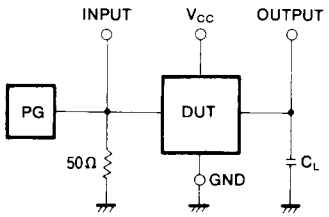
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − Q)		2.0			125		156	ns
			4.5			25		32	
			6.0			21		27	
t_{PHL}			2.0			125		156	ns
			4.5			25		32	
			6.0			21		27	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (D − $\overline{Q}$)		2.0			110		138	ns
			4.5			22		28	
			6.0			19		24	
t_{PHL}			2.0			110		138	ns
			4.5			22		28	
			6.0			19		24	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (LE − Q)		2.0			145		181	ns
			4.5			29		36	
			6.0			25		31	
t_{PHL}			2.0			145		181	ns
			4.5			29		36	
			6.0			25		31	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (LE − $\overline{Q}$)		2.0			125		156	ns
			4.5			25		31	
			6.0			22		28	
t_{PHL}			2.0			125		156	ns
			4.5			25		31	
			6.0			22		28	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 3)				66				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per latch)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

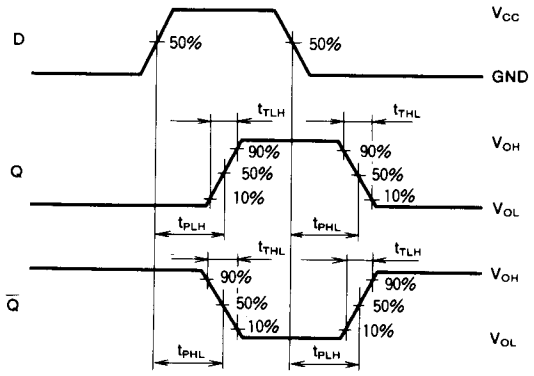
Symbol	Parameter	Test conditions	Limits					Unit
				25℃		−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	LE pulse width		2.0	80			100		ns
			4.5	16			20		
			6.0	14			18		
t_{su}	D setup time with respect to LE		2.0	100			125		ns
			4.5	20			25		
			6.0	17			21		
t_h	D hold time with respect to LE		2.0	5			5		ns
			4.5	5			5		
			6.0	5			5		

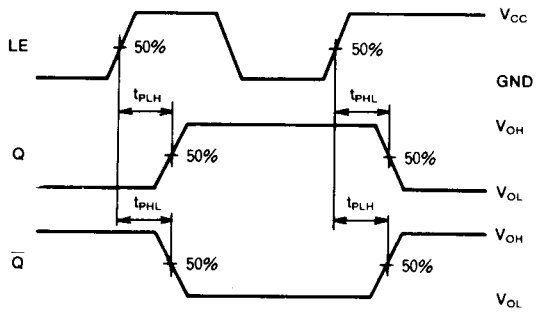
Note 4 : Test Circuit

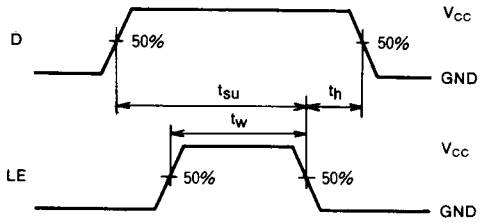


(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM







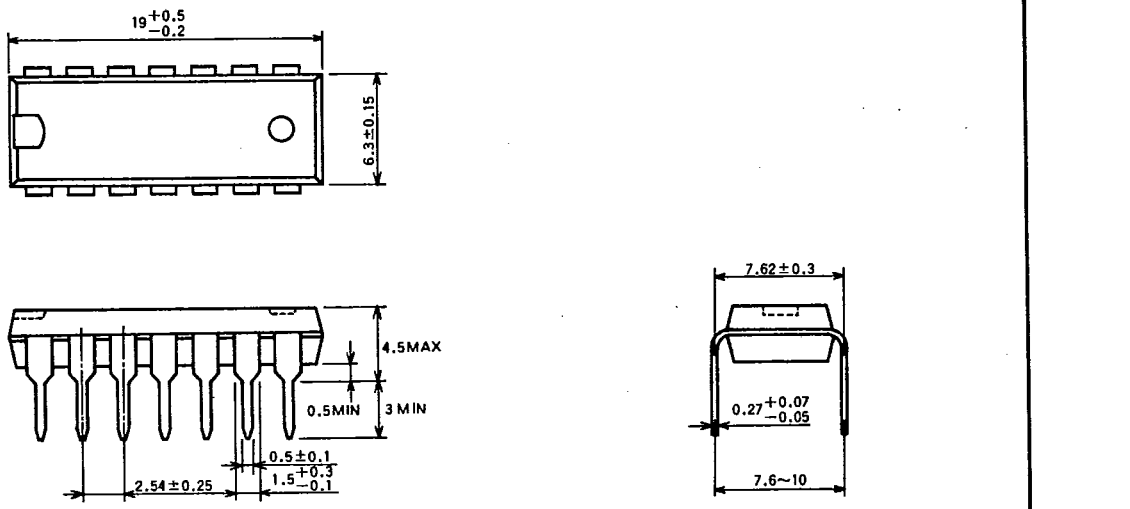
MITSUBISHI ELECTRIC

MITSUBISHI HIGH SPEED CMOS

PACKAGE OUTLINES

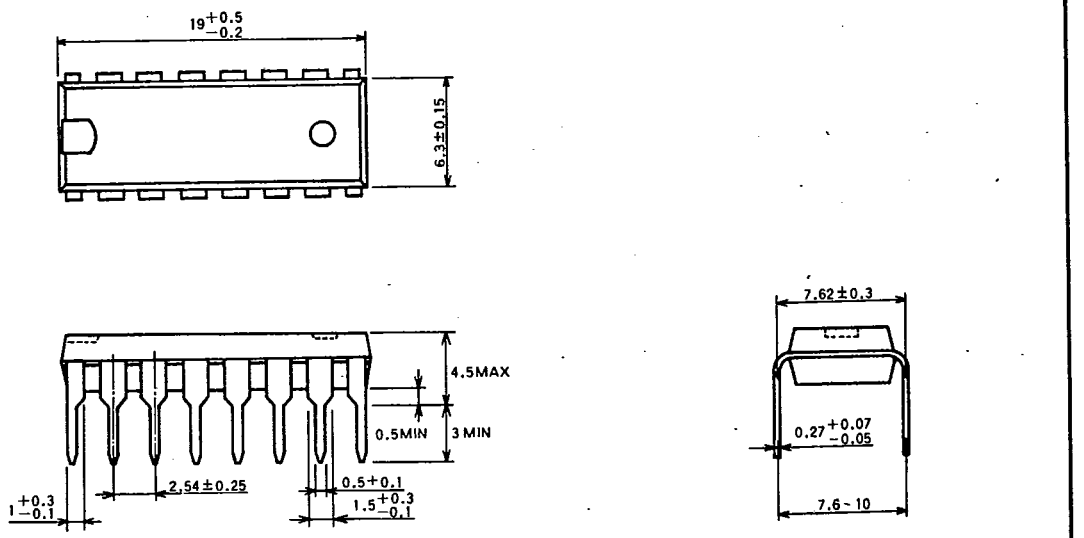
TYPE 14P4 14-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIP

Dimension in mm

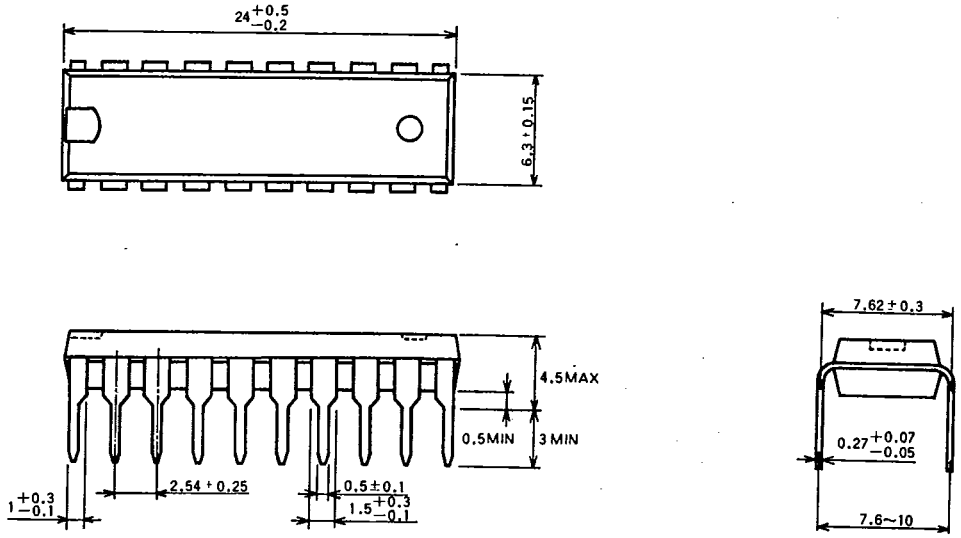


MITSUBISHI HIGH SPEED CMOS

PACKAGE OUTLINES

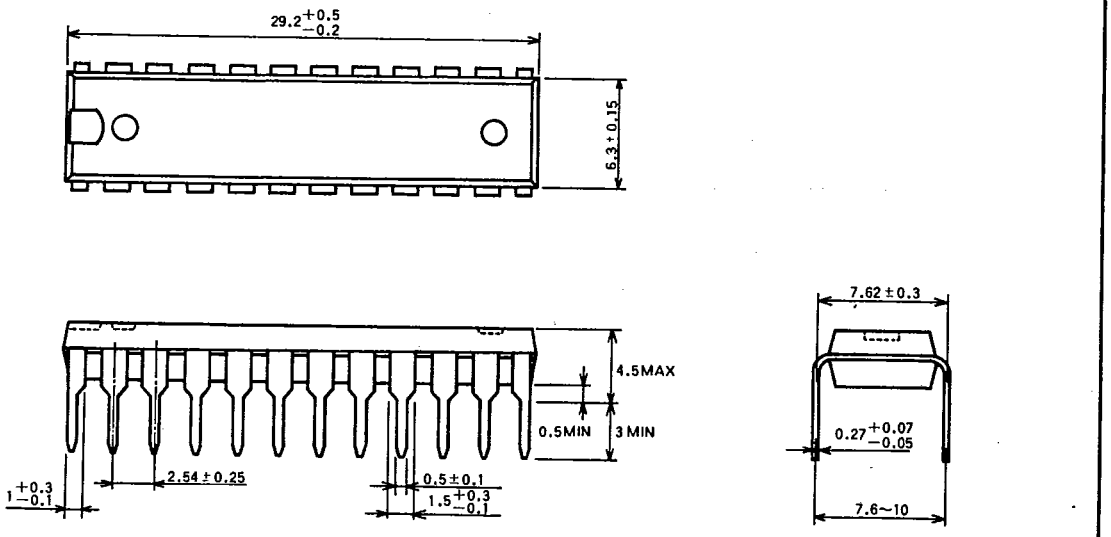
TYPE 20P4 20-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 24P4D 24-PIN MOLDED PLASTIC DIP

Dimension in mm



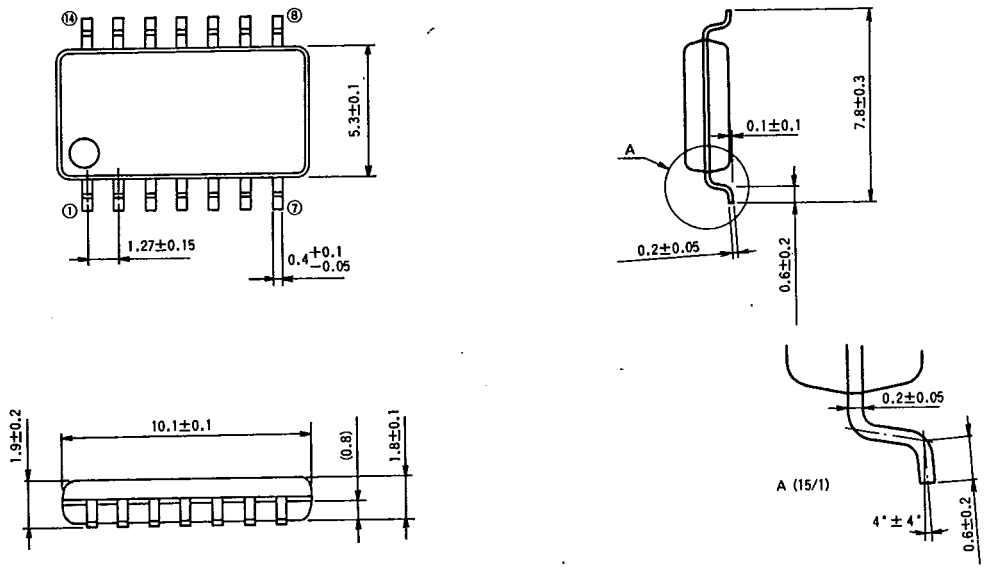
MITSUBISHI ELECTRIC

MITSUBISHI HIGH SPEED CMOS

PACKAGE OUTLINES

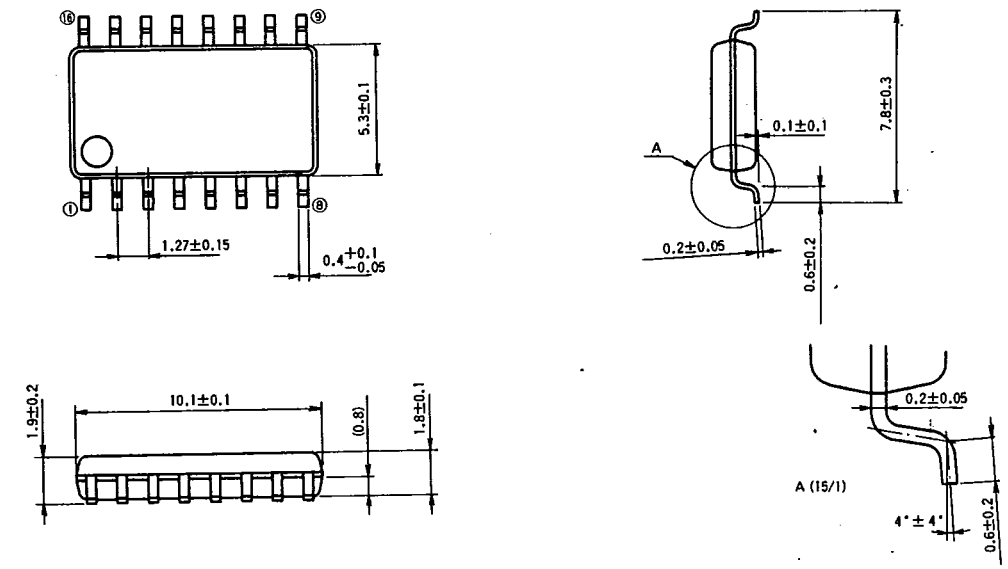
TYPE 14P2N 14PIN MOLDED PLASTIC SOP

Dimension in mm



TYPE 16P2N 16PIN MOLDED PLASTIC SOP

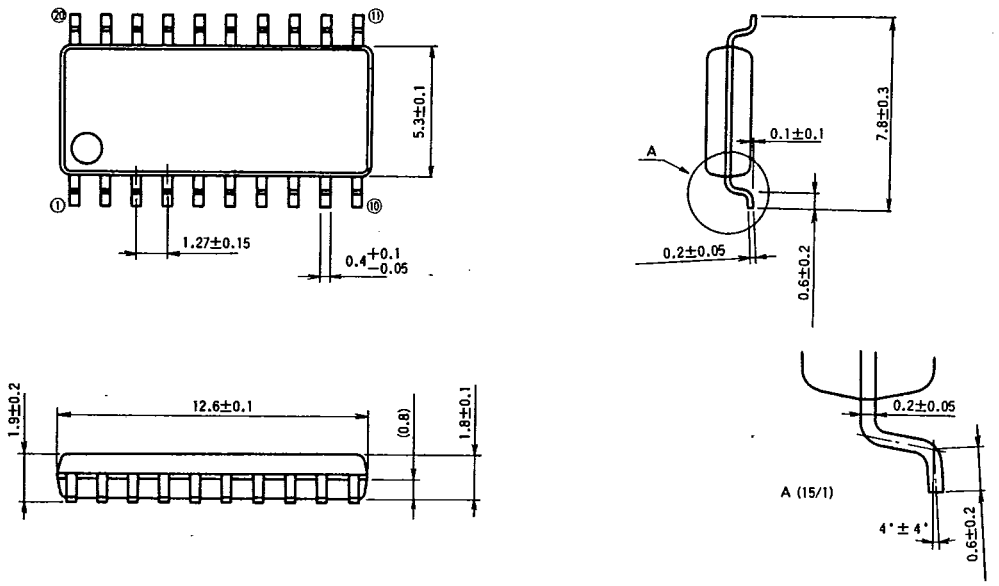
Dimension in mm



PACKAGE OUTLINES

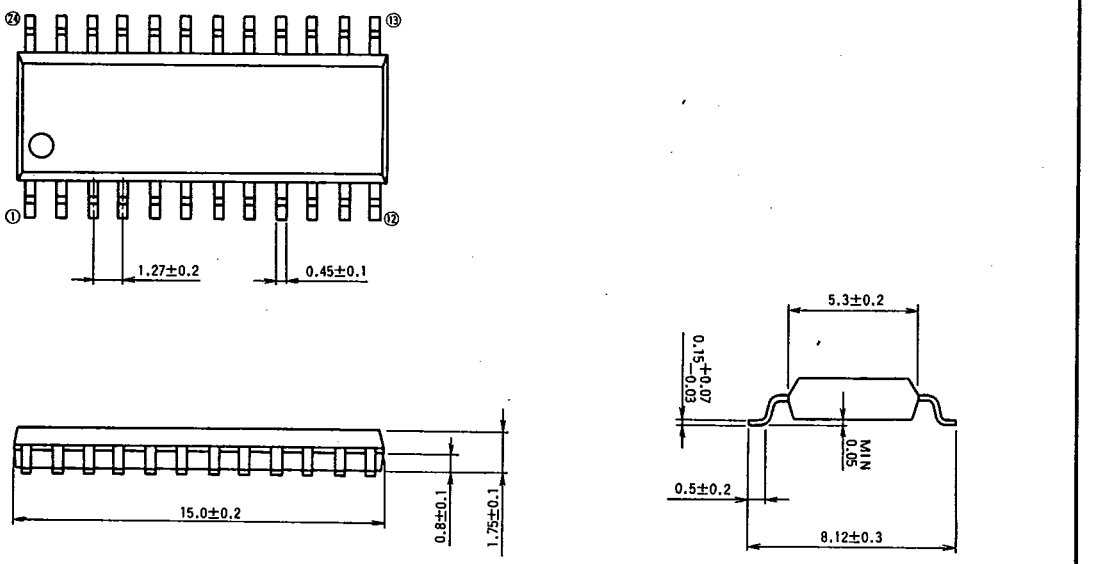
TYPE 20P2N 20PIN MOLDED PLASTIC SOP

Dimension in mm



TYPE 24P2 24PIN MOLDED PLASTIC SOP

Dimension in mm

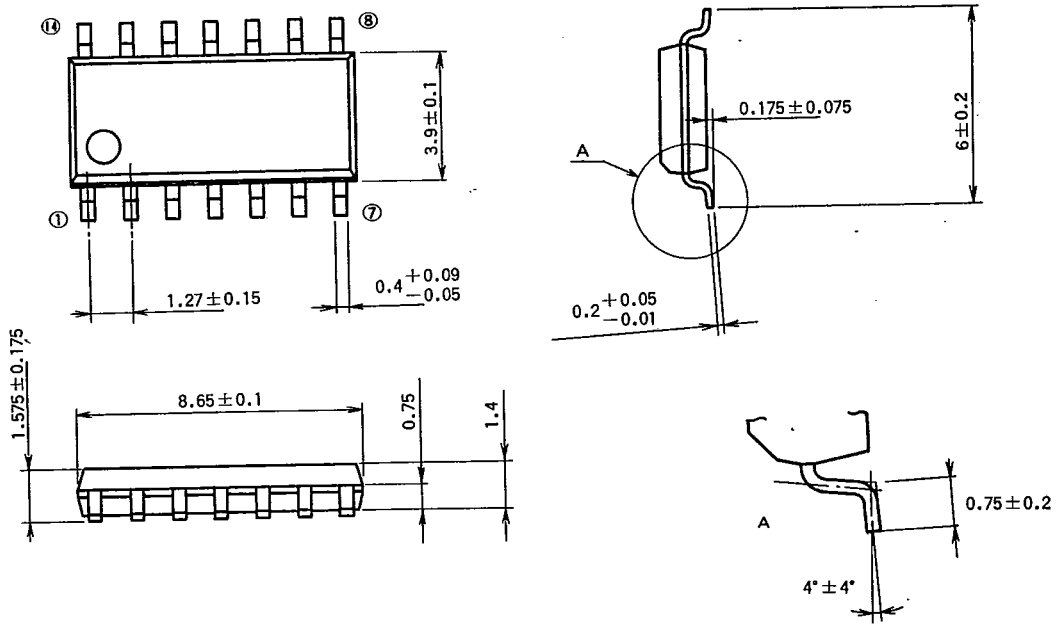


MITSUBISHI ELECTRIC

PACKAGE OUTLINES

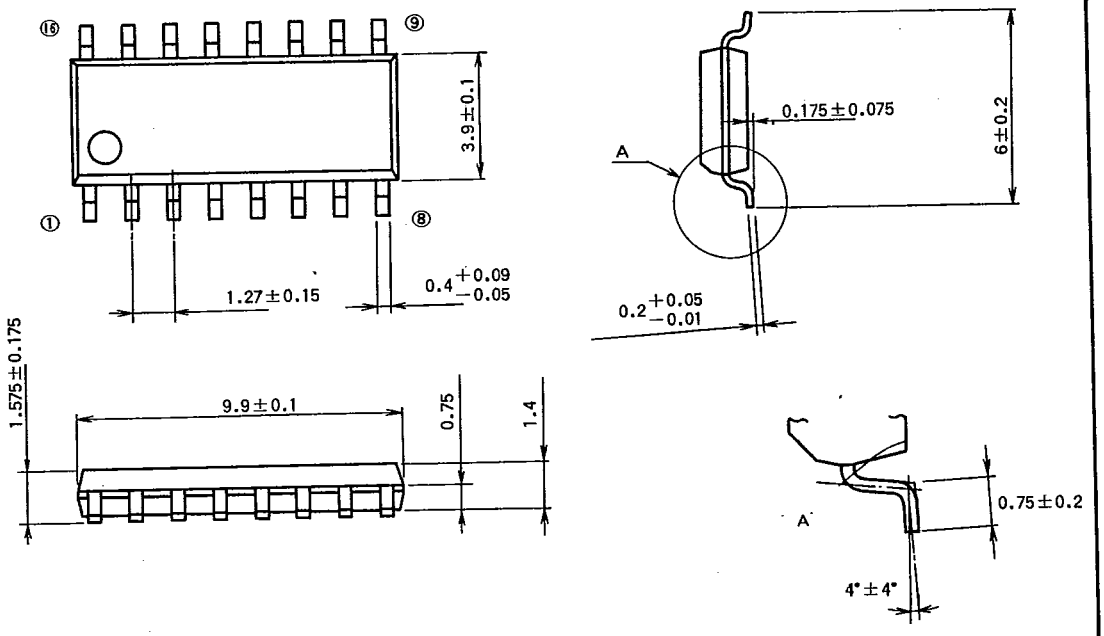
TYPE 14P2P 14-PIN MOLDED PLASTIC SOP(JEDEC 150mil body)

Dimension in mm

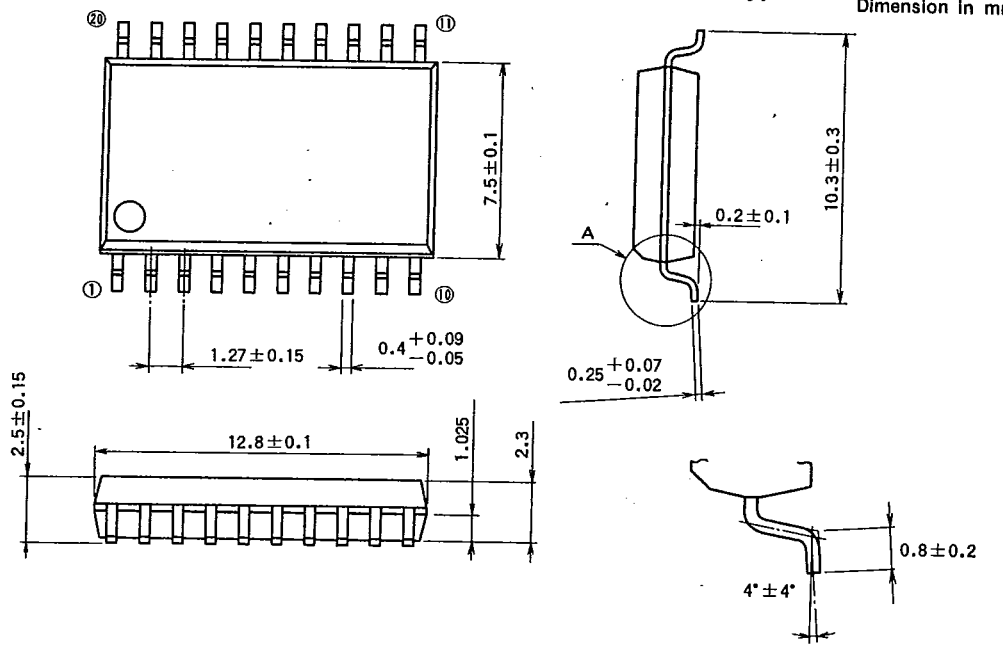


TYPE 16P2P 16-PIN MOLDED PLASTIC SOP(JEDEC 150mil body)

Dimension in mm



PACKAGE OUTLINES

TYPE 20P2V 20-PIN MOLDED PLASTIC SOP(JEDEC 300mil body)

Dimension in mm