NOVATEK
聯 詠 科 技

Data Sheet

NT39703-5

TFT LCD Timing Controller

V0.2

Preliminary Spec

Index

Revise History

NT39703-5 Specification Revision History			
Version	**Content**	**Page**	**Date**
0.2	Modify Features Rename 18 bit RGB timing table Modify Operating temperature	4 10 12	2007/06/08
0.1	New spec	-	2007/04/25

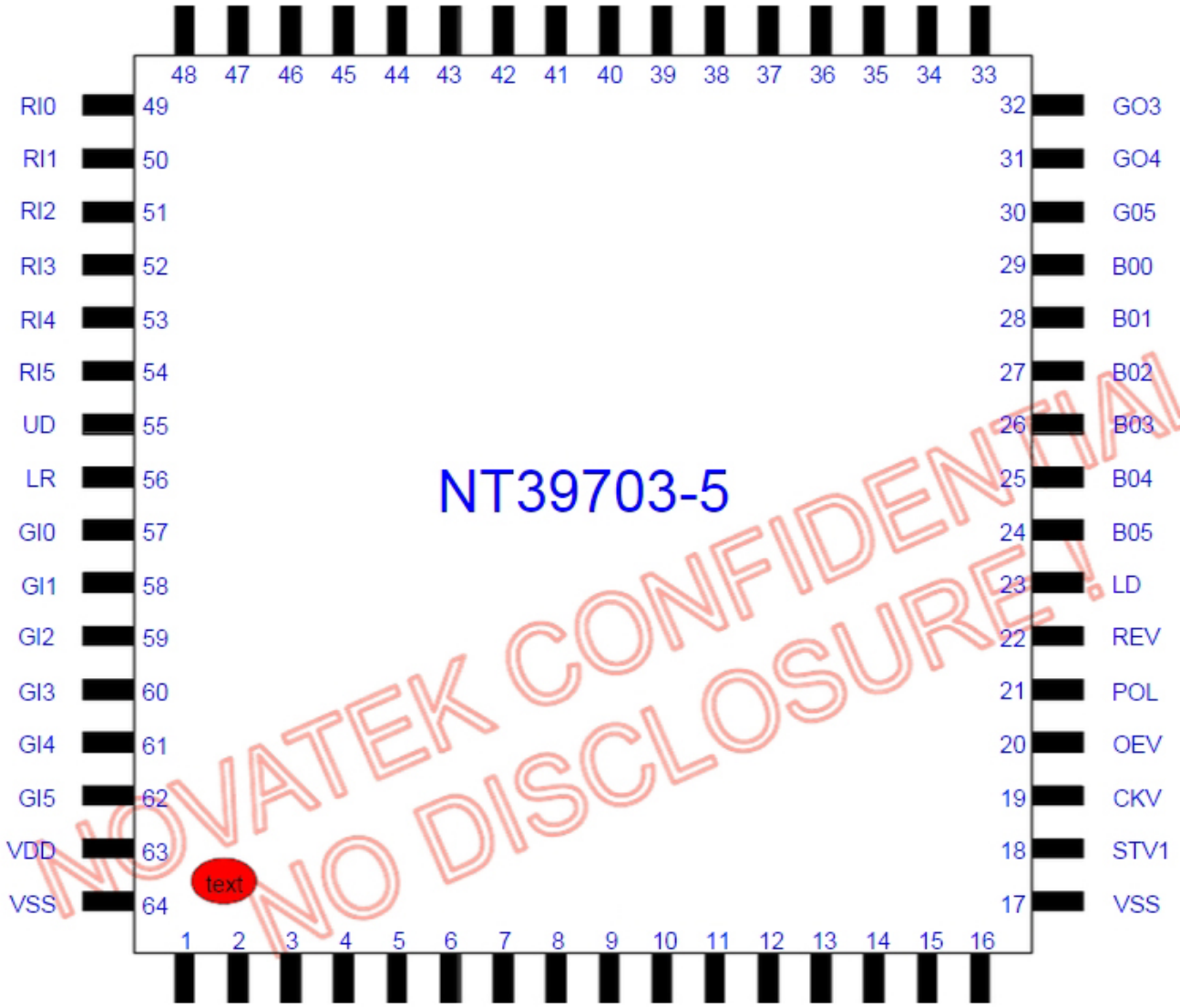
Features

- Support 3 different digital TFT-LCD panels
  - 800x600, 800x480, 640x480
- 18 bit RGB input signals
- Support HV mode and DE mode
- Build-in output data reverse function for better EMI
- Build-in 16 test pattern
- Support no_clock detection
- Provide source and gate drivers control timing
- Operating voltage : 2.7V~3.6V
- Master clock frequency: 71MHz
- 64 TQFP

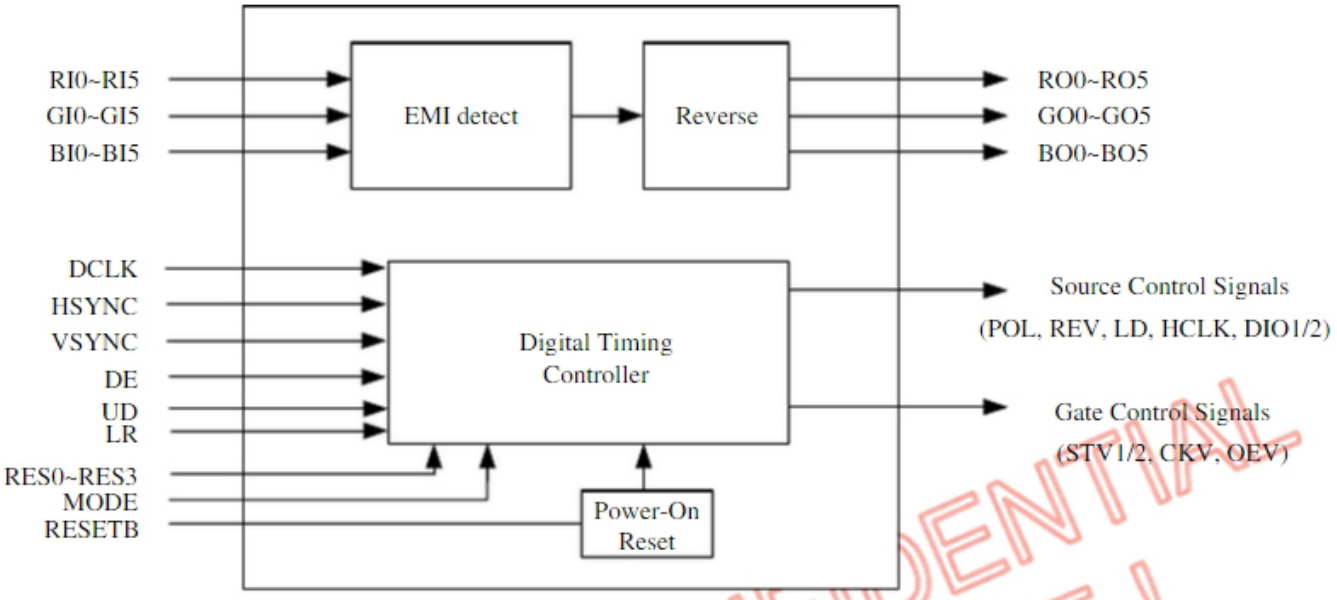
General Description

The NT39703-5 is a digital TFT-LCD timing controller with built-in 16 test pattern. The input signal is digital R/G/B with HSYNC/VSYNC or DE. User can use the MODE pin to select input signal to be either HV mode or DE mode. Outputs support REV function to reduce EMI. When system clock disable for 10us will trigger the no_clock detect function, and then output data will be forced to zero.

Pin Assignment



Function Block Diagram

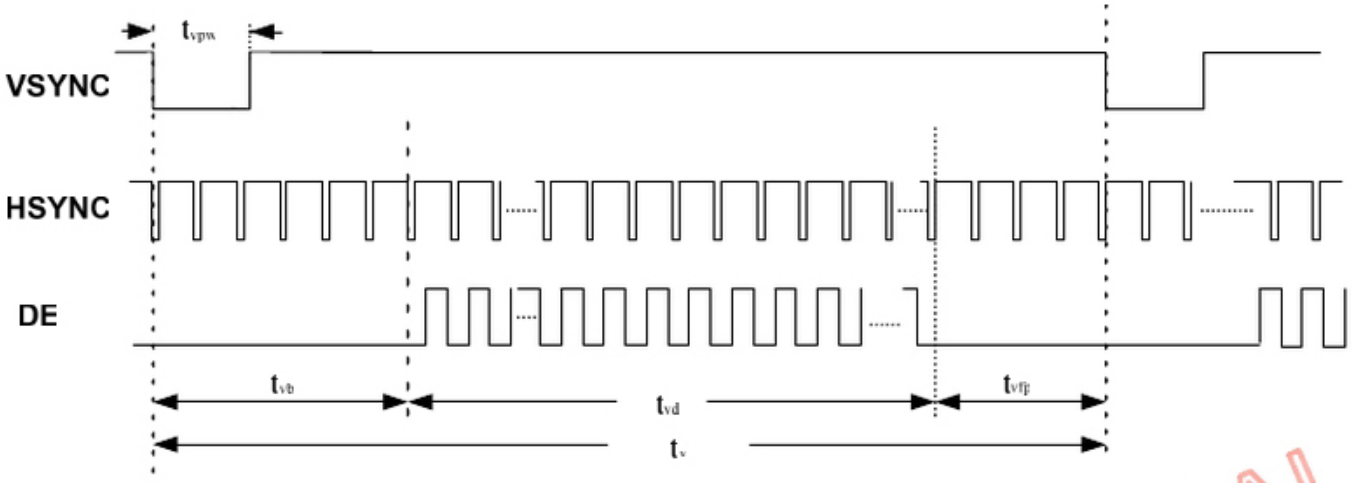


Pad Description

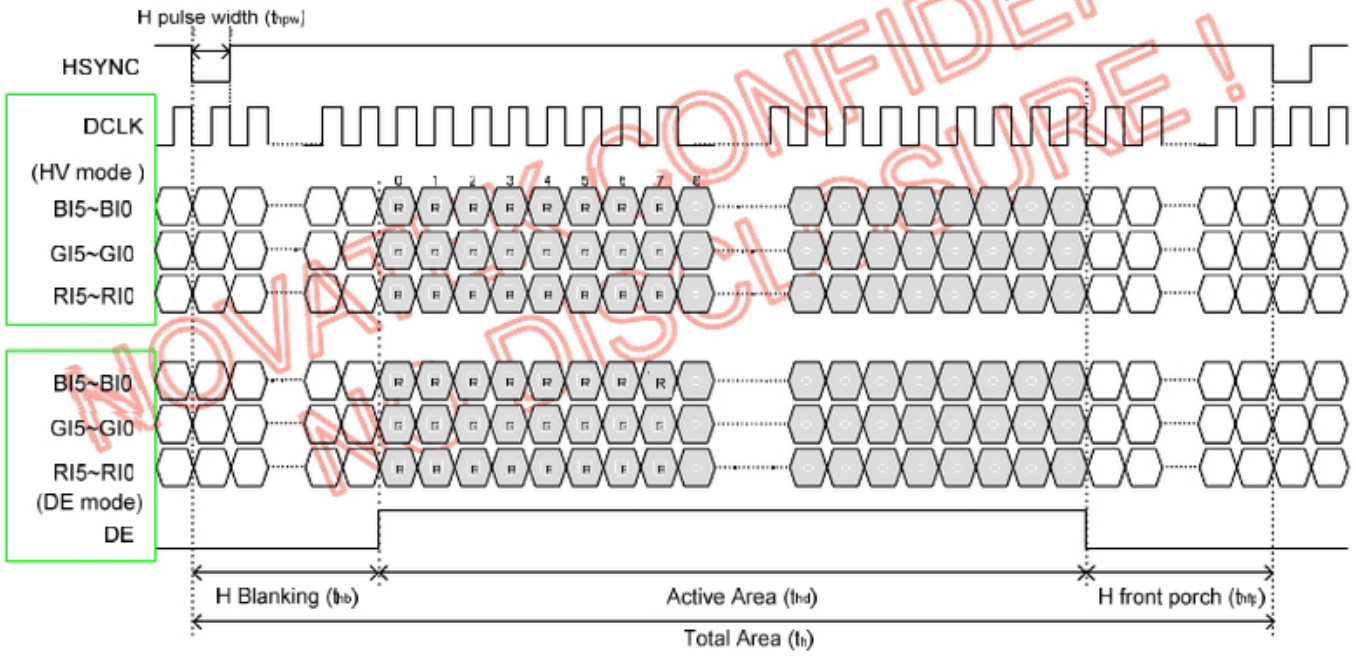
SYMBOL	Pin No	I/O	Description
RI5~RI0 GI5~GI0 BI5~BI0	54-49 62-57 8-3	I	6-bit data input.
DCLK	46	I	Clock signal; latch data at falling edge.
HSYNC	10	I	MODE = L : Horizontal sync input. Negative polarity. MODE = H : enable build-in test patterns when HSYNC = H. Normally pull low
VSYNC	11	I	Vertical sync input. Negative polarity. Normally pull low
DE	9	I	MODE = H : Data input enable. Active High to enable data input. MODE = L : enable build-in test patterns when DE = H. Normally pull low
MODE	12	I	DE / SYNC mode select. Normally pull high H : DE mode. L : SYNC mode.
RESETB	15	I	Hardware global reset. Low active. Normally pull high
UD	55	I	Up/Down control. Normally pull high UD = H : STV1 output , STV2 in HiZ state. UD = L : STV2 output , STV1 in HiZ state.
LR	56	I	Left/Right control. Normally pull high LR = H : DIO1 output , DIO2 in HiZ state. LR = L : DIO2 output , DIO1 in HiZ state.
RES0	14	I	Resolution selection. Normally pull low 1 : 800x600 and 800x480. 0 : 640x480.
RES2,RES3	2,13	I	Pull high in normal operation.
RO5~RO0 GO5~GO0 BO5~RO0	36-41 30-35 24-29	O	Data output.
HCLK	42	O	Source driver shift clock.
DIO1, DIO2	43,48	I/O	Source driver start pulse signal. Floating is inhibited
LD	23	O	Source driver latch pulse and output enable.
POL	21	O	Source driver polarity select.
REV	22	O	Controls whether the data are inverted or not. When “REV”=1 output data will be inverted. EX. “00” → “ 3F”, “07”→ “ 38”, “15”→ “2A”, and so on. Note: source driver with REV only
CKV	19	O	Gate driver clock scan clock.
STV1, STV2	18,47	I/O	Gate Driver start pulse signal. Floating is inhibited.
OEV	20	O	Output enable control of gate driver.
NC	1	N	Don’t care.
VDD	16,44,63	P	Power supply for digital circuits.
VSS	17,45,64	P	Ground pins for digital circuits

Input Data Format

1. Vertical input timing



2. Horizontal input timing



3. 18 bit RGB timing table

For 800x600/480 panel

Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		thd	800			DCLK
DCLK frequency		fclk	Min.	Typ.	Max.	
			32.5	35	40	MHz
1 Horizontal Line		th	862	1056	1100	DCLK
HSYNC pulse width	Min.	thpw	1			
	Typ.		1			
	Max.		1			
HSYNC blanking		thb	46	46	46	
HSYNC front porch		thfp	16	210	254	

Vertical input timing

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Vertical display area	tvd	600			H
VSYNC period time	tv	628	635	650	H
VSYNC pulse width	tvpw	1	1	1	H
VSYNC Blanking (tvb)	tvb	23	23	23	H
VSYNC Front porch (tvfp)	tvfp	5	12	27	H

For 640x480 panel

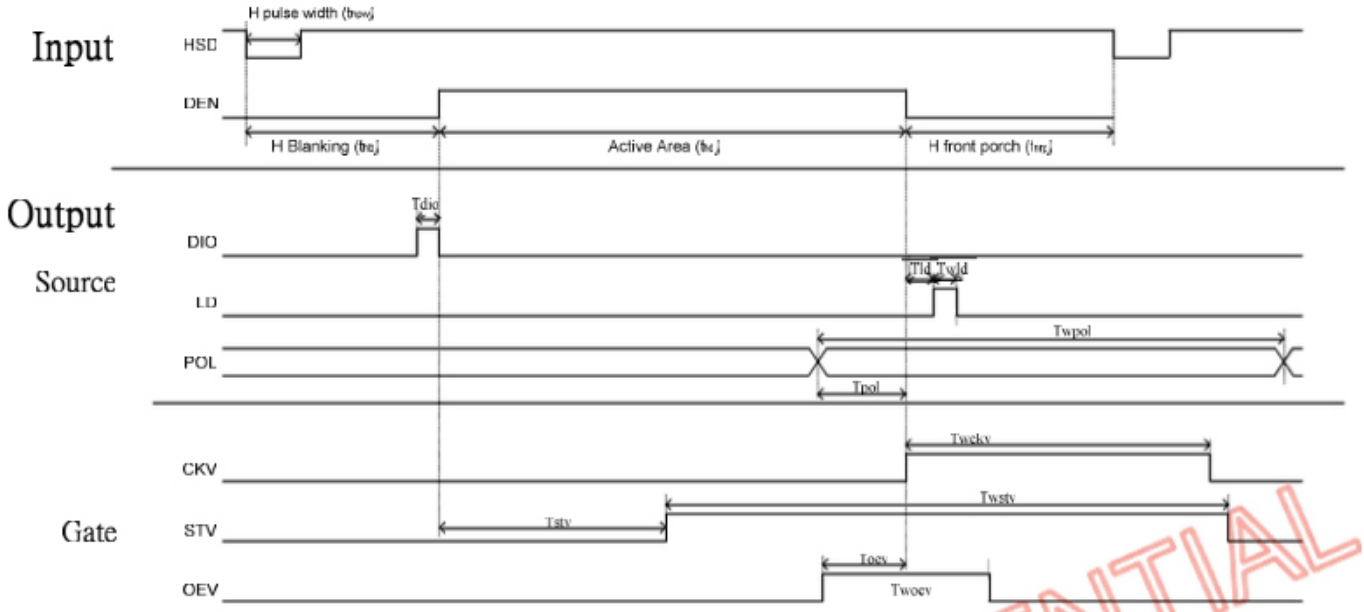
Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		thd	640			DCLK
DCLK frequency		fclk	Min.	Typ.	Max.	
			23	25	30	MHz
1 Horizontal Line		th	750	800	900	DCLK
HSYNC pulse width	Min.	thpw	1			
	Typ.		1			
	Max.		1			
HSYNC blanking		thb	46	46	46	
HSYNC front porch		thfp	64	114	214	

Vertical input timing

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Vertical display area	tvd	480			H
VSYNC period time	tv	515	525	560	H
VSYNC pulse width	tvpw	1	1	1	H
VSYNC Blanking (tvb)	tvb	34	34	34	H
VSYNC Front porch (tvfp)	tvfp	1	11	46	H

Output Data format



Parameter	Symbol	Value	Unit
Source			
Dio rising to first data	Tdio	1	DCLK
Last data to LD rising	Tld	12	DCLK
LD pulse width	Twld	4	DCLK
POL transition to last data	Tpol	1/16	H
POL cycle time	Twpol	1	H
Gate			
CKV pulse width	Twckv	0.5	H
First data to STV rising	Tstv	0.5	thd
STV pulse width	Twstv	1	H
OEV to last data	Toev	1/16	H
OEV pulse width	Twoev	1/8	H

Absolute Maximum Ratings

	MIN.	MAX.	UNIT
Logic supply voltage, VDD Digital input voltage Output voltage	-0.5	5	V

TEMPREATURE

	MIN.	MAX.	UNIT
Operating temperature	-20	85	°C
Storage temperature	-55	125	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or under any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(Test Condition VDD =3.3V , GND=0V, TA=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	VDD	2.7	3.3	3.6	V	Digital power: default 3.3V
Low Level Input Voltage	Vil	GND	-	0.2xVDD	V	Digital input pins
High Level Input Voltage	Vih	0.8xVDD	-	VDD	V	Digital input pins
Input Leakage Current	Ii	-	-	±1	uA	Digital input pins.
Pull-high Impedance	Rin	150k	200k	250k	ohm	Digital control input pins
Pull-low Impedance	Rin	150k	200k	250k	ohm	Digital control input pins
High Level Output Voltage	Voh	VDD-0.4	-	-	V	Digital output pins; Ioh= 4 mA
Low Level Output Voltage	Vol	GND	-	GND+0.4	V	Digital output pins; Iol= -4 mA
Digital Operating Current	Icc	-	5	-	mA	Resolution 800x480; DCLK = 32Mhz no load

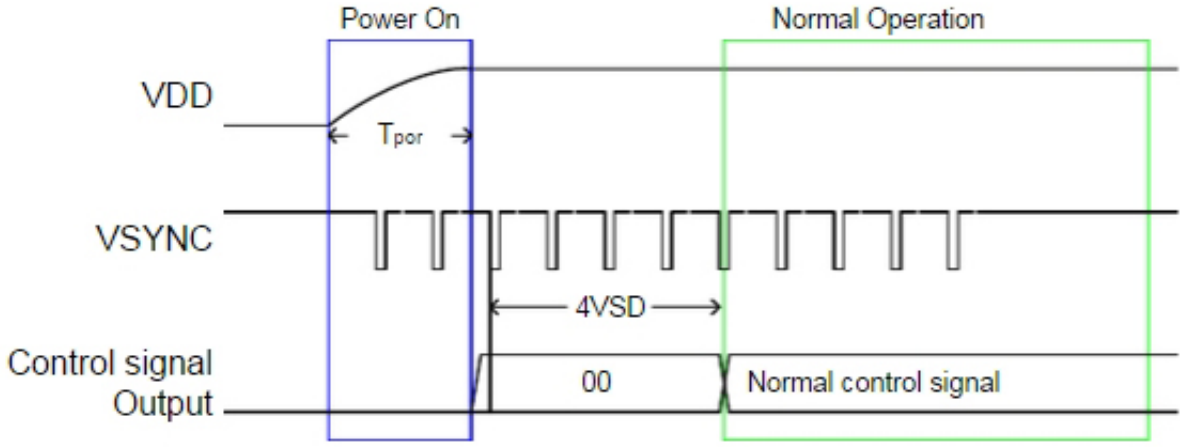
AC Electrical Characteristics

(VDD =3.3V , GND=PGND=0V, TA= 25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power on RESET time	Tpor	-	-	10	ms	VDD = 3.3V
RESET time	tRSTW	1	-	-	ms	VDD = 3.3V
DCLK cycle time	Tclk	14	-	200	ns	
DCLK pulse duty	Tcwh	40	50	60	%	
VSYNC setup time	Tvst	4	-	-	ns	
VSYNC hold time	Tvhd	4	-	-	ns	
HSYNC setup time	Thst	4	-	-	ns	
HSYNC hold time	Thhd	4	-	-	ns	
Data set-up time	Tdsu	4	-	-	ns	RI,GI,BI to DCLK
Data hold time	Tdhd	4	-	-	ns	RI,GI,BI to DCLK
DE setup time	Tesu	4	-	-	ns	
DE hold time	Tehd	4	-	-	ns	
HCLK cycle time	Tcph	1			Tclk	
Output data setup time	Tsu	5			ns	
Output data hold time	Thd	5			ns	

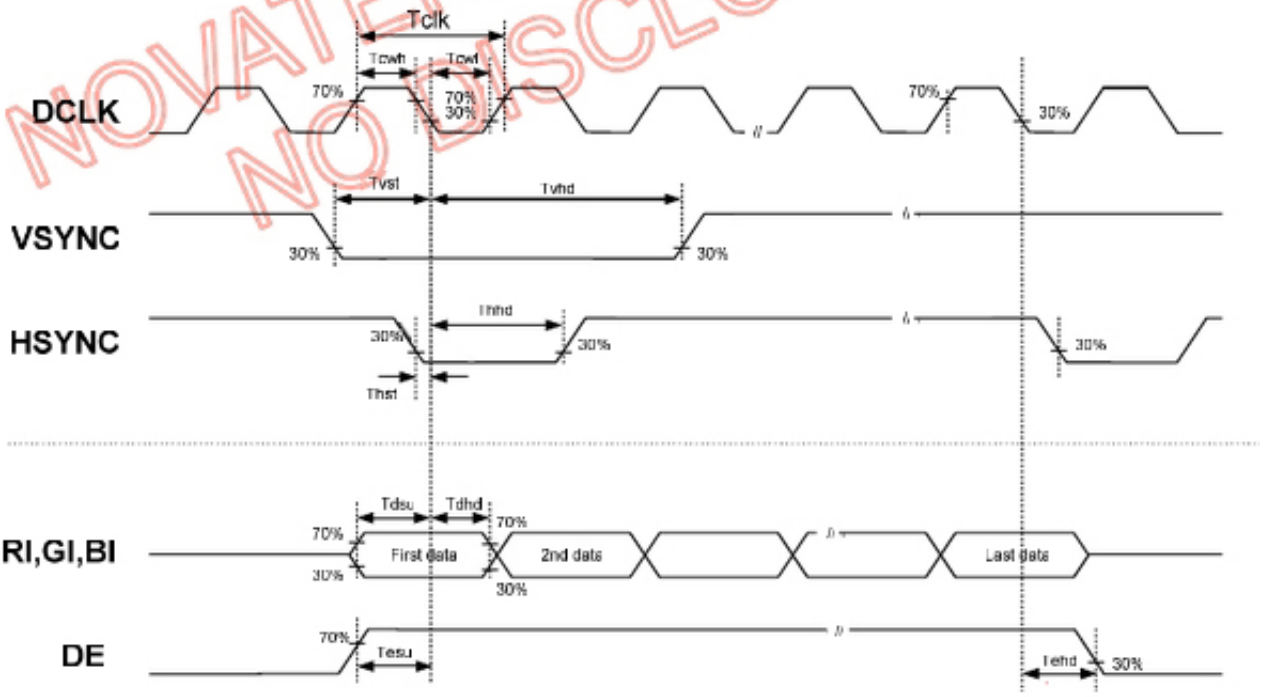
Timing Diagram

1. Power on sequence

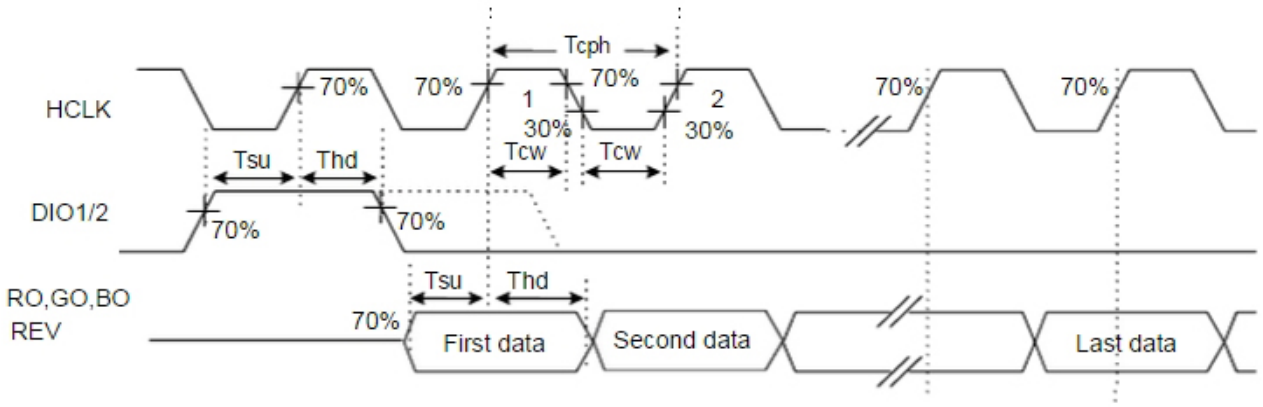


2. Reset time

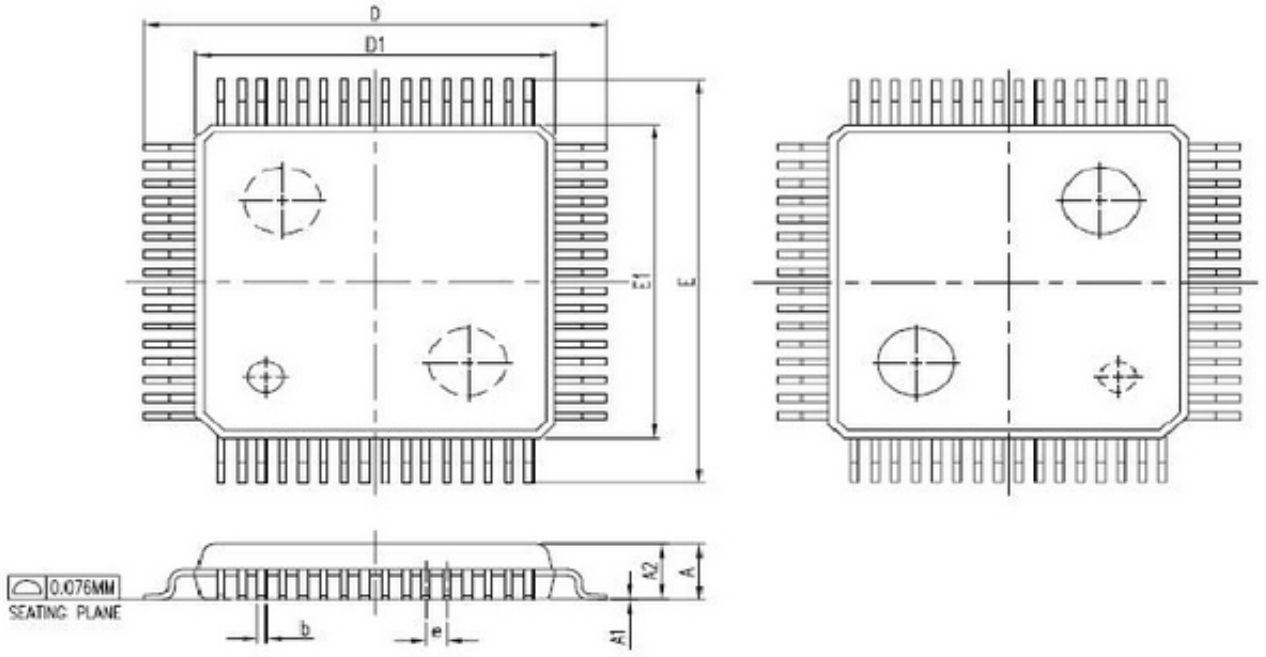
3. Clock and data input timing diagram

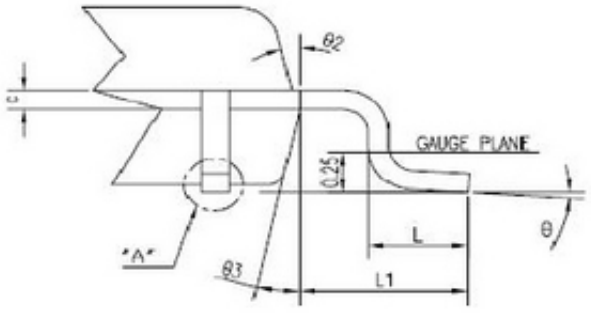


4. Output timing diagram

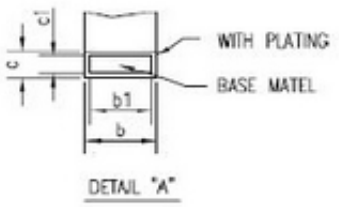


Package Information





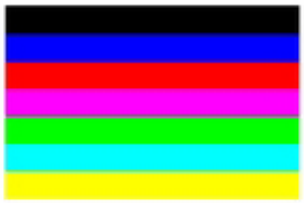
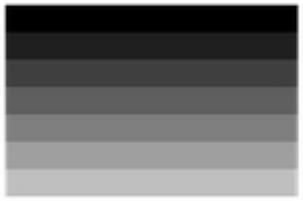
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.156			0.046
A1	0.05		0.15	0.002		0.006
A2	0.94	1.00	1.06	0.037	0.039	0.042
c	0.119		0.185	0.005		0.007
c1	0.127 TYP.			0.005 TYP.		
D	8.90	9.00	9.10	0.350	0.354	0.358
D1	6.95	7.00	7.05	0.273	0.276	0.278
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	6.95	7.00	7.05	0.273	0.276	0.278
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	1.00 REF.			0.039 REF.		
θ	1.5	3.5	5.5	1.5	3.5	5.5
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13



	MIN.	NOM.	MAX.	NOM.	MIN.	MAX.	NOM.	MIN.	MAX.
b	0.34		0.45	0.15		0.26	0.15		0.26
b1	0.34	0.37	0.40	0.15	0.18	0.21	0.15	0.18	0.21
e	0.80BSC.			0.50BSC.			0.40BSC.		
N	32			48			64		
JEDEC	MS-026 ABA			MS-026 ABC			MS-026 ABD		

Appendix A: Test Pattern

No.	Pattern	Test function Description	Notice
1		1. Color alignment with color filter.	
2		1. Color alignment with color filter.	
3		1. Color alignment with color filter.	
4		1. 64/256 Gray scale smooth?? 2. Data bit lose?? 3. Dithering function??	
5	Red grayscale	1. 64/256 Red grayscale smooth?? 2. Data bit lose?? 3. Dithering function??	
6	Green grayscale	1. 64/256 Green grayscale smooth?? 2. Data bit lose?? 3. Dithering function??	
7	Blue grayscale	1. 64/256 Blue grayscale smooth?? 2. Data bit lose?? 3. Dithering function??	
8		1. Cross talk?? (Vertical cross talk: Belong to Panel issue, Horzontal cross talk: Inversion structure issue(Line inversion),	

9		1. Customer standard test pattern. 2. Color alignment with color filter. 3. Driver scan direction.	
10		1. Customer standard test pattern. 2. Color alignment with color filter. 3. Driver scan direction.	
11		1. Customer standard test pattern.	
12		1. Customer standard test pattern.	
13	Black background with white boundary	1. Customer standard test pattern.	
14		1. Customer standard test pattern.	
15		1. Pixel black-gray pattern.	
16		1. Black-Gray flicker pattern	