

The SN5405 is obsolete and no longer is supplied.

SN54LS05, SN54S05 SN7405, SN74LS05, SN74S05 HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

SDLS030A – DECEMBER 1983 – REVISED NOVEMBER 2003

- Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs

- Dependable Texas Instrument Quality and Reliability

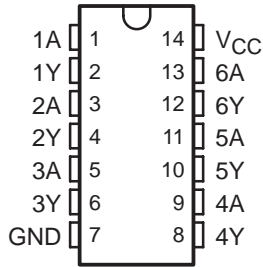
SN5405, SN54LS05, SN54S05 . . . J PACKAGE

SN7405 . . . N PACKAGE

SN74LS05 . . . D, DB, N, OR NS PACKAGE

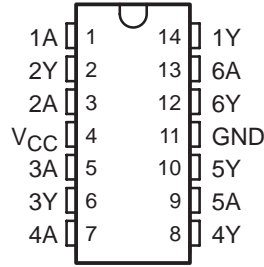
SN74S05 . . . D, N, OR NS PACKAGE

(TOP VIEW)



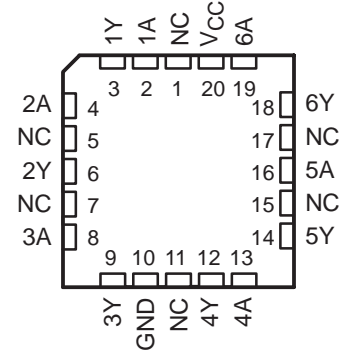
SN54LS05, SN54S05 . . . W PACKAGE

(TOP VIEW)



SN54LS05, SN54S05 . . . FK PACKAGE

(TOP VIEW)



NC – No internal connection

description/ordering information

These devices contain six independent inverters. To perform correctly, the open-collector outputs require pullup resistors. These devices may be connected to other open-collector outputs to implement active-low wired-OR or active-high wire-AND functions. Open-collector devices often are used to generate high V_{OH} levels.

ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING | |
|----------------|---------------|-------------|-----------------------|------------------|------------|
| 0°C to 70°C | PDIP – N | Tube | SN7405N | SN7405N | |
| | | | SN74LS05N | SN74LS05N | |
| | | | SN74S05N | SN74S05N | |
| | SOIC – D | Tube | SN74LS05D | LS05 | |
| | | | Tape and reel | | SN74LS05DR |
| | | | Tube | SN74S05D | S05 |
| | | | | Tape and reel | |
| SOP – NS | Tape and reel | SN74LS05NSR | 74LS05 | | |
| | | SN74S05NSR | 74S05 | | |
| –55°C to 125°C | CDIP – J | Tube | SNJ54LS05J | SNJ54LS05J | |
| | | | SNJ54S05J | SNJ54S05J | |
| | CDIP – W | Tube | SNJ54LS05W | SNJ54LS05W | |
| | | | SNJ54S05W | SNJ54S05W | |
| | LCCC – FK | Tube | SNJ54LS05FK | SNJ54LS05FK | |
| SNJ54S05FK | | | SNJ54S05FK | | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54LS05, SN54S05
SN7405, SN74LS05, SN74S05
HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

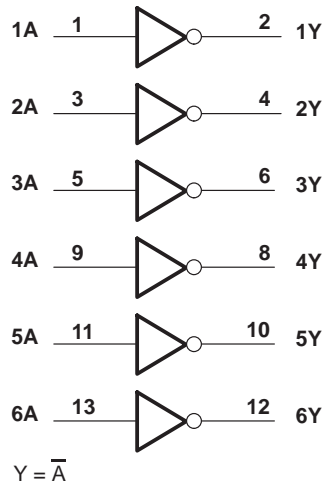
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FUNCTION TABLE
(each inverter)

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | L |
| L | H |

logic diagram (positive logic)



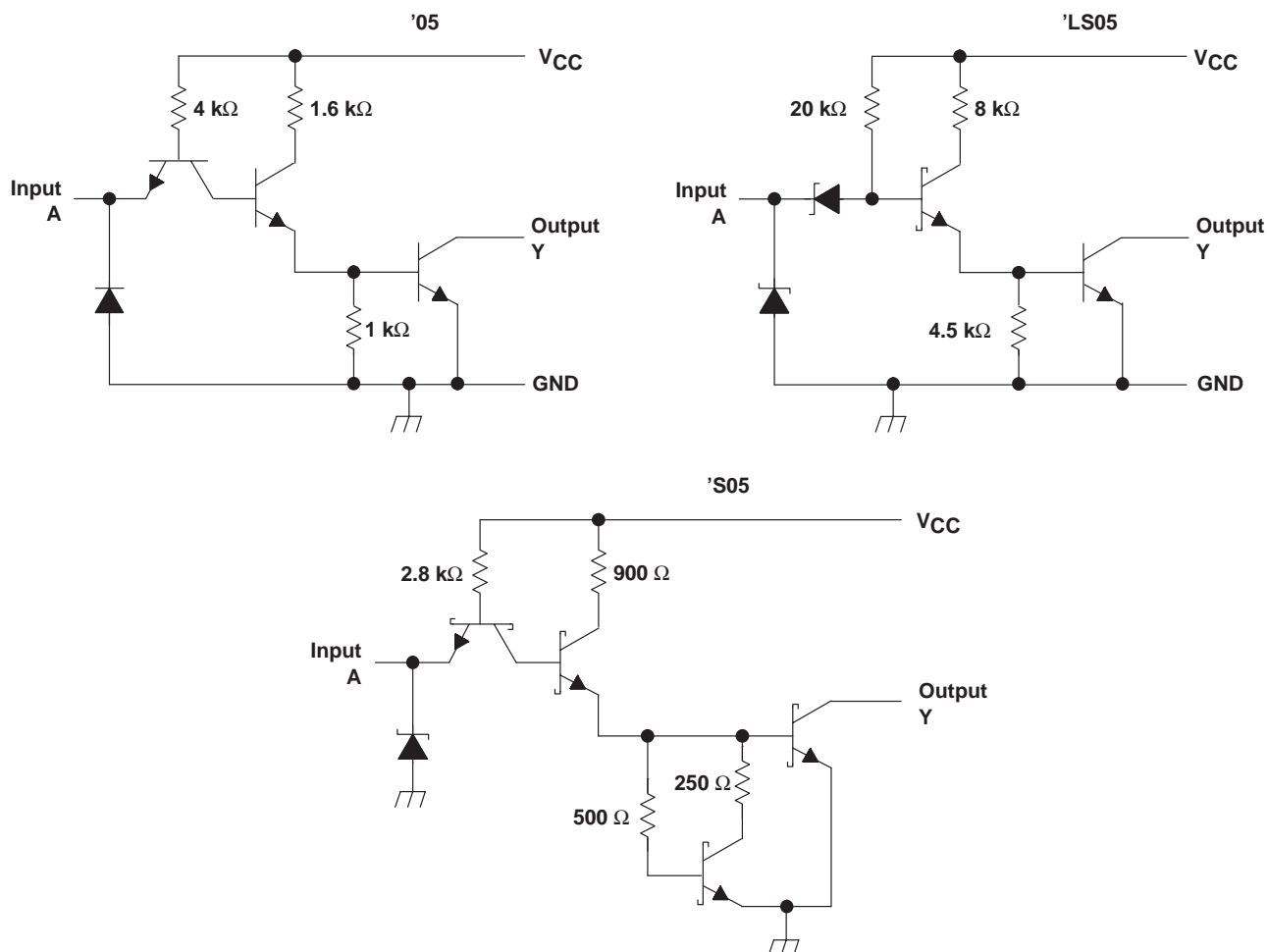
Pin numbers shown are for the D, DB, J, N, and NS packages.

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SN54LS05, SN54S05 SN7405, SN74LS05, SN74S05 HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

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schematic (each inverter)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

| | |
|--|----------------|
| Supply voltage, V _{CC} (see Note 1): '05, 'LS05, 'S05 | 7 V |
| Input voltage, V _I : '05, 'S05 | 5.5 V |
| 'LS05 | 7 V |
| Off-state output voltage, V _O | 7 V |
| Package thermal impedance, θ_{JA} (see Note 2): D package | 86°C/W |
| DB package | 96°C/W |
| N package | 80°C/W |
| NS package | 76°C/W |
| Storage temperature range, T _{stg} | -65°C to 150°C |

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

**SN54LS05, SN54S05
SN7405, SN74LS05, SN74S05
HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS**

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recommended operating conditions

| | SN5405 | | | SN7405 | | | UNIT |
|---|--------|-----|-----|--------|-----|------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V _{IH} High-level input voltage | 2 | | | 2 | | | V |
| V _{IL} Low-level input voltage | | | 0.8 | | | 0.8 | V |
| V _{OH} High-level output voltage | | | 5.5 | | | 5.5 | V |
| I _{OL} Low-level output current | | | 16 | | | 16 | mA |
| T _A Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS† | SN5405 | | | SN7405 | | | UNIT |
|------------------|--|--------|------|------|--------|------|------|------|
| | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| V _{IK} | V _{CC} = MIN, I _I = -12 mA | | | -1.5 | | | -1.5 | V |
| I _{OH} | V _{CC} = MIN, V _{OH} = 5.5 V V _{IL} = 0.8 V V _{IL} = 0.7 V | | | | | | 0.25 | mA |
| V _{OL} | V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 16 mA | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| I _I | V _{CC} = MAX, V _I = 5.5 V | | | 1 | | | 1 | mA |
| I _{IH} | V _{CC} = MAX, V _I = 2.4 V | | | 40 | | | 40 | µA |
| I _{IL} | V _{CC} = MAX, V _I = 0.4 V | | | -1.6 | | | -1.6 | mA |
| I _{CCH} | V _{CC} = MAX, V _I = 0 V | | 6 | 12 | | 6 | 12 | mA |
| I _{CCL} | V _{CC} = MAX, V _I = 4.5 V | | 18 | 33 | | 18 | 33 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------------------|--------------|-------------|------------------------|------------------------|-----|-----|-----|------|
| t _{PLH} | A | Y | R _L = 4 kΩ | C _L = 15 pF | | 40 | 55 | ns |
| t _{PHL} | | | R _L = 400 Ω | | | 8 | 15 | |



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SN54LS05, SN54S05
SN7405, SN74LS05, SN74S05
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recommended operating conditions

| | | SN54LS05 | | | SN74LS05 | | | UNIT |
|-----------------|--------------------------------|----------|-----|-----|----------|-----|------|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V _{IH} | High-level input voltage | 2 | | | 2 | | | V |
| V _{IL} | Low-level input voltage | | | | 0.7 | | | V |
| V _{OH} | High-level output voltage | | | | 5.5 | | | V |
| I _{OL} | Low-level output current | | | | 4 | | | mA |
| T _A | Operating free-air temperature | -55 | | | 125 | | | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS† | SN54LS05 | | | SN74LS05 | | | UNIT | |
|------------------|---|----------|------|-----|----------|------|------|------|----|
| | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | | |
| V _{IK} | V _{CC} = MIN, I _I = -18 mA | | | | -1.5 | | | V | |
| I _{OH} | V _{CC} = MIN, V _{IL} = MAX, V _{OH} = 5.5 V | | | | 0.1 | | | mA | |
| V _{OL} | V _{CC} = MIN, V _{IH} = 2 V | | | | 0.25 | 0.4 | 0.25 | 0.4 | V |
| | | | | | 0.35 | | | 0.5 | |
| I _I | V _{CC} = MAX, V _I = 7 V | | | | 0.1 | | | mA | |
| I _{IH} | V _{CC} = MAX, V _I = 2.7 V | | | | 20 | | | μA | |
| I _{IL} | V _{CC} = MAX, V _I = 0.4 V | | | | -0.4 | | | mA | |
| I _{CCH} | V _{CC} = MAX, V _I = 0 V | | | | 1.2 | 2.4 | 1.2 | 2.4 | mA |
| I _{CCL} | V _{CC} = MAX, V _I = 4.5 V | | | | 3.6 | 6.6 | 3.6 | 6.6 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--------------|-------------|---|-----|-----|-----|------|
| t _{PLH} | A | Y | R _L = 2 kΩ, C _L = 15 pF | | | 32 | ns |
| t _{PHL} | | | | 15 | 28 | | |



**SN54LS05, SN54S05
SN7405, SN74LS05, SN74S05
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recommended operating conditions

| | SN54S05 | | | SN74S05 | | | UNIT |
|---|---------|-----|-----|---------|-----|------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V _{IH} High-level input voltage | 2 | | | 2 | | | V |
| V _{IL} Low-level input voltage | | | 0.8 | | | 0.8 | V |
| V _{OH} High-level output voltage | | | 5.5 | | | 5.5 | V |
| I _{OL} Low-level output current | | | 20 | | | 20 | mA |
| T _A Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS† | | SN54S05 | | | SN74S05 | | | UNIT |
|------------------|------------------------|--|---------|------|------|---------|------|------|------|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| V _{IK} | V _{CC} = MIN, | I _I = -18 mA | | | -1.2 | | | -1.2 | V |
| I _{OH} | V _{CC} = MIN, | V _{OH} = 5.5 V | | | | | 0.25 | | mA |
| | | V _{IL} = 0.8 V | | | | | | | |
| | | V _{IL} = 0.7 V | | | 0.25 | | | | |
| V _{OL} | V _{CC} = MIN, | V _{IH} = 2 V, I _{OL} = 20 mA | | | 0.5 | | | 0.5 | V |
| I _I | V _{CC} = MAX, | V _I = 5.5 V | | | 1 | | | 1 | mA |
| I _{IH} | V _{CC} = MAX, | V _I = 2.7 V | | | 50 | | | 50 | µA |
| I _{IL} | V _{CC} = MAX, | V _I = 0.5 V | | | -2 | | | -2 | mA |
| I _{CCH} | V _{CC} = MAX, | V _I = 0 V | | 9 | 19.8 | | 9 | 19.8 | mA |
| I _{CCL} | V _{CC} = MAX, | V _I = 4.5 V | | 30 | 54 | | 30 | 54 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

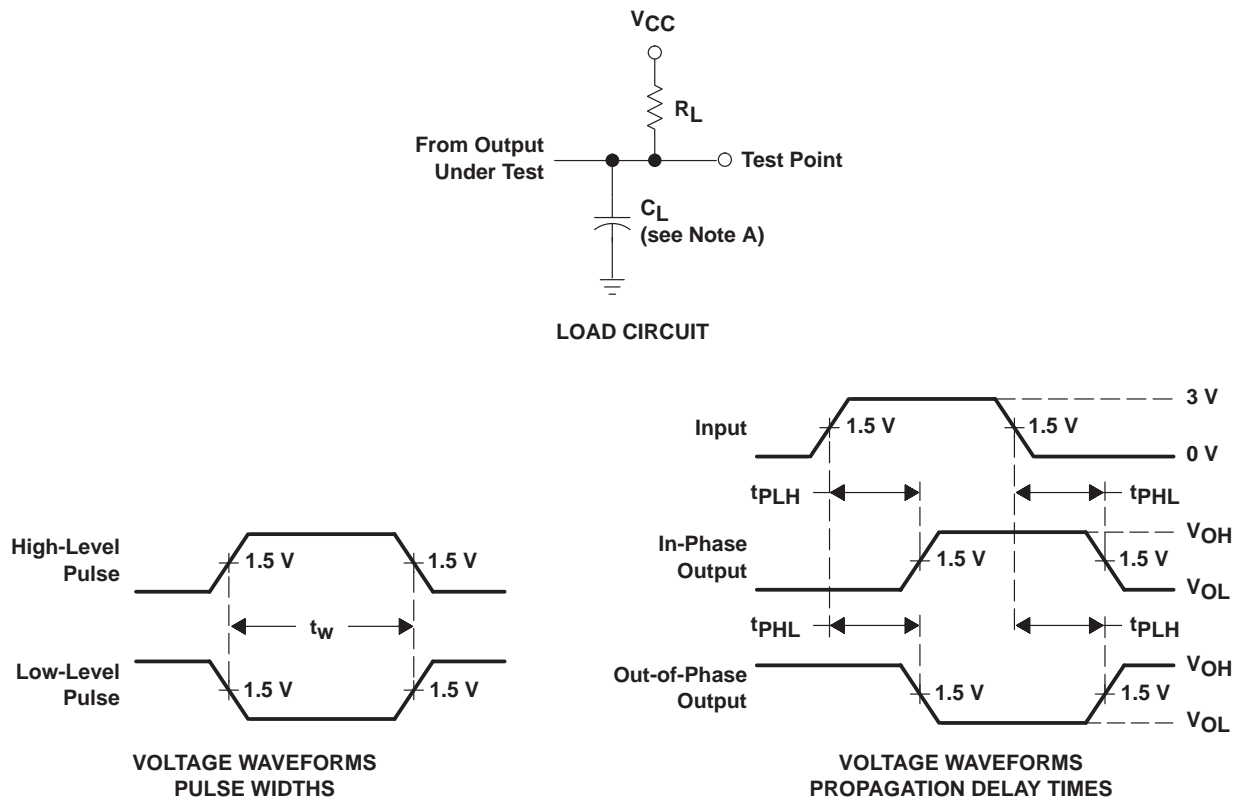
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------------------|--------------|-------------|------------------------|------------------------|-----|-----|-----|------|
| t _{PLH} | A | Y | R _L = 280 Ω | C _L = 15 pF | 2 | 5 | 7.5 | ns |
| t _{PHL} | | | | | 2 | 4.5 | 7 | |
| t _{PLH} | | | | C _L = 50 pF | 7.5 | ns | | |
| t _{PHL} | | | | | 7 | | | |



PARAMETER MEASUREMENT INFORMATION
SERIES 54/74 AND 54S/74S DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, and:
 For Series 54/74, $t_r \leq 7 \text{ ns}$, $t_f \leq 7 \text{ ns}$.
 For Series 54S/74S, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**SN54LS05, SN54S05
SN7405, SN74LS05, SN74S05
HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS**

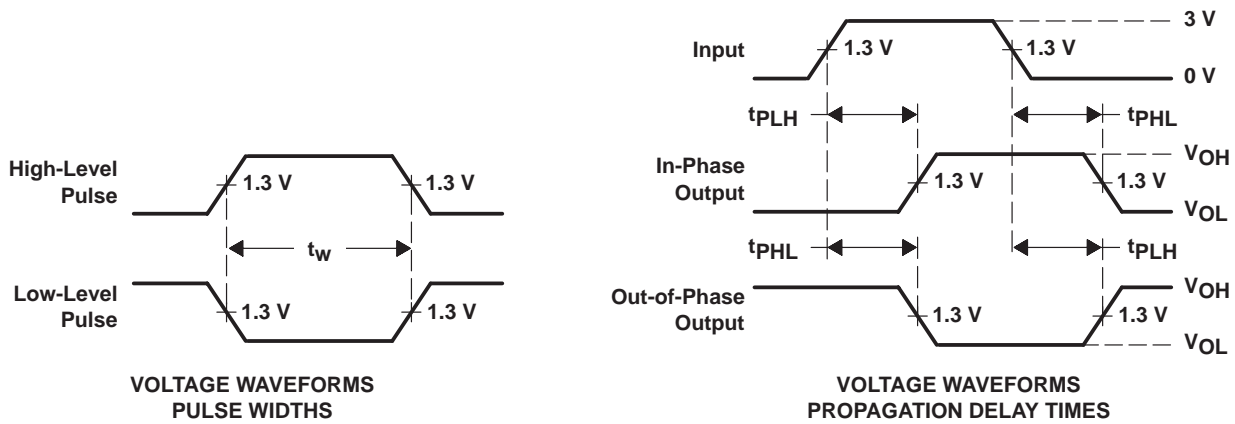
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**PARAMETER MEASUREMENT INFORMATION
SERIES 54LS/74LS DEVICES**



LOAD CIRCUIT



- NOTES: A. C_L includes probe and jig capacitance.
 B. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 1.5$ ns, $t_f \leq 2.6$ ns.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| JM38510/07004BCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 07004BCA | Samples |
| M38510/07004BCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 07004BCA | Samples |
| SN54LS05J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54LS05J | Samples |
| SN54S05J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54S05J | Samples |
| SN7405N | ACTIVE | PDIP | N | 14 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN7405N | Samples |
| SN7405NE4 | ACTIVE | PDIP | N | 14 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN7405N | Samples |
| SN74LS05D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS05 | Samples |
| SN74LS05DBR | ACTIVE | SSOP | DB | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS05 | Samples |
| SN74LS05DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS05 | Samples |
| SN74LS05DRE4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS05 | Samples |
| SN74LS05N | ACTIVE | PDIP | N | 14 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS05N | Samples |
| SN74LS05NE4 | ACTIVE | PDIP | N | 14 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS05N | Samples |
| SN74LS05NSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS05 | Samples |
| SN74S05D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | S05 | Samples |
| SN74S05N | ACTIVE | PDIP | N | 14 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74S05N | Samples |
| SN74S05NSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74S05 | Samples |
| SNJ54LS05FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | SNJ54LS 05FK | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SNJ54LS05J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ54LS05J | Samples |
| SNJ54LS05W | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ54LS05W | Samples |
| SNJ54S05FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | SNJ54S05FK | Samples |
| SNJ54S05J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ54S05J | Samples |
| SNJ54S05W | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ54S05W | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54LS05, SN54S05, SN74LS05, SN74S05 :

- Catalog: [SN74LS05](#), [SN74S05](#)
- Military: [SN54LS05](#), [SN54S05](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LS05DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LS05NSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74S05NSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LS05DR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| SN74LS05NSR | SO | NS | 14 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74S05NSR | SO | NS | 14 | 2000 | 367.0 | 367.0 | 38.0 |

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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