

### SILICON GATE CMOS

### 65,536 WORD x 16 BIT CMOS STATIC RAM

#### Description

The TC55V1664J/FT is a 1,048,576 bit high speed CMOS static random access memory organized as 65,536 words by 16 bits and operated from a single 3.3V supply. Toshiba's advanced CMOS technology and circuit design enable high speed operation.

The TC55V1664J/FT features low power dissipation when the device is deselected using chip enable ( $\overline{CE}$ ), and has an output enable input ( $\overline{OE}$ ) for fast memory access. Byte access is supported by upper and lower byte controls.

The TC55V1664J/FT is suitable for use in high speed applications such as cache memory and high speed storage. All inputs and outputs are LVTTTL compatible.

The TC55V1664J/FT is available in a 400mil width, 44-pin plastic SOJ and thin small outline package (forward type) suitable for high density surface assembly.

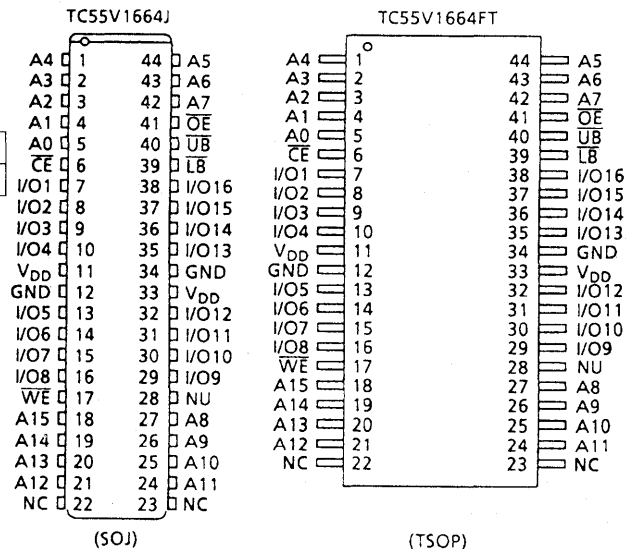
#### Features

- Fast access time
  - TC55V1664J/FT -10 10ns (max.)
  - TC55V1664J/FT -12 12ns (max.)
  - TC55V1664J/FT -15 15ns (max.)
- Low power dissipation

Cycle Time	10	12	15	20	30	ns
Operation (max.)	260	220	200	180	150	mA

- Standby: 1mA (max.)
- Single 3.3V power supply: 3.3V±0.3V
- Fully static operation
- Inputs and outputs LVTTTL compatible
- Output buffer control:  $\overline{OE}$
- Data byte controls:  $\overline{LB}$ ,  $\overline{UB}$
- Package
  - TC55V1664J: SOJ44-P-400
  - TC55V1664FT: TSOP44-P-400

#### Pin Connection (Top View)

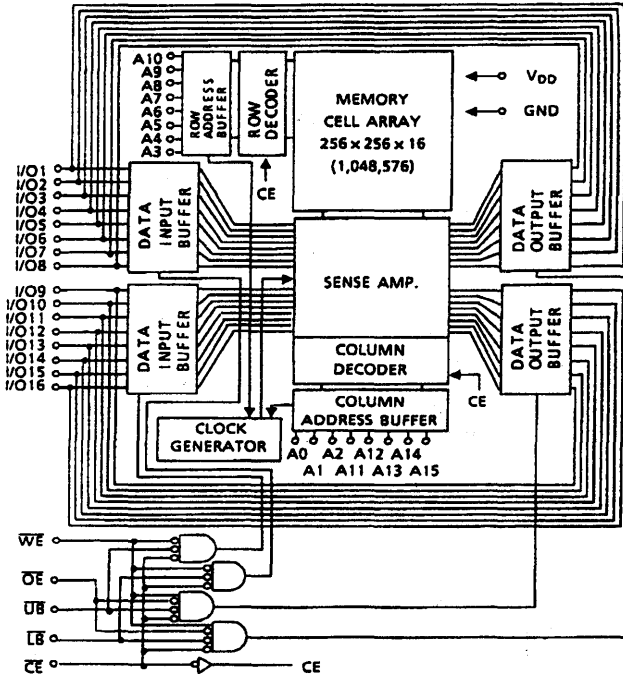


#### Pin Names

A0 ~ A15	Address Inputs
I/O1 ~ I/O16	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$ , $\overline{UB}$	Data Byte Control Inputs
V <sub>DD</sub>	Power (+3.3V)
GND	Ground
NC	No Connection
NU*	Not Usable (Input)

\* The NU pin must be kept electronically open, pulled down to GND, or less than 0.8V. Applying a voltage greater than 0.8V to the NU pin is prohibited.

Block Diagram



Operating Mode

MODE	PIN	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/01 - I/08	I/09 ~ I/016	POWER
Read	L	L	L	H	L	L	Output	Output	$I_{DD0}$
					H	L	High Impedance	Output	$I_{DD0}$
					L	H	Output	High Impedance	$I_{DD0}$
Write	L	L	*	L	L	L	Input	Input	$I_{DD0}$
					H	L	High Impedance	Input	$I_{DD0}$
					L	H	Input	High Impedance	$I_{DD0}$
Output Disable	L	L	H	H	*	*	High Impedance	High Impedance	$I_{DD0}$
					H	H	High Impedance	High Impedance	$I_{DD0}$
Standby	H	H	*	*	*	*	High Impedance	High Impedance	$I_{DDs}$

\*H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
$V_{DD}$	Power Supply Voltage	-0.5 ~ 4.6	V
$V_{IN}$	Input Voltage	-0.5* ~ 4.6	V
$V_{IO}$	Input/Output Voltage	-0.5* ~ $V_{DD} + 0.5^{**}$	V
$P_D$	Power Dissipation	1.2	W
$T_{SOLDER}$	Soldering Temperature • Time	260 • 10	°C • sec
$T_{STRG}$	Storage Temperature	-65 ~ 150	°C
$T_{OPR}$	Operating Temperature	-10 ~ 85	°C

\*\* Not yet specified

## DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub>	Power Supply Voltage	3.0	3.3	3.6	V
V <sub>IH</sub>	Input High Voltage	2.0	-	V <sub>DD</sub> + 0.3**	V
V <sub>IL</sub>	Input Low Voltage	-0.3*	-	0.8	V

\*/\*\* Not yet specified

DC Characteristics (Ta = 0 ~ 70°C, V<sub>DD</sub> = 3.3V±0.3V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
I <sub>LI</sub>	Input Leakage Current (except NU Pin)	V <sub>IN</sub> = 0 ~ V <sub>DD</sub>	-	-	±1	μA	
I <sub>LO</sub>	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$ V <sub>OUT</sub> = 0 ~ V <sub>DD</sub>	-	-	±1	μA	
I <sub>I(NU)</sub>	Input Current (NU Pin)	V <sub>IN</sub> = 0 ~ 0.8V	-1	-	20	μA	
		V <sub>IN</sub> = 0 ~ 0.2V	-	-	±1		
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -2mA	2.4	-	-	V	
		I <sub>OH</sub> = -20μA	V <sub>DD</sub> - 0.2	-	-		
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2mA	-	-	0.4	V	
		I <sub>OL</sub> = 20μA	-	-	0.2		
I <sub>DDO</sub>	Operating Current	$\overline{CE} = V_{IL}$ , I <sub>OUT</sub> = 0mA, Other Inputs = V <sub>IH</sub> /V <sub>IL</sub>	t <sub>cycle</sub> = 10ns	-	-	260	mA
			t <sub>cycle</sub> = 12ns	-	-	220	
			t <sub>cycle</sub> = 15ns	-	-	200	
			t <sub>cycle</sub> = 20ns	-	-	180	
			t <sub>cycle</sub> = 30ns	-	-	150	
I <sub>DDS1</sub>	Standby Current	$\overline{CE} = V_{IH}$ , Other Inputs = V <sub>IH</sub> /V <sub>IL</sub>	-	-	20	mA	
		$\overline{CE} = V_{DD} - 0.2V$ Other Inputs = V <sub>DD</sub> - 0.2V or 0.2V	-	-	1		

## Capacitance\* (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = GND	6	pF
C <sub>I/O</sub>	Input/Output Capacitance	V <sub>I/O</sub> = GND	8	pF

\*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C<sup>(1)</sup>, V<sub>DD</sub> = 3.3V±0.3V)

Read Cycle

SYMBOL	PARAMETER	TC55V1664J/FT -10		TC55V1664J/FT -12		TC55V1664J/FT -15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	10	—	12	—	15	—	ns
t <sub>ACC</sub>	Address Access Time	—	10	—	12	—	15	
t <sub>CO</sub>	$\overline{CE}$ Access Time	—	10	—	12	—	15	
t <sub>OE</sub>	$\overline{OE}$ Access Time	—	5	—	6	—	8	
t <sub>BA</sub>	$\overline{UB}$ , $\overline{LB}$ Access Time	—	5	—	6	—	8	
t <sub>OH</sub>	Output Data Hold Time from Address Change	3	—	3	—	3	—	
t <sub>COE</sub>	Output Enable Time from $\overline{CE}$	3	—	3	—	3	—	
t <sub>OEE</sub>	Output Enable Time from $\overline{OE}$	1	—	1	—	1	—	
t <sub>BE</sub>	Output Enable Time from $\overline{UB}$ , $\overline{LB}$	1	—	1	—	1	—	
t <sub>COD</sub>	Output Disable Time from $\overline{CE}$	—	6	—	7	—	8	
t <sub>ODO</sub>	Output Disable Time from $\overline{OE}$	—	6	—	7	—	8	
t <sub>BD</sub>	Output Disable Time from $\overline{UB}$ , $\overline{LB}$	—	6	—	7	—	8	

Write Cycle

SYMBOL	PARAMETER	TC55V1664J/FT -10		TC55V1664J/FT -12		TC55V1664J/FT -15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	10	—	12	—	15	—	ns
t <sub>WP</sub>	Write Pulse Width	7	—	8	—	9	—	
t <sub>CW</sub>	Chip Enable to End of Write	9	—	10	—	11	—	
t <sub>BW</sub>	$\overline{UB}$ , $\overline{LB}$ Enable to End of Write	9	—	10	—	11	—	
t <sub>AW</sub>	Address Valid to End of Write	9	—	10	—	11	—	
t <sub>AS</sub>	Address Setup Time	0	—	0	—	0	—	
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	0	—	
t <sub>DS</sub>	Data Setup Time	6	—	7	—	8	—	
t <sub>DH</sub>	Data Hold Time	0	—	0	—	0	—	
t <sub>OEW</sub>	Output Enable Time from $\overline{WE}$	1	—	1	—	1	—	
t <sub>ODW</sub>	Output Disable Time from $\overline{WE}$	—	6	—	7	—	8	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

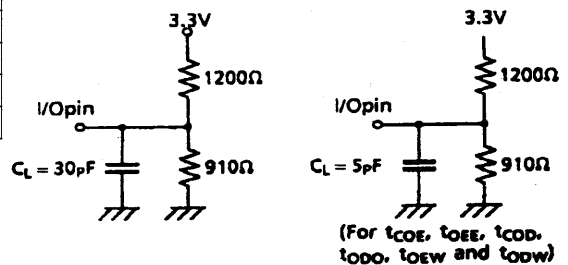
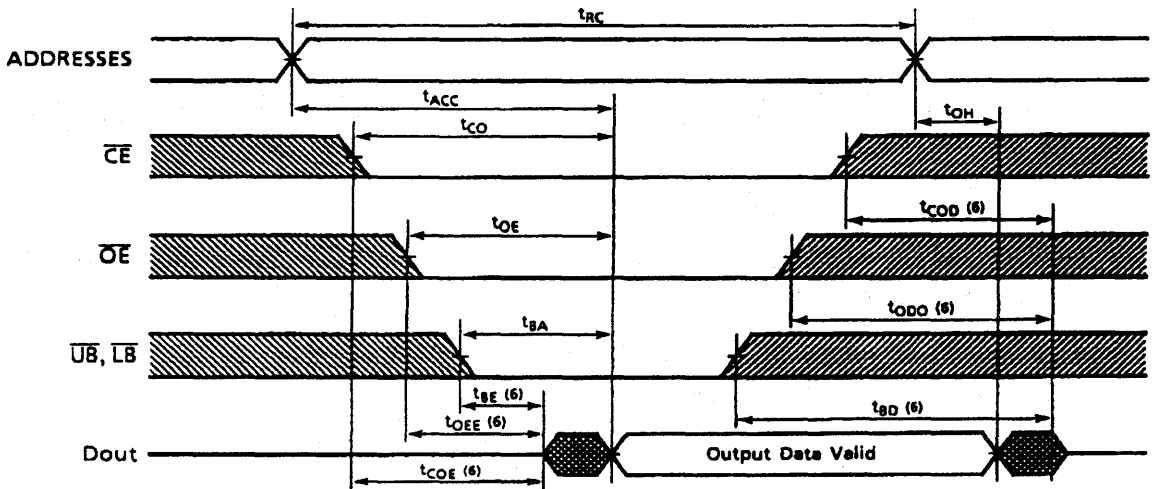


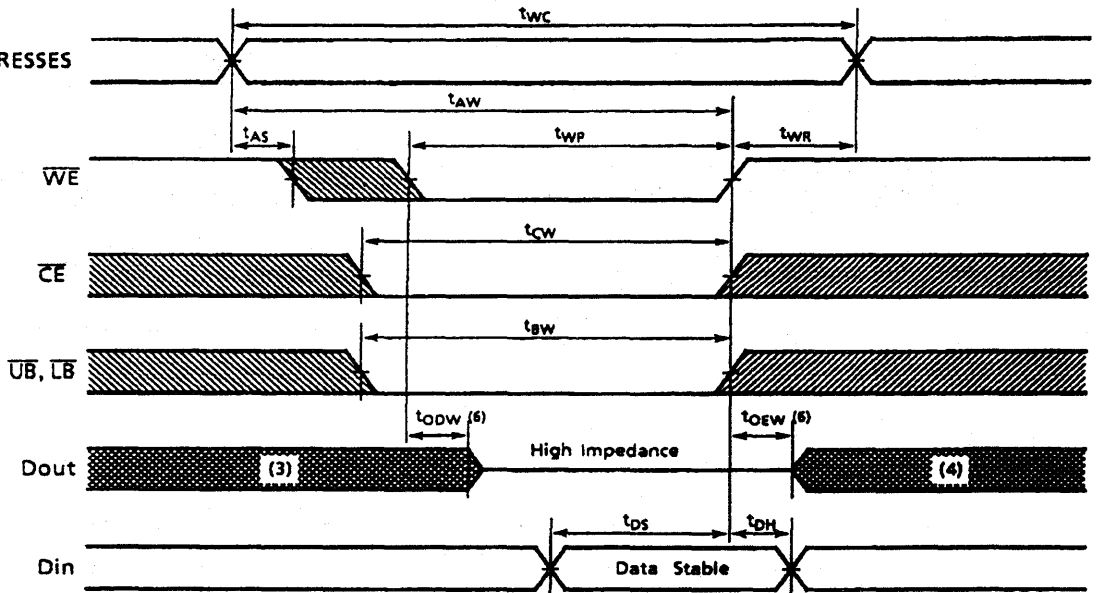
Figure 1.

Timing Waveforms

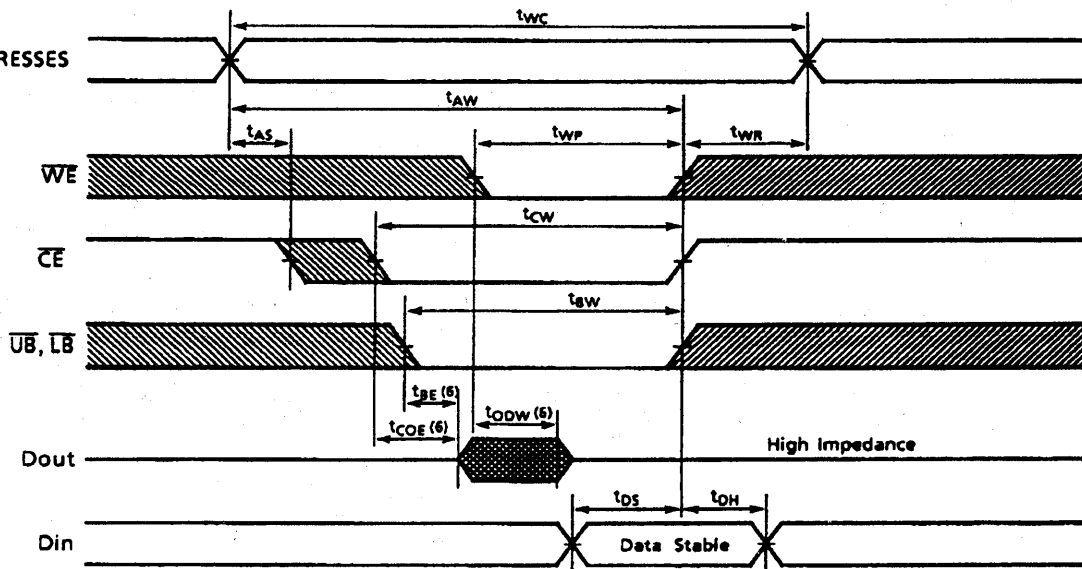
Read Cycle <sup>(2)</sup>



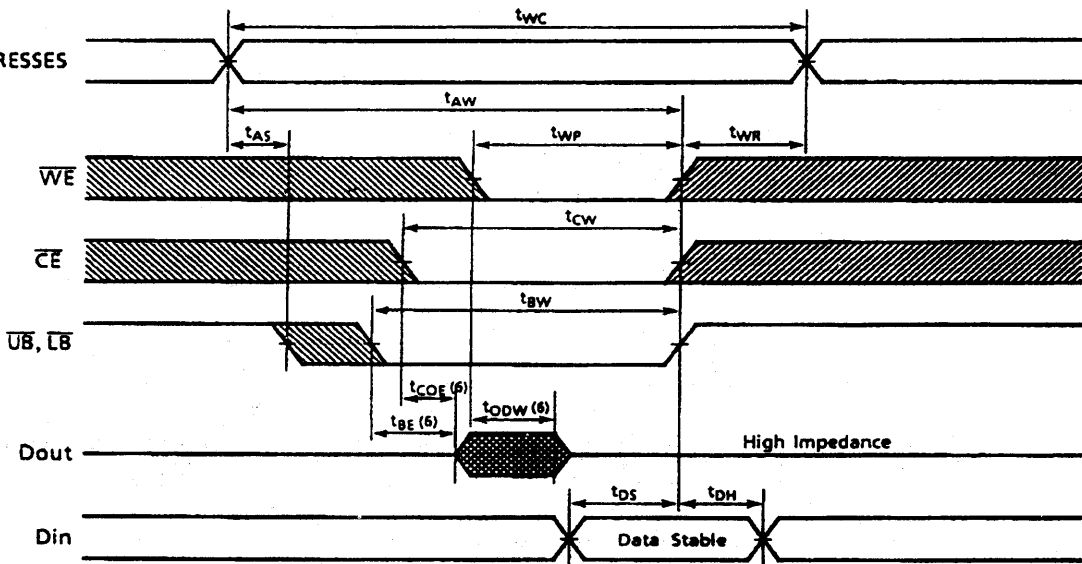
Write Cycle 1 <sup>(5)</sup> ( $\overline{WE}$  Controlled)



Write Cycle 2 <sup>(5)</sup> ( $\overline{CE}$  Controlled)



Write Cycle 3 <sup>(5)</sup> ( $\overline{UB}, \overline{LB}$  Controlled)



Notes:

1. The operating temperature ( $T_a$ ) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2.  $\overline{WE}$  is high for read cycles.
3. If the  $\overline{CE}$  low transition occurs coincident with or after the  $\overline{WE}$  low transition, outputs remain in a high impedance state.
4. If the  $\overline{CE}$  high transition occurs coincident with or prior to the  $\overline{WE}$  high transition, outputs remain in a high impedance state.
5. If  $\overline{OE}$  is high during a write cycle, the outputs are in a high impedance state during this period.
6. The following parameters are measured using the load shown in Fig. 1.  
 (A)  $t_{COE}$ ,  $t_{OEE}$ ,  $t_{BE}$ ,  $t_{OE\overline{W}}$  . . . . . Output Enable Time  
 (B)  $t_{COD}$ ,  $t_{ODO}$ ,  $t_{BD}$ ,  $t_{OD\overline{W}}$  . . . . . Output Disable Time

