MOTOROLA

MC14548B

Advance Information

DUAL MONOSTABLE MULTIVIBRATOR
(RETRIGGERABLE, RESETTABLE)

The MC14548B is identical in pinout to the MC14538B and the MC14528B.

This dual monostable multivibrator may be triggered by either the positive (A input) or the negative edge (B input) of an input pulse, and produces an output pulse over a wide range of pulse widths. The output pulse width is determined by the external timing components, R_X and C_X. The device has a reset function which forces the Q output low and $\overline{Q}$ output high, regardless of the state of the output pulse circuitry.

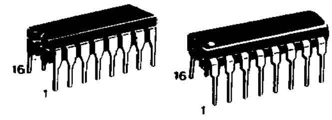
Due to minimal output pulse width variation over temperature, the MC14548 is recommended for new designs in lieu of the MC14528 or MC14538. However, the MC14548 requires more quiescent current than the MC14528 or MC14538.

- Unlimited Rise and Fall Times Allowed on the A Trigger Input
- Output Pulse Width is Independent of the Trigger Pulse Width
- Latched Trigger and Reset Inputs
- Supply Voltage Range = 3.0 to 18.0 Vdc
- For pulse widths < 1 μs, use the HC4538

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL (RETRIGGERABLE, RESETTABLE) MONOSTABLE MULTIVIBRATOR



L SUFFIX
CERAMIC PACKAGE
CASE 620

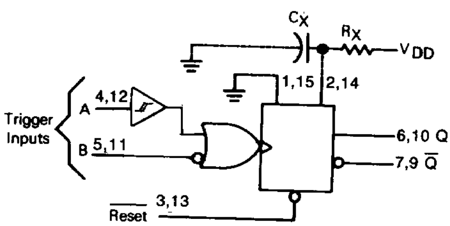
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

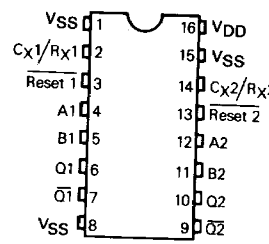
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

BLOCK DIAGRAM (1/2 OF DEVICE SHOWN)

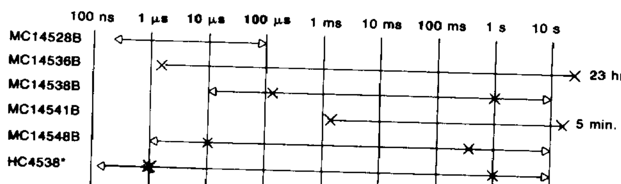


V_{DD} = Pin 16
V_{SS} = Pin 1, Pin 8, Pin 15
R_X and C_X are external components

PIN ASSIGNMENT



ONE-SHOT SELECTION GUIDE



*LIMITED OPERATING VOLTAGE (2-6V)

Total Output Pulse Width Range ◁————▷
Recommended Pulse Width Range ×————×

FUNCTION TABLE

Inputs			Outputs	
$\overline{Reset}$	A	B	Q	$\overline{Q}$
H	↑	H	⊓	⊔
H	L	↓	⊓	⊔
H	↑↓	L	Not Triggered	
H	H	↑↓	Not Triggered	
H	L, H, ↓	H	Not Triggered	
H	L	L, H, ↑	Not Triggered	
L	X	X	L	H
↓↑	X	X	Not Triggered	

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD}	T_{low}*		25°C			T_{high}*		Unit
		Vdc	Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage "0" Level, V_{in} = V_{DD} or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	V
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level, V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	V
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc)	V_{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	V
(V_O = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
"1" Level (V_O = 0.5 or 4.5 Vdc)	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	V
(V_O = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current Source (V_{OH} = 2.5 Vdc)	I_{OH}	5.0	−3.0	—	−2.4	−4.2	—	−1.7	—	mA
(V_{OH} = 4.6 Vdc)		5.0	−0.64	—	−0.51	−0.88	—	−0.36	—	
(V_{OH} = 9.5 Vdc)		10	−1.6	—	−1.3	−2.25	—	−0.9	—	
(V_{OH} = 13.5 Vdc)		15	−4.2	—	−3.4	−8.8	—	−2.4	—	
Sink (V_{OL} = 0.4 Vdc)	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mA
(V_{OL} = 0.5 Vdc)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current, Pin 2 or 14	I_{in}	15	—	±0.05	—	±0.00001	±0.05	—	±0.5	µA
Input Current, Other Inputs	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	µA
Input Capacitance, Pin 2 or 14	C_{in}	—	—	—	—	25	—	—	—	pF
Input Capacitance, Other Inputs (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current, Standby State (AL Devices) (Per Package) Q = Low, $\overline{Q}$ = High	I_{DD}	5.0	—	60	—	50	60	—	170	µA
		10	—	85	—	75	85	—	220	
		15	—	110	—	80	110	—	270	
Quiescent Current, Standby State (CL/CP Devices) (Per Package) Q = Low, $\overline{Q}$ = High	I_{DD}	5.0	—	80	—	50	80	—	220	µA
		10	—	105	—	75	105	—	270	
		15	—	130	—	80	130	—	370	
Quiescent Current, Active State (ALL) (Per Package) $\overline{Q}$ = Low, Q = High	I_{DD}	5.0	—	2.0	—	.04	.20	—	2.0	mA
		10	—	2.0	—	.08	.45	—	2.0	
		15	—	2.0	—	.13	.70	—	2.0	

* T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

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SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types Min	All Types Typ #	All Types Max	Unit
Output Transition Time Q or $\overline{Q}$	t_{TLH}, t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time A or B to Q or $\overline{Q}$	t_{PLH}, t_{PHL}	5.0 10 15	— — —	200 100 80	400 200 160	ns
$\overline{\text{Reset}}$ to Q or $\overline{Q}$		5.0 10 15	— — —	185 90 75	370 180 150	ns
Input Pulse Width A, B or $\overline{\text{Reset}}$	$t_{w(H)}$, $t_{w(L)}$	5.0 10 15	50 30 20	25 15 10	— — —	ns
Retrigger Time, To Extend Pulse Input A or B (C_X in μf) $K_1 = 2000\left(\frac{V}{\mu F}\right)$; $K_2 = 13\left(\frac{V}{\mu F}\right)$	t_{rx}	5.0 10 15	$0.75 + \frac{K_1 C_X}{V_{DD}+K_2 C_X}$	— — —	— — —	μs
Retrigger Time, To Issue New Pulse Input A or B	t_{rr}	5.0 10 15	0 0 0	— — —	— — —	ns
Recovery Time $\overline{\text{Reset}}$ Inactive to A or B	t_{rec}	5.0 10 15	20 10 6	11.6 4.8 3.0	— — —	ns
Input Rise and Fall Time $\overline{\text{Reset}}$	t_r, t_f	5.0 10 15	— — —	— — —	15 5 4	μs
B Input		5.0 10 15	— — —	286 40 22	200 25 15	
A Input		5.0 10 15	No Limit			
Output Pulse Width — Q or $\overline{Q}$ C_X = 0.001 μF R_X = 10 kΩ	τ	5.0 10 15	9 8 8	12.6 11.8 11.6	15 14 14	μs
C_X = 0.01 μF R_X = 10 kΩ		5.0 10 15	82 69 61	90 77 73	100 85 80	μs
C_X = 1.0 μF R_X = 100 kΩ		5.0 10 15	64 62 62	71 68 68	78 75 75	ms
Pulse Width Match between circuits in the same package C_X = 0.1 μF R_X = 100 kΩ	$\frac{T1 - T2}{T1}$	5.0 10 15	— — —	±1 ±1 ±1	— — —	%

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

OPERATING CONDITIONS

External Timing Resistance	R_X	—	5.0	—	*	kΩ
External Timing Capitance	C_X	—	0	—	*	pF

* The maximum allowable values of R_X and C_X are a function of the leakage of capacitor C_X, the leakage of the MC14548B, and leakage due to board layout and surface resistance. Values of R_X and C_X should be chosen so that the maximum current into pin 2 or pin 14 is 10 mA. Susceptibility to externally induced noise signals may occur for $R_X \gg 1$ MΩ.

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PIN DESCRIPTIONS

INPUTS

A1, A2 (Pins 4, 12) — Positive-edge trigger inputs. A rising-edge signal on either of these pins will trigger the corresponding multivibrator when there is a high voltage level on the B1 or B2 input.

B1, B2 (Pins 5, 11) — Negative-edge trigger inputs. A falling-edge signal on either of these pins will trigger the corresponsing multivibrator when there is a low voltage level on the A1 or A2 input.

$\overline{\text{Reset 1}}$, $\overline{\text{Reset 2}}$ (Pins 3, 13) — Reset inputs (active low). When a low voltage is applied to one of these pins, the Q output of the corresponding multivibrator is reset to a low voltage and the $\overline{Q}$ output is set to a high voltage.

C_X1/R_X1 and C_X2/R_X2 (Pins 2 and 14) — External timing components. These pins are tied to the common points of the external timing resistors and capacitors (see the Block Diagram).

OUTPUTS

Q1, Q2 (Pins 6,10) — Noninverted monostable outputs. These pins (normally low) pulse high when the multivibrator is triggered at either the A or the B input. The width of the pulse is determined by the external timing components, R_X and C_X.

$\overline{\text{Q1}}$, $\overline{\text{Q2}}$ (Pins 7, 9) — Inverted monostable outputs. These pins (normally high) pulse low when the multivibrator is triggered at either the A or the B input. These outputs are the inverse of Q1 and Q2.

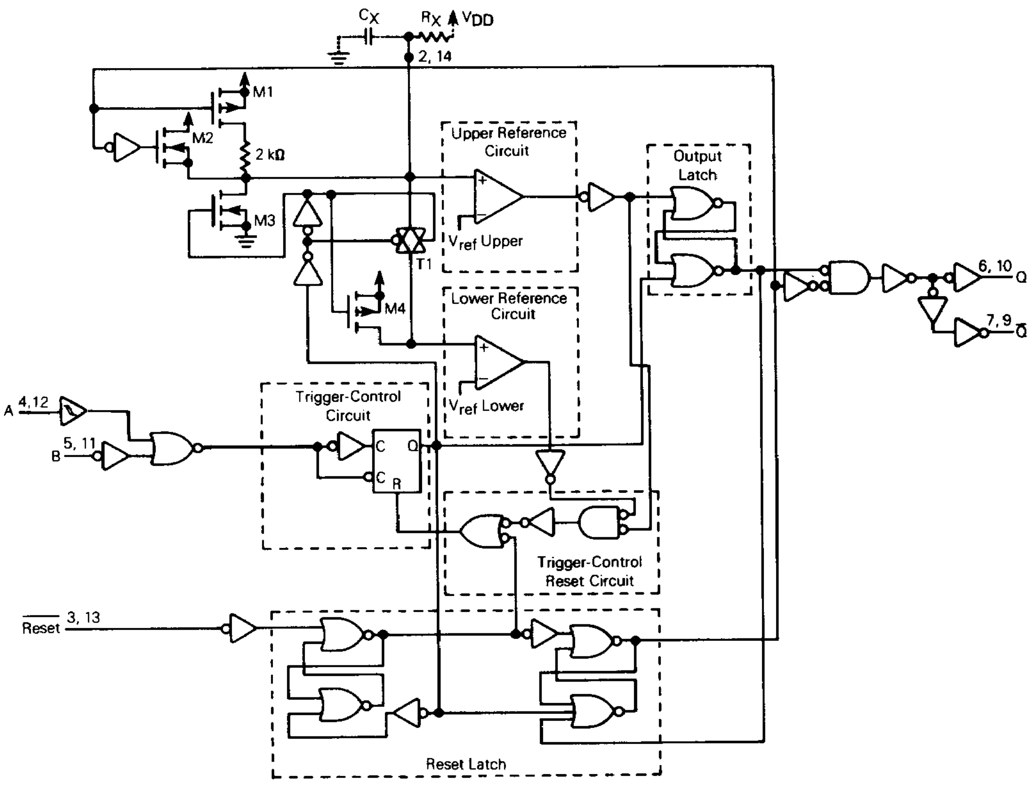
POWER

V_{DD} (Pin 16) — Most positive supply potential. This voltage may range from 3 to 18 volts with respect to V_{SS}.

V_{SS} (Pins 1, 8, 15) — Most negative supply potential (usually ground).

NOTE: All 3 pins must be connected externally to the power supply to insure proper performance.

FIGURE 1 — FUNCTION DIAGRAM
(½ the device)



CIRCUIT OPERATION

Figure 4 shows the 14548B configured in the retriggerable mode. Briefly, the device operates as follows (refer to Figure 1). In the quiescent state, the external timing capacitor, C_X, is charged to V_{DD}. When a trigger occurs, the Q output goes high and C_X discharges quickly to the lower reference voltage (V_{ref} Lower ≈ 1/3 V_{DD}). C_X then charges, through R_X, back up to the upper reference voltage (V_{ref} Upper ≈ 2/3 V_{DD}), at which point the one-shot has timed out and the Q output goes low.

The following, more detailed description of the circuit operation refers to both the function diagram (Figure 1) and the timing diagram (Figure 2).

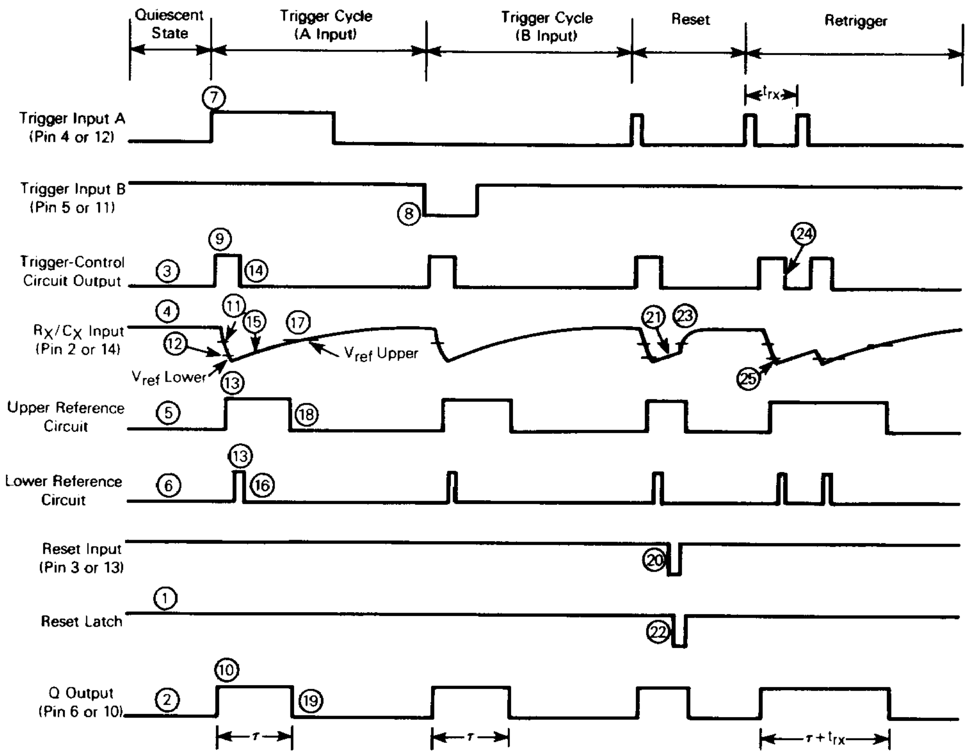
QUIESCENT STATE

In the quiescent state, before an input trigger appears, the output latch is high and the reset latch is high (#1 in Figure 2). Thus the Q output (pin 6 or 10) of the monostable multivibrator is low (#2, Figure 2).

The output of the trigger-control is low (#3), and transistors M1, M2, and M3 are turned off. The external timing capacitor, C_X, is charged to V_{DD} (#4), and the upper reference circuit has a low output (#5). Transistor M4 is turned on and transmission gate T1 is turned off. Thus the lower reference circuit has V_{DD} at the noninverting input and a resulting low output (#6).

In addition, the output of the trigger-control reset circuit is low.

FIGURE 2 — TIMING DIAGRAM



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TRIGGER OPERATION

The 14548B is triggered by either a rising-edge signal at input A (#7) or a falling-edge signal at input B (#8), with the unused trigger input and the Reset input held at the voltage levels shown in the Function Table. Either trigger signal will cause the output of the trigger-control circuit to go high (#9).

The trigger-control circuit going high simultaneously initiates three events. First, the output latch goes low, thus taking the Q output of the 14548B to a high state (#10). Second, transistor M3 is turned on, which allows the external timing capacitor, C_X, to rapidly discharge toward ground (#11). (Note that the voltage across C_X appears at the input of the upper reference circuit comparator). Third, transistor M4 is turned off and transmission gate T1 is turned on, thus allowing the voltage across C_X to also appear at the input of the lower reference circuit comparator.

When C_X discharges to the reference voltage of the lower reference circuit (#12), the outputs of both reference circuits will be high (#13). The trigger-control reset circuit goes high, resetting the trigger-control circuit flip-flop to a low state (#14). This turns transistor M3 off again, allowing C_X to begin to charge back up toward V_{DD}, with a time constant $t = R_XC_X$ (#15). In addition, transistor M4 is turned on and transmission gate T1 is turned off. Thus a high voltage level is applied to the input of the lower reference circuit comparator, causing its output to go low (#16). The monostable multivibrator may be retriggered at any time after the trigger-control circuit goes low.

When C_X charges up to the reference voltage of the upper reference circuit (#17), the output of the upper reference circuit goes low (#18). This causes the output latch to toggle, taking the Q output of the 14548B to a low state (#19), and completing the time-out cycle.

RESET OPERATION

A low voltage applied to the $\overline{\text{Reset}}$ pin always forces the Q output of the 14548B to a low state.

The timing diagram illustrates the case in which reset occurs (#20) while C_X is charging up toward the reference voltage of the upper reference circuit (#21). When a reset occurs, the output of the reset latch goes low (#22), turning on transistor M1. Thus C_X is allowed to quickly charge up to V_{DD} (#23) to await the next trigger signal.

RETRIGGER OPERATION

When used in the retriggerable mode (Figure 4), the MC14548B may be retriggered during timing out of the output pulse at any time after the trigger-control circuit flip-flop has been reset (#24). Because the trigger-control circuit flip-flop resets shortly after C_X has discharged to the reference voltage of the lower reference circuit (#25), the minimum retrigger time, t_{rx} (Figure 1) is a function of internal propagation delays and the discharge time of C_X.

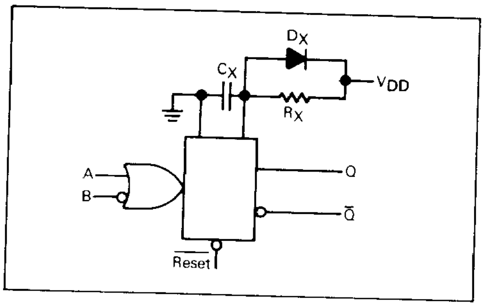
Figure 5 shows the device configured in the non-triggerable mode.

POWER-DOWN CONSIDERATIONS

Large values of C_X may cause problems when powering down the 14548B because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor may discharge from V_{DD} through the input protection diodes at pin 2 or pin 14. Current through the protection diodes must be limited to 10 mA, therefore, the turn-off time of the V_{DD} power supply must not be faster than $t = V_{DD} \bullet C_X/(10\ mA)$. For example, if $V_{DD} = 5$ V and $C_X = 15\ \mu F$, the V_{DD} supply must turn off no faster than $t = (5\ V) \bullet (15\ \mu F)/10\ mA = 7.5$ ms. This is usually not a problem because power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of V_{DD} to zero volts occurs, the MC14548B may sustain damage. To avoid this possibility, use an external clamping diode, D_X, connected as shown in Figure 3.

FIGURE 3 — DISCHARGE PROTECTION DURING POWER DOWN



TYPICAL APPLICATIONS

FIGURE 4 – RETRIGGERABLE MONOSTABLE CIRCUITRY

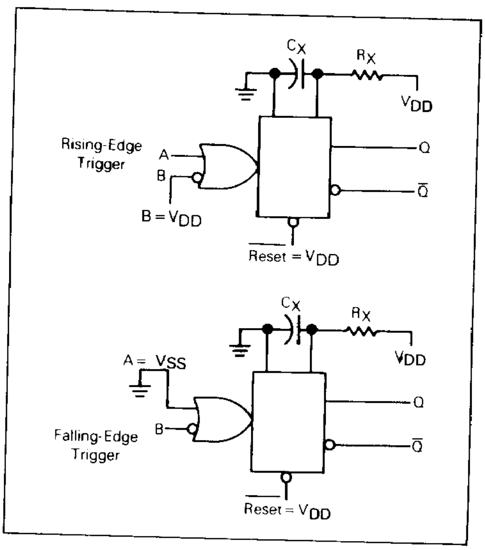
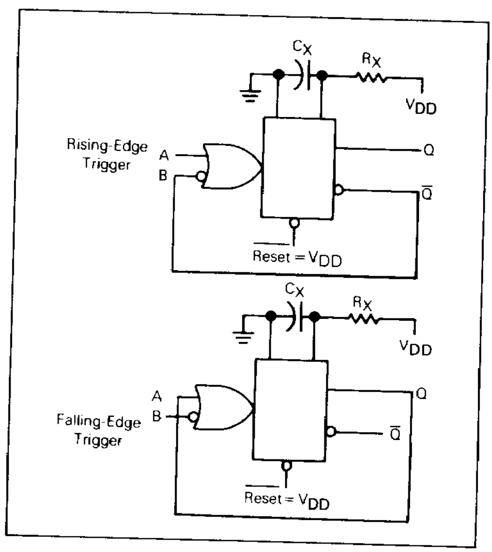


FIGURE 5 – NONRETRIGGERABLE MONOSTABLE CIRCUITRY



SWITCHING WAVEFORMS

FIGURE 6

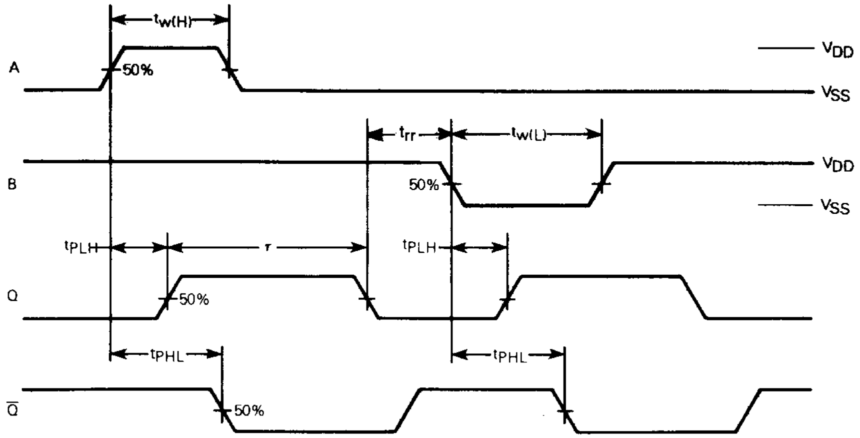


FIGURE 7

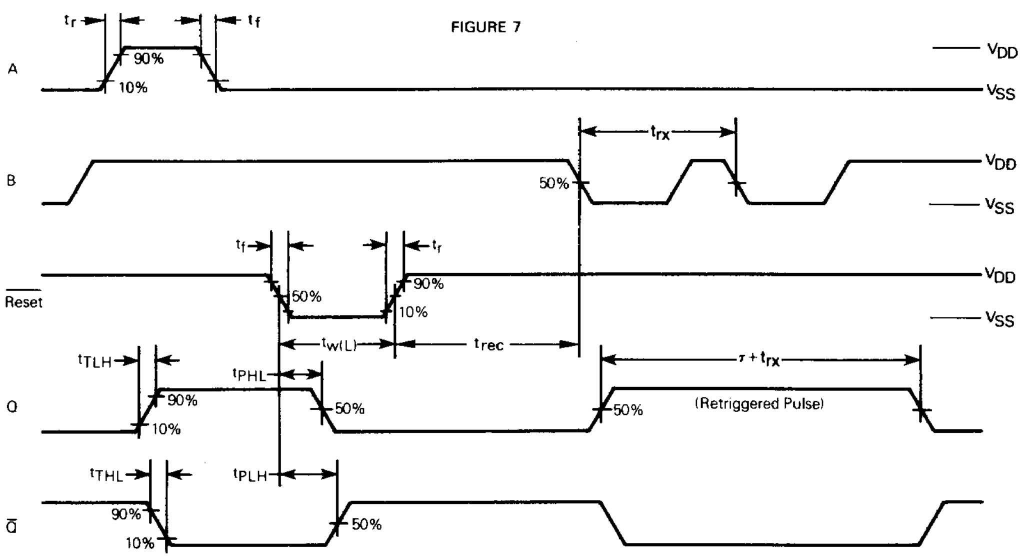
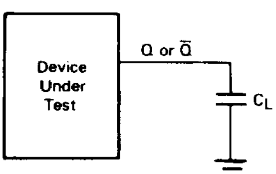


FIGURE 8 — TEST CIRCUIT



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