Version 12.1

Evaluation Guide

Featuring
ACCEL Schematic,
ACCEL P-CAD PCB,
and ACCEL PRO Route

ACCEL Technologies, Inc.

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ACCEL develops and markets design tools to meet the present and future needs of engineering professionals worldwide, who share our passion for innovation, excellence, and exceptional value.

Evaluation Guide Contents

Introducing ACCEL EDA

Thank you for taking the time to review this evaluation of ACCEL EDA, the premier schematic entry and printed circuit board design system for the professional designer. This guide is intended for designers having any level of Electronic Design Automation (EDA) tool experience; from the novice to the experienced user.

As a second generation Microsoft® Windows™ product line, ACCEL EDA is well-founded in a comprehensive specification based on years of research, field testing, and customer input. With roots in the popular P-CAD and Tango products, ACCEL EDA provides versatility and extensive functionality in a logical, easy-to-use manner. We think you'll be pleased with the results.

In this guide we've highlighted the user interface, basic editing commands, and some advanced design features. Should you wish to explore further, check the on-line help with hypertext cross-references and search facility.

The bottom line for measuring the worth of electronic design tools is whether they enable you to create quality designs in less time -- in other words, do they make you *more productive*? We're confident ACCEL EDA does the job. And by testing the software in this evaluation package, you can judge for yourself. So without further commercial interruption, here's ACCEL EDA.

The ACCEL EDA system

ACCEL EDA for Windows is a complete printed circuit board design tool suite with the following components:

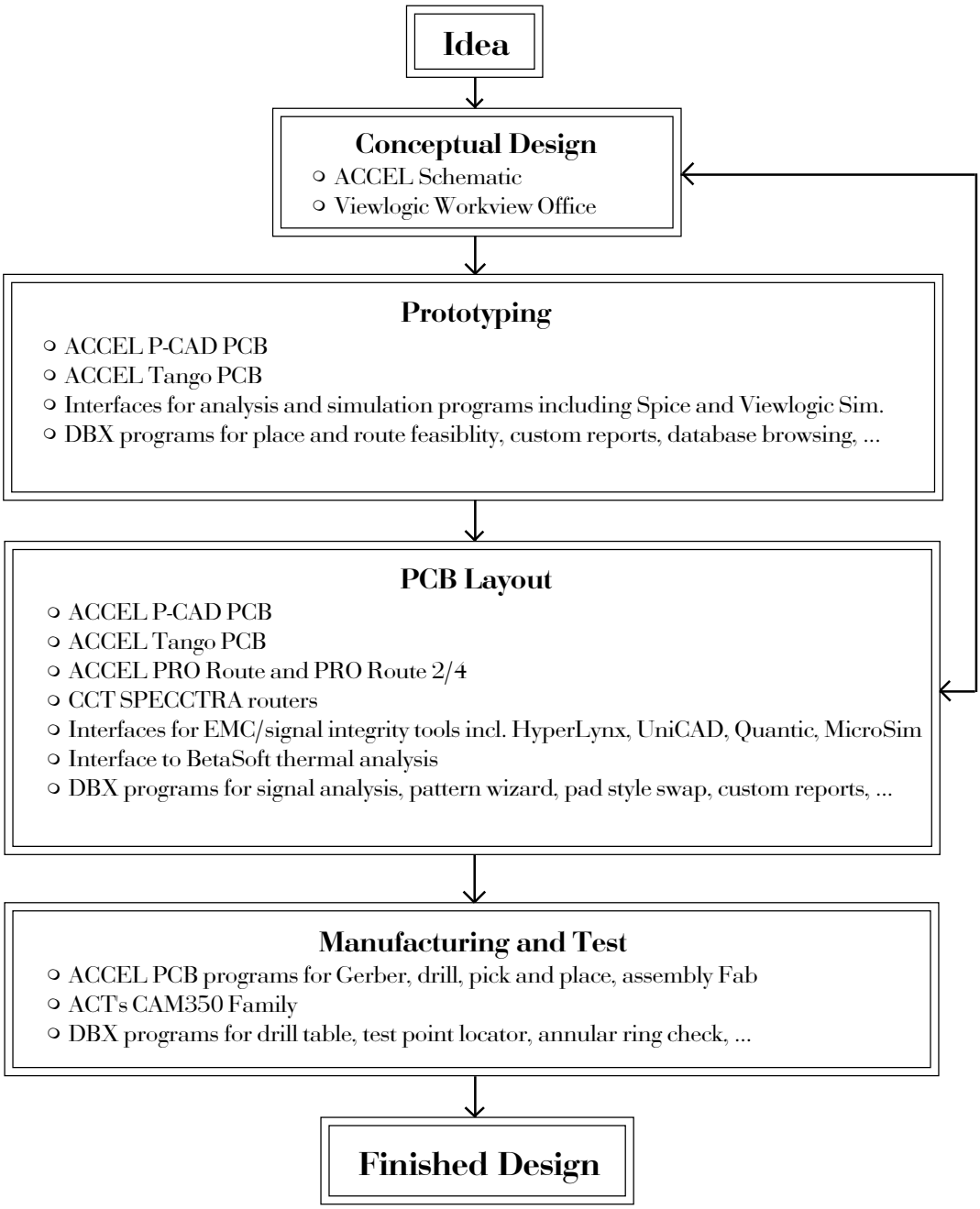
- **ACCEL Schematic:** ACCEL Schematic is an advanced schematic-entry program. It seamlessly interfaces ACCEL EDA's PCB applications, sharing component libraries, passing net and component data forward, and receiving ECO data back from the PCB layout program.
- **ACCEL P-CAD PCB:** ACCEL P-CAD PCB is the design editor within which components are placed, connections are made, routing is completed, design rule checking is performed, and artwork and CAM files are generated. Includes a built-in maze autorouter, QuickRoute, and an interactive shape-based routing tool, InterRoute.
- **ACCEL PRO Route:** ACCEL PRO Route is an optional, high-completion, rip-up and reconstruct autorouting engine that operates seamlessly from within ACCEL P-CAD PCB.
- **ACCEL Library Manager:** ACCEL Library Manager is used to manage the symbolic, physical, and electrical data of ACCEL EDA's integrated components. It is supplied with ACCEL Schematic and ACCEL PCB.

ACCEL Tango PCB is the streamlined version of ACCEL P-CAD PCB, available to address the needs of 80% of all designers. Built with the same user-friendly interface described in this guide, it is priced to be an exceptional value. **ACCEL PRO Route 2/4** is a cost-effective alternative of ACCEL PRO Route for designs with up to 4 signal layers and 4000 pins, or those up to 2 signal layers with no pin limit.

ACCEL also offers high-end **SPECCTRA** autorouting and placement tools, an interface to **Viewlogic** engineering tools, the **CAM350** Family of CAM tools, floating network licenses, an application programming interface (API), and several translators to meet your special needs for designing today's PC boards.

Together, ACCEL EDA applications provide the flexibility and power needed to meet your most challenging design requirements.

From concept through finished board, ACCEL EDA offers a complete solution for your design needs:



Evaluation version limitations

The software included with this evaluation package is the real thing with these exceptions:

- Design work cannot be saved or copied to a file.
- You can only generate output (specifically prints, plots, schematic netlists, and DXF) for files that have not been edited with the eval version. Gerber photoplot output cannot be generated.
- Database exchange (DBX) functions are disabled.
- Cut and copy functions are disabled.
- For routing, ACCEL PRO Route checkpointing is disabled and you cannot save the output or restart that router. You cannot edit or save SPECCTRA Do-Files or start the SPECCTRA software.
- A subset of library components is distributed and some sample files are missing. Additional files can be accessed by calling either of our bulletin board systems at 619 554-1018 or 408 271-1413 and downloading PRODEMOS.ZIP. Settings are automatically detected.
- The eval is unsecured and may be freely copied.

Otherwise, you have access to the functionality in the full ACCEL EDA package. We encourage you to try out as many features as time permits.

Using this guide

This guide leads you through installation and evaluation of the ACCEL EDA product line including schematic, PCB, and routing applications. You would benefit by going through the entire document in order. However, if you are interested in reviewing only one or two of these products, or already own ACCEL EDA, you can save time by referring to the relevant sections.

If you're not already an ACCEL EDA user, you'll want to go through Sections 2 and 3 to learn the fundamentals of the ACCEL EDA family of products. We've kept the user interface information generic so either ACCEL Schematic or ACCEL P-CAD PCB can be used to follow along. ACCEL EDA users can bypass these sections; the basics don't have to be relearned because the interfaces are so similar!

Following the basics, Sections 4, 5, and 6 focus on Schematic entry, PCB design, and autorouting, respectively. You can head directly to the sections that pertain to your interests and skip the others. *Linking the Pieces* is covered in Section 7 and is of interest to both Schematic and PCB designers.

The final section, *Taking the Next Step*, is for everyone. It concludes the evaluation and directs you toward the next step.

Let's get started!

SECTION 1

Installation and Setup

This section covers the required hardware and software necessary for installation, and shows you how to install the ACCEL EDA programs.

We assume you are already familiar with the basic layout and operations of Windows.

System requirements

Be sure that your PC (or compatible) and its software conform to the following ACCEL EDA requirements and recommendations:

- A 486 or later processor running at least at a 33 MHz clock speed is required; 66 MHz or more is recommended.
- Microsoft Windows V3.x, Windows 95, or Windows NT operating system.
- 16 MB of RAM is required, more if you are running an autorouter.
- CD-ROM drive.
- A hard disk is required. Space used depends on programs installed and is indicated during the installation procedure.
- A Microsoft (or compatible) mouse is required.
- A VGA (or better) graphics card is required. Color is recommended.
- *share.exe* must be loaded to run the Library Manager under Windows 3.x. See your Windows manual for information on installing it from within your *autoexec.bat* file.

1. Start Windows and display the Program Manager utility.
2. Insert the ACCEL EDA evaluation CD into your disk drive.
3. From the Program Manager in Windows 3.x or NT, select Run from the File menu to display the Run dialog box

   or

   if you are using Windows 95, choose the Run command after selecting the Start button.
4. In the edit box, type

   ```
   d:\setup
   ```

   where d: represents your CD drive letter. Click **OK**. The ACCEL EDA installation utility will begin. Just follow the on-screen instructions.

New users should at least install ACCEL Schematic or ACCEL P-CAD PCB since either can be used to learn the program fundamentals presented in Sections 3 and 4. ACCEL Schematic, ACCEL P-CAD PCB, or the Library Manager may be installed alone or in any combination. However, because autorouting is invoked as a PCB command, you must install both ACCEL P-CAD PCB and ACCEL PRO Route to evaluate the autorouter.

Note to ACCEL EDA users

If you are already an ACCEL EDA user and are installing this software to evaluate another application, be sure to install the eval in a directory other than where your full copy of ACCEL EDA resides. By default, the evaluation is installed in a separate directory so the production version is not overwritten.

If you own ACCEL PCB and want to evaluate the autorouter, you must install the evaluation versions of both applications. The eval version of ACCEL PRO Route will *not* operate with a licensed version of ACCEL PCB.

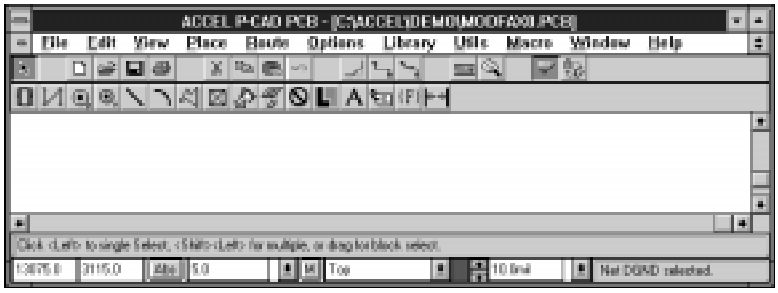
SECTION 2

ACCEL EDA Basics

In this section, we'll introduce you to ACCEL EDA's user interface and some of the options for customizing the program for your own use. The ACCEL Schematic and PCB interfaces are so similar that you may use either program to follow along.

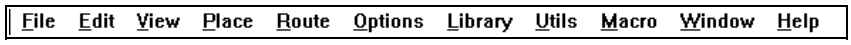
The ACCEL EDA interface

After starting ACCEL Schematic or ACCEL P-CAD PCB you'll notice icons and menu items unique to ACCEL EDA within the standard Windows interface. Application-specific differences exist between ACCEL Schematic and ACCEL PCB (like the tools offered in the Toolbar), but the screens are otherwise the same.



Menu bar

To activate a menu command, click on the menu title or press the *Alt* key in combination with the underlined letter of the title (e.g., *Alt+F* to display the File menu). When the menu is displayed, click on the menu item or press the underlined letter to enable a command. The PCB menu is shown below; the Schematic menu includes the Rewire command instead of Route.



Command Toolbar

The Command Toolbar consists of graphical buttons displayed just below the menu bar or on either side of the screen, according to a setting in the Options Preferences command. These provide direct access to menu commands and other system functions. The Schematic and PCB Command Toolbars follow in order. See your ACCEL Schematic and ACCEL P-CAD PCB Quick Reference Cards for more details.

The buttons correspond to the following actions:

 Edit Select

 File New

 File Open

 File Save

 File Print

 Edit Cut

 Edit Copy

 Edit Paste

 Edit Undo

 Rewire Manual (Schematic)

 Utils Rename Net (Schematic)

 Edit Measure

 View Zoom Window

 Utils Record ECOs

 Route Miter (PCB)

 Route Manual (PCB)

 Route Interactive (PCB)

 Enable Online DRC (PCB)

Placement Toolbar

The Placement Toolbar provides shortcut access to ACCEL EDA's placement commands. Using the Options Preferences command, you can locate this Toolbar vertically on the left or right of your display or horizontally below the Command Toolbar. The Schematic and PCB Placement Toolbars follow:

 -Schematic

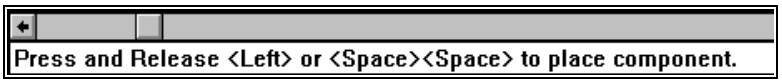
 -PCB

See your ACCEL Schematic and ACCEL P-CAD PCB Quick Reference Cards for more details. The buttons correspond to the placement of the following items:

	Part (Schematic)		Field
	Wire (Schematic)		IEEE Symbol (Schematic)
	Bus (Schematic)		Component (PCB)
	Port (Schematic)		Connection (PCB)
	Pin (Schematic)		Pad (PCB)
	Line		Via (PCB)
	Arc		Copper Pour (PCB)
	Polygon		Cutout (PCB)
	Reference Point		Keepout (PCB)
	Text		Split Plane (PCB)
	Attribute		Dimension (PCB)

Prompt line

The Prompt line lies below the work area and scroll bar, extending the width of the ACCEL EDA display. When there is no prompt, the area is empty.



Status line

The Status line features are as follows, from left to right:

- X and Y coordinate edit boxes
- grid toggle button, edit box, and select button
- default macro record button

- schematic sheet or PCB layer combo box, select button, color block (click it to quickly access the Options Sheet or Options Layers dialog box), and scroll buttons
- line width edit box and select button
- Status line information area

A new X and Y coordinate, grid, and line width can be set by typing into the corresponding edit boxes. This is a speedy way to get to an exact location or create a new grid or line width.

Keyboard basics

ACCEL EDA also supports keyboard operations, including shortcut keys, for those leery of electronic rodents. The ACCEL EDA keyboard shortcuts are listed on the Quick Reference Cards provided with this evaluation. You can also place objects using only the keyboard. The following are keyboard equivalents of actions otherwise performed with the mouse:

Access the menu:	Press *Alt* and the underlined letter shown on the menu bar
Execute a command:	Choose the underlined letter for the command
Dialog box operations:	Press the *Tab* key to cycle through dialog controls; *arrow* key to move within a control; *spacebar* to toggle a checkbox or make a selection
Move cursor 1 grid point:	Press the *arrow* keys
Move cursor 10 grid points:	Press the *Ctrl+arrow* keys
Mouse down (click):	Press *spacebar* once
Mouse down and up: (click and release)	Press *spacebar* twice
Terminate a command:	Press *Esc*

Loading a file

Like most Windows applications, the File New command starts a new design and File Open is for loading an existing file. You can also read Tango-Schematic and Tango-PCB PLUS designs directly into ACCEL EDA once your DOS libraries are translated using the Library Manager's Library Translate command.

drag and drop file loading

As an alternative to File Open, save time with the *drag and drop* method of loading a file. Using Windows File Manager or Explorer, click on the filename icon of a design file in the eval's Demo subdirectory (e.g., `c:\acceval\demo\digdemo.sch` for Schematic, or `c:\acceval\demo\accsampl.pcb` for PCB), drag it into the ACCEL EDA window, and release to drop it. The design file will open. This method works to open design files (.SCH or .PCB), library files (.LIB), and netlist files (.NET).

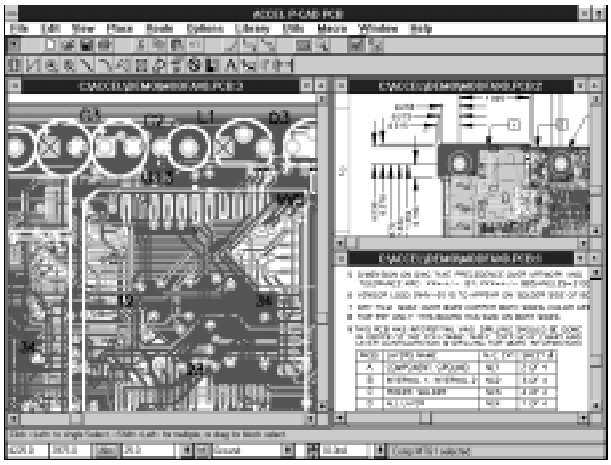
working with PDIF files

P-CAD binary or PDIF files can be imported using the File Open and File PDIF In commands respectively. For more details see Appendix A or B on Using P-CAD Files.

Multiple document interface (MDI)

ACCEL EDA has a built-in Multiple Document Interface (MDI) capability for maximum flexibility in viewing your designs.

1. Open an additional file. To open a new view of the current file, choose the Window New Window command. Notice that all of your open windows are listed at the bottom of the Windows pull-down menu. You can set any window to be the current window by choosing it from this list.
2. Cascade the open windows by using Window Cascade. Use the standard Windows interface to move, resize, minimize, maximize, close, or make any of them current.
3. Next run Window Tile to set up for viewing the windows.



MDI lets you view multiple designs at the same time - cut/copy/paste between them for fast editing (licensed version only)

Zoom commands

Zooming comes in handy while placing components, routing connections, or otherwise working close-up on your design. ACCEL EDA offers several options for controlling how much of the design you see and what parts are visible.

(View) Zoom In/Out

Move the cursor to any area on the sample board and choose the View Zoom In and View Zoom Out commands from the menu, or press the *plus* (*+*) key to zoom in and the *minus* (-) key to zoom out. The **Zoom Factor** value in the Options Configure dialog determines how much the display is changed. Use Options Configure to modify this value and try zooming again.

(View) Zoom Window

With Zoom Window, you can zoom into any area of the workspace. Invoke this command with the *Z* key, the Toolbar zoom button, or the View Zoom Window menu command. Click and drag the cursor to define a viewing window. Release the button and the window you designated will fill the workspace.

other View options

You may want to experiment with a number of the other options available on the View menu, such as View Center (the *C* key) and View Extent. These will respectively center the view at the cursor location and cause the display to encompass all items in the workspace. You can pan across the workspace by repeatedly moving the cursor and pressing *C*. When using *arrow* keys, the screen automatically pans when moving your cursor to the screen's edge. The screen is shifted by the **Autopan (% Display)** amount set in Options Configure. Toggle between the last two "views" of the design by using the View Last command. And, the entire workspace becomes visible with View All.

Customized shortcut keys

Choose the Options Preferences command and take a look at how much control you have over configuring your keyboard shortcuts. Keys, including those you just used for zooming, can be assigned to menu commands, many special actions, and macros. ACCEL EDA ships with default settings which can be modified to match your preferences.

Next we'll assign the Redraw command to a function key. Here's how: With the **Menu commands** radio button selected, choose

View Redraw from the combo box on the left. Click in the **Press a Shortcut Key** box and press the *F1* key on the keyboard. A message displayed below the shortcut box indicates the key is already assigned: *Current Binding: Help Contents*.

Assigning *F1* to Redraw would delete the current assignment. Instead, press *F3* (which has no other assignment) and click the **Assign** button to bind *F3* to the command.

These shortcuts are saved in a key file that can be recalled at any time by pressing the **Key File** button and entering the file name. This allows settings to be shared or carried to other machines.

Complete Imperial and metric support

ACCEL EDA supports metric and Imperial units, and accurate conversion between them. To change your global design units at any time, choose Options Configure and select mils, millimeters, or (in Schematic) inches in the **Units** box. Toggle between **mils** and **mm** to see how the workspace size is automatically converted.

ACCEL EDA intelligently handles units of measure. All data throughout the system is presented in the chosen global units, and any data you input is assumed to be in those design units. However, you can always override the units by appending a suffix (with no space) to the value; **mm** for millimeters, **mil** for mils, **in** for inches. For example, if your design units are millimeters, you might specify `100mil` in a dialog box. This value would be converted and displayed as 2.54 millimeters.

measure-ment tool

To measure distances in your design, choose Edit Measure from the menu or click on the Toolbar button. Click on the starting point but don't release the mouse. As you move the cursor notice x, y, and total distances are provided on the Status line.

ACCEL EDA's 32-bit database precision assures absolute accuracy whether using Imperial or metric units.

Styles

The concept of using styles in software is not unique, but it does require some explanation. A *style,* in ACCEL EDA, is a named combination of properties defining an object. For instance, text is characterized by a font and the font's size. ACCEL EDA's *(Default)* text style is a stroke font that is 100 mils high. When this style is active and text is placed, the text is created using that 100 mil stroke font. Pads and vias are also defined by styles in ACCEL EDA. Pad shape and size per layer, drill hole data, and plane swell are all defined by the pad's or via's style.

styles are applied to any number of similar objects

A new style must be created and named the first time a particular combination of properties is needed. Default text, pad, and via styles are provided for your convenience. The default for each is used unless you create a different style and set it to be current. The current style is applied to objects as they are created. Placed objects can be later modified to have a different style.

using styles simplifies global editing

Except for pre-defined styles, styles themselves can be redefined. This powerful feature must be used with caution. Changing a style's properties affects each object using the style!

Styles are created, modified, deleted, and set current in the Options (Text/ Pad/ Via) Style commands. You'll get a chance to use pad and via styles in the PCB Design Session.

Setting grids

Whether you are running ACCEL Schematic, PCB, or Route, correct grid spacing is important for placing objects in your design.

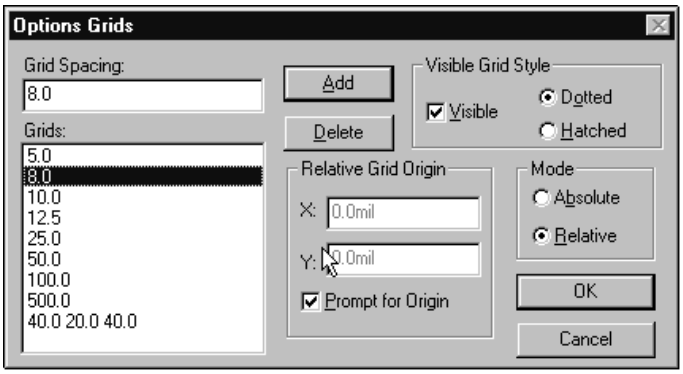
Use the Options Grids command to set the current grid for your particular requirements: perhaps 2.54 mm spacing for easy alignment of your metric Schematic symbols, or 50 mils for placing your surface mount PCB components.

To set a new current grid, choose **Absolute** Mode, then select a grid from the **Grids** list and click **OK**. If the desired spacing is not shown, type a new value in the **Grid Spacing** box and click **Add**. The Status line reflects the change.

You can also set or change the settings for relative grid mode. Whereas the absolute grid origin is always the bottom left hand corner of the workspace, the relative grid origin can be located anywhere. A relative grid is particularly useful for locating objects in relation to a datum point.

We've already mentioned you can also toggle the grid mode and select or add a new grid spacing directly from the Status line. Although direct access will probably become your preferred method of grid selection, the Options Grids command dialog box includes some additional features.

select relative or absolute grids for placement and routing with the Options Grids command



Notice you can also control the grid visibility and style, delete a grid, and define the relative origin from within the dialog.

Component libraries

In ACCEL EDA, a component is a collection of data including electrical information (e.g., pin designator, pin name, "swap-ability"), a symbol for use in Schematic, and a pattern for use in PCB. The ACCEL Library Manager manages and integrates component data for use by both Schematic and PCB.

Thousands of components are organized into libraries and shipped with the software. As described in Section 7 of this guide, you can also create custom components.

We won't go into detail on this now, other than to say that parts in Schematic and components in PCB are placed from libraries, and libraries must be opened prior to placement.

section review

In this section you have seen:

- The ACCEL EDA user interface, including a tour of the screen, menus, and keyboard operations.
- How to load files.
- How to display multiple views of multiple designs.
- The various zoom options for viewing the workspace.
- How to customize your keyboard for taking shortcuts.
- How to mix Imperial and metric data.
- How styles are used.
- How to set up grids.
- Component libraries.

We'll now move on to cover the basics of placing, selecting, moving, changing, and deleting objects in a design.

SECTION 3

Placing, Selecting, and Editing Objects

This section introduces you to the ease of placing, selecting, moving, and modifying objects in ACCEL EDA.

why it's so easy to use

ACCEL EDA was designed for efficiency. You can initiate object placement directly from the Toolbar without extra key strokes or mouse clicks. Then, when you need to move, edit, or delete any combination of placed objects, select them and do it!

Pop-up menus, keyboard shortcuts, context sensitive editing, and the editable Status line all contribute to letting you concentrate on your work without wasting time weaving through commands.

Placing objects in ACCEL EDA

Place commands allow you to either draw new objects or place already created objects, such as components, into your design.

The items that can be placed in your design are those listed in the Place menu. Objects common to Schematic and PCB are **Line, Arc, Polygon, Text, Attribute**, and **Field**. In ACCEL Schematic you can also place a **Part, Wire, Bus, Port, Pin, Ref Point**, and **IEEE Symbol**; and using ACCEL P-CAD PCB you can place a **Component**, **Connection, Pad**, **Via**, **Point**, **Copper Pour**, **Cutout**, **Keepout, (**Split) **Plane,** and **Dimension**.

All objects can also be placed using the Placement Toolbar. Icons are in the same order as listed in the Place menu. Toolbar visibility is controlled with the View Placement Toolbar command. Choose the **Toolbars** tab within the Options Preferences dialog box to display the Toolbar along the top or either side of your design.

options during placement

During placement, certain actions are available depending on the type of object being placed. These include zooming, moving, rotating, and flipping objects (e.g., text, parts, pins, pads, ports, components), unwinding (i.e., erasing segments of polygons, copper pours, split planes, wires, buses, lines, manual routes), and changing the center point of an arc before placement is final.

undo

Undo saves the day!

There's no need to worry if you goof during placement, or while performing just about any other action for that matter, because ACCEL EDA comes with Undo. Your last operation is undone in a single step by selecting the Edit Undo command, clicking the Undo Toolbar icon, or pressing the *U* key. It's that easy!

ACCEL EDA supports one level of undo. Placements, deletions, and changes can all be undone, and you can even undo an undo.

hands-on practice

The following are some simple step-by-step exercises in placing various objects, using some of the placement options. Since ACCEL Schematic and ACCEL P-CAD PCB operate the same way, you can use either application to practice.

If ACCEL EDA is not already running, start either ACCEL Schematic or ACCEL P-CAD PCB by double-clicking the application's icon. Otherwise, use File New to start a new design. In either case, maximize the window to fill the workspace. Zoom in a bit and try the following placement exercises.

exercise #1: placing lines

Lines are non-electrical entities, used for creating board outlines, symbols and patterns, and annotating your designs.

1. First create a new sheet or layer. Choose Options Sheet (Schematic) or Options Layers (PCB). Enter a new name and, for PCB only, a new number, type, and bias. Then choose **Add**. Notice your new entry is added to the list box. Make it current by choosing the **Current** button or **Current Layer** combo box, and then close the dialog.

   Choose View Status line if the Status line is not visible. Practice switching between existing sheets or layers using the Select and Scroll buttons on the Status line.

2. To add lines, choose the Place Line command from the Toolbar, menu, or keyboard and move the cursor into the workspace. Click, drag, and release to draw the first segment; repeat the action (or position and click) to draw two

or three more segments. Terminate line creation by pressing *Esc* or the right mouse button.

change line settings during placement

3. Use Options Current Line to change the default line width or style. Alternately change the width by typing directly into the width edit box on the Status line or choosing from the Status line's width combo box. Start your next line; just click and drag in the workspace. Subsequent lines are created with the new setting. The width can be changed after any segment is placed, before terminating the line.

line length is dynamically calculated and displayed on the status line

4. Watch the Status line information area (lower right corner of the screen) as you draw line segments; the delta-X and -Y measurements are given while you drag a segment, and the total line length is given when you complete each segment.

orthogonal modes make placing complex lines easy

5. ACCEL EDA supports several orthogonal modes. While drawing a diagonal line segment (and before the left mouse button is released), press the *O* key to toggle through the options. Once you get to the orthogonal shape you like, press the *F* key to flip the line. In PCB, the arc is only supported for manual routing, not for placing lines. Enable and disable modes using the Options Configure command.

unwind unwanted line segments during placement

6. Before completing the line, press the *backspace* (unwind) key ←, and the previous segment disappears. Add or unwind more segments, then complete the series of segments with a right click. For practice, press *U* once to undo the entire line, and again to bring it back.

exercise #2: placing arcs and circles

Arcs are partial circles, and a circle is defined as a 360 degree arc. Like lines, arcs are used for non-electrical purposes.

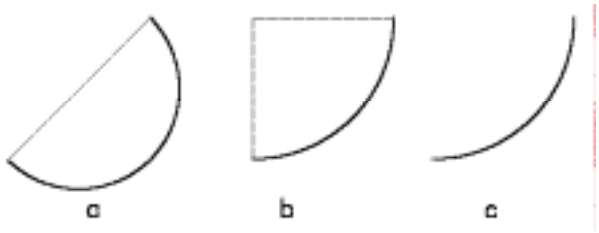
The Options Current Line command is used to establish the width setting for arcs. You should also note that in PCB arcs differ from current-carrying curved tracks which are created while routing with the manual routing tools.

Arcs are constructed counter-clockwise; an initial click (down), drag, and release (up) define the start and end points of the arc. A second click and drag allows you to move the center point, effectively changing the arc's radius and sweep angle.

To create a full circle, the first click and release should be at the same point (with no drag), along the X-axis of the desired circle.

The circle's center point is then defined by clicking a second time and dragging the mouse horizontally.

1. Choose the Place Arc Toolbar button or menu command.
2. Move the cursor to a grid point in your workspace. Click and drag the mouse at a 45-degree angle towards the upper right of the workspace, then release. The unfinished arc should look like **a** in the diagram below. Press the *F* key to see how to flip the arc. Press it again to return to **a**.
3. Click over the center point and drag it towards the upper left to form a 90-degree corner as shown in **b**. Release and notice that you have created a 90-degree arc, like **c**:



4. Create a circle by clicking and releasing without dragging the mouse. Click a second time and drag to the right and left to see how the size of the circle changes.

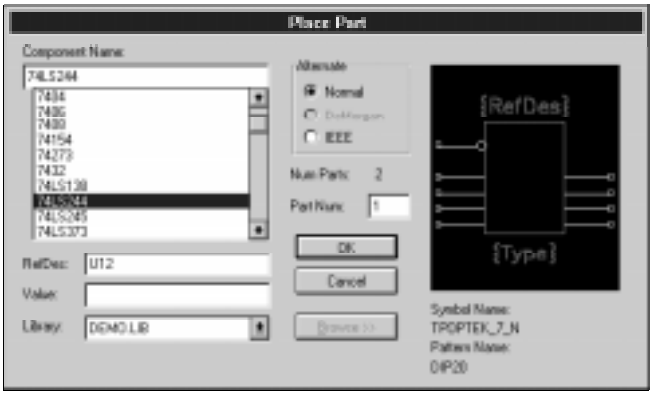
exercise #3: placing parts and components

Schematic part symbols and PCB component patterns are placed similarly, from an integrated library. ACCEL EDA's libraries contain information for both applications.

1. Choose the Library Setup command to open a library. Click **Add** and select DEMO.LIB from the eval's Demo subdirectory, then close the dialog box by clicking **OK**.

2. Choose Place Part (Schematic) or Place Component (PCB) from the Toolbar or menu. Click left in the workspace. A dialog box lists available components or parts. Choose **Browse** to view each item graphically (only displayed if a symbol or pattern is defined for the component).
3. Scroll through and click on any name listed in the box. Specify a **RefDes** if desired, and click **OK**. Then click left in the workspace and *hold* down the mouse button.

browse library parts prior to placing them in ACCEL Schematic



a single keystroke rotates or flips parts and components during placement

4. While holding the button down, press *R* to rotate the item 90 degrees counterclockwise. In the PCB Design Session section you'll learn how to rotate to other angles. Press *F* to flip the object and, finally, release the mouse to place it.

   Each new click places another object of the same type and orientation. It can be moved, rotated, and flipped as well. Notice on the Status line that the RefDes is automatically increased by 1 each time. Press *D* before placing another object to increase the RefDes; *Shift+D* to decrease it. In Schematic, *P* increases the part number on multi-part packages; *Shift+P* decreases it.

   The *Esc* key or right button ends the placement of a particular object. Click the left button again to display the dialog, and select a different part or component to place.

exercise #4: try placing some other objects

Now let's try placing the remaining objects, briefly described below. All are accessible from the Toolbar, Place menu, or keyboard. Follow the Prompt line and use the Help command if necessary. The *F* and *R* keys flip and rotate many objects during placement. In PCB, items can be rotated to 0.1 degree precision.

The following objects can be placed in both Schematic and PCB:

- The **Ref Point** command in ACCEL Schematic is used for placing reference points when you are creating new symbols. Click the left mouse button, drag to the desired location, and release to place the point.

  Point is the corresponding command in PCB. Use it to place reference points, glue dots, and pick-and-place points on new patterns as you create them.

- A **Polygon** is a filled, multi-sided entity without net data. Create one just like you created the multi-segment line. It is filled when *Esc* or the right mouse button is pressed.

- **Text** is free text in a design. Click in the workspace to view the dialog box for assigning text, orientation, and style.

- An **Attribute** is an entity with an assigned value, placed globally or as part of a component, part, or net. To place a global attribute, click in the workspace. Component, part, and net attributes are accessed through the object's Properties dialog (double-click the component, part, or net). In either case, select a category and pre-defined attribute name from the list boxes, or enter a new user-defined name. Add a value or leave it blank to be entered later.

  All attributes and their values can be set in the schematic and transferred to the PCB via the netlist. They play an important role in ACCEL EDA's *correct by design* philosophy, and are covered in more detail in the schematic and PCB sections that follow.

- A **Field** is an item that is updated automatically. The **Current Date**, **Current Time**, **Current Sheet**, **Number Of Sheets**, and **Filename** fields are maintained by ACCEL EDA. Values for **Author**, **Date**, **Time**, **Revision**, and **Title** fields are taken from the File Design Info command dialog box. Add a few of these fields, then update the data using Design Info. Redraw the screen to see the new values.

Several more objects can be placed in ACCEL Schematic:

- A **Bus** is an electrical item used to carry multiple signals. It is placed like a line. When a wire is placed to start or end on a bus, the net is automatically assigned to the bus and the connection is graphically displayed with a bus entry.

- A **Wire** is an electrical item that defines net connectivity. Place wires like lines, starting and ending on pins, buses, or other wires. Watch the Status line during placement. Default net names are automatically assigned. We'll show you later how to reassign them. A junction is automatically added when a wire starts or ends on another wire. Junction size and the display of unconnected ends are controlled in the **Miscellaneous** box in Options Display.

- A **Port** identifies subnets of logically, but not physically, connecting portions of a single net. Click in the workspace to bring up the dialog for selecting net name and display options. Then click and drag to locate the port on a wire.

- A **Pin** is the part of a symbol used for connecting wires. Use the Place Pin command to place pins during part creation. Click in the workspace and choose the pin characteristics. Click and drag to locate the pin.

- An **IEEE Symbol** is placed by choosing this command and clicking in the workspace. **Adder**, **Amplifier**, **Astable**, **Complex**, **Generator**, **Hysteresis**, and **Multiplier** symbols are available. Symbol size is controlled within the dialog.

These objects are specific to ACCEL P-CAD PCB:

- Place a **Pad** or **Via** freely on the board or as part of a library component pattern. Set the desired style in Options Pad (or Via) Style, then choose the Place Pad or Via icon. Click and drag, then release, to locate the object in the workspace.

- The **Copper Pour** is a solid or hatch-filled polygon placed on a signal layer, with user-defined backoff from all other entities in the area. It can be attached to a net. Pours are often used for shielding. (Wait to try this one, because we'll take a close look at it in the PCB Design Session.)

- A **Cutout** is an area defined within a copper pour that is void of copper. It is placed just like a polygon.

- The **Keepout** (PCB, Route) defines a boundary which the autorouter will not cross. Choose the keepout type and define it for one or all layers in the Options Current Keepout dialog. Create keepouts like lines and polygons.

- A **Connection** defines electrical connectivity between two pads. Click on a component pad, drag to another pad in the same net, and release. Nets can be defined in this way.

- A split **Plane** divides a power or ground plane to allow for multiple net assignments. Splits are created as polygonal areas. Details are provided in the PCB Design Session.

- A **Dimension** is added to annotate the design for manufacturing. Choose this command and click on a line or arc to be dimensioned. Point-to-point, baseline, diameter, center, leader, radial, and angular dimensions are supported.

Selecting objects for action

ACCEL EDA's select tool is the most powerful in the business

We're proud of ACCEL EDA's placement commands and the options, functionality, and interface we provide for creating designs. But it's the strength of ACCEL EDA's "select-edit" methodology that really sets us apart and allows you to complete designs in a more effective manner. When you're ready to move, copy, modify, resize, delete, highlight, or otherwise operate on any part of your design, you simply select objects and do it.

selection methods

A variety of methods are offered to efficiently isolate *exactly* those items you wish to edit. Let's cover these before jumping to the great things you can do with the selected items!

Choose the Select tool from the Toolbar or Edit menu, or by pressing the *S* key. When an object is selected, its display changes to the Selection color set in the Options Display dialog.

the status line identifies selected items

The Status line information area identifies selected items, either specifically (e.g., part #) or generally (e.g., # of items selected).

Zooming can be performed while you are selecting objects, just like during placement. Try pressing the *Z* (View Zoom Window), *C* (View Zoom Center), *+* (View Zoom In), and - (View Zoom Out) keys to adjust your view during selection.

- **single select.** In Select mode, click over a single object to select it. If items are collocated (on top of each other), click at the same location to toggle through the items until the one you want is highlighted.

  In ACCEL P-CAD PCB, item selection is layer-specific. If an item is on a specific layer, then that layer must be current to allow selection. Change the current layer using the Status line layer Select or Scroll buttons. Some items, such as through-hole pads and components, exist on all layers.

it's simple to add to, and delete from, a selection

- **multiple select.** Add items to the selection by holding down the *Ctrl* key and clicking on the additional items. Remove an object from the selection by pressing *Ctrl*+click on it a second time. Use this in conjunction with other selection methods to update the selection list at any time.

Add collocated items to a multiple selection by clicking at the same location to toggle through items until the one you want is added to the selection.

> *Note: The Ctrl and Shift keys used to extend a selection or to sub-select items can be reversed. Locate this option by selecting the Mouse tab within the Options Preferences command.*

sub-selection gives you editing access to the individual parts of an item

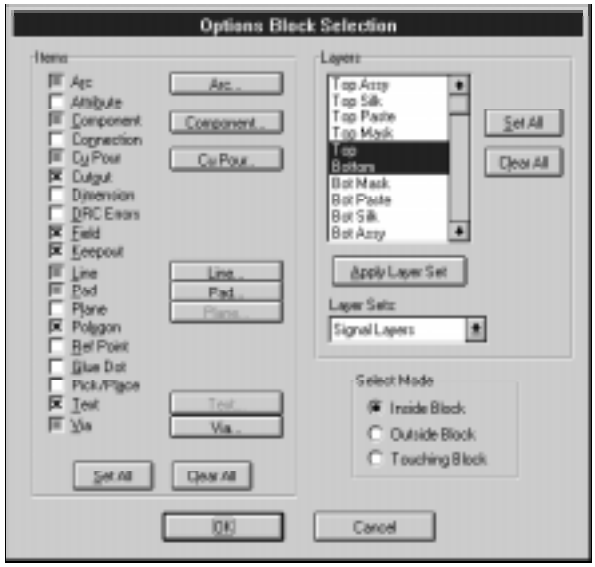
- **sub-select.** Select a portion of an item by holding down the *Shift* key (see note above) and clicking on a sub-item. Try selecting a component pad or pin, a net name, or RefDes.
- **block select.** To select a block of items, click and drag to create a *selection box* to surround the desired objects.

Block selections are extremely powerful because of the variety of ways you can include or exclude specific types of objects in the selection. This filtering is controlled from the Options Block Selection dialog. Add several text strings using different text justifications and styles to your design. We will select them using the filter.

control the type of objects being selected

Choose Options Block Selection. Checkboxes are available for every object that can be placed. Clearing an object's checkbox excludes that object type from being block selected. Checking the box includes the object type.

perform editing operations on the items of your choice with the block selection filter



Try selecting all text on your current Schematic sheet or PCB design. Click the **Clear All** button and then enable only the **Text** checkbox. In PCB, click **Set All** to enable all layers; block selection looks for items only on enabled layers. Choose the **Outside Block** radio button then click **OK**. Be sure you are in Select mode, then click and drag to define a small selection box, making sure you avoid all text. Practice choosing items inside, outside, and touching a block.

be specific in your selection

Selection of objects with an associated push button (e.g., arcs, lines, text) can be more specifically defined. Try this for text. Choose Options Block Selection again. This time toggle the **Text** checkbox to be gray, which enables the **Text** push button. Click this push button. Set the Text Selection Mask to match some text in your design, then block select only that text. Try again by specifying different justifications or styles. ***Remember to reset your block selection options before trying to block select other objects!***

a single command finds all items in a net

- **select net.** Place a few wires or connections in your design and try selecting an entire net (use the Place command to add parts or components, then again to add the connections or wires). Select one item in the net, click right, and choose **Select Net** from the menu. The entire net will be selected.

- **edit nets.** Use the Edit Nets command to select nets by their name. Choose one or more net names from the list box and then click the **Select** button.

- **select nets by node count.** To select nets with a given number of nodes, choose the Edit Nets command from the menu, or select a net and pick the command from the right mouse pop-up menu. Enter the desired **Min:** and **Max:** node count, then press the **Set Net By Node Count** push button. All nets with the correct number of nodes will be highlighted in the list box. Press the **Select** button and these nets will be selected (it will be grayed if no nets match the node count).

- **select contiguous.** (Schematic only) In the Schematic Design Session we'll show you how to create wires that are not physically connected, but carry the same signal. This is important for global nets such as power or clock lines. To choose only the physically connected wires (i.e., a sub-net), the

Select Contiguous option is available from the right mouse pop-up menu when a wire is selected. We'll try this out later.

- **select all.** Use Edit Select All to select all items on a Schematic sheet or in a PCB design.

restart the selection list by deselecting

- **deselect.** Click on an empty area to deselect all items. You are still in Select mode, but no objects are selected.
- **deselect all.** Use Edit Deselect All as an alternate way to deselect all items.

Editing actions on selected objects

You are now ready to operate! Actions on selected objects can include the following, but depend on the type of item selected:

- delete
- move
- rotate and flip
- resize
- cut, copy, and paste
- modify
- obtain net information
- duplicate in a matrix
- align parts or components
- move by reference designator
- move to layer (PCB only)
- explode or alter parts and components
- cross probe between applications

Except for the last three items, we'll briefly examine each of these operations here. Feel free to explore more on your own.

right-button is the shortcut to editing selected items

The right mouse pop-up menu provides direct access to the most common commands performed on selected objects. The list is *context sensitive*, meaning the actions presented are appropriate for, and apply to, the selected objects. Here's the menu presented when a part or component is selected and the right mouse button is clicked.

context sensitive pop-up menus give direct access to common commands

delete

To delete selected objects, use the Edit Delete command, press the *Del* key, or click the right mouse button to bring up the handy pop-up menu, and select the **Delete** option.

move

After items are selected, move the objects by clicking within the selection box and dragging to the new location, then releasing. It's that easy... click, drag, and drop.

ACCEL EDA Tip

If you are concerned about the accuracy of moving items while holding down the left mouse button (or if you just have a lazy index finger), you can use the spacebar instead of the left mouse button, as follows:

- one stroke *spacebar* = mouse button down (for dragging)
- two strokes *spacebar* = mouse button down *and* up (click and release).

You can also use the *Alt* key to free your index finger. Press the *Alt* key, click the left mouse button, and release the *Alt* key; you can then move the object anywhere without having to keep the mouse button depressed.

rotate and flip

Press *R* to rotate your selection 90 degrees counterclockwise. Connectivity of net items (e.g., wires, traces) is maintained. In the PCB Design Session, you'll see how to rotate by 0.1 degree. To flip your selection in the X direction (about the Y- axis), press *F*. That makes flipping an object easier than tipping a cow, and a whole lot safer!

resize

Resize an object by picking one of its handles and dragging to stretch the object. Handles are the squares displayed when certain objects are selected singly.

resize handles on an arc make it easy to change the sweep angle

For example, after selecting an arc, pick one of its endpoint resize handles and drag it to change the sweep angle. To resize a polygon, grab any vertex handle and move it to a new location.

cut, copy, and paste

For copying within the same design, you can use the shortcut *copy drag-and-drop*, which is available in this eval. Select one or more objects then *Ctrl*+click left over the selection and drag to where you want to place the copy. Release to fix the object(s) in the new location.

easily copy part of one design into another

Although this evaluation software does not support cutting from, and pasting to, the Windows clipboard, this valuable feature is available in the licensed version of ACCEL EDA. It is particularly useful for copying from one design into another. Use the Windows standard accelerator keys (*Ctrl+X, Ctrl+C,* and *Ctrl+V*) or choose the commands from the Edit menu.

include pictures in your design documentation

Graphics are also cut or copied to the clipboard in bitmap form (Windows Metafile format) for pasting into other Windows programs. This feature facilitates design documentation.

modify properties

Once an object is selected, its properties are easily modified. The changes allowed depend on the type of object selected.

What objects can be modified? *Everything except points and IEEE symbols.* Double-click any of these items and an *object* Properties dialog is presented.

Alternately, select one or more objects, click the right mouse button, and choose **Properties.** If multiple items of the same type are selected, all boxes with unmatched values will be left blank or grayed in the Properties dialog. Enter updated information in the dialog box and click **OK**. All of the selected objects will uniformly take on the characteristics (e.g., values) you specified.

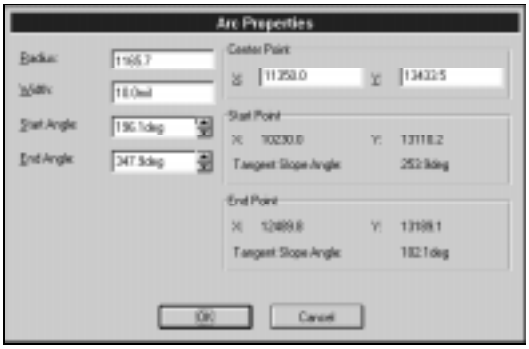
modify line properties

The Line Properties dialog for Schematic is shown below. The line width, style and location can be modified. The PCB lines dialog is similar, but without a style option.

change the line width, style, and location in ACCEL Schematic

modify arc properties

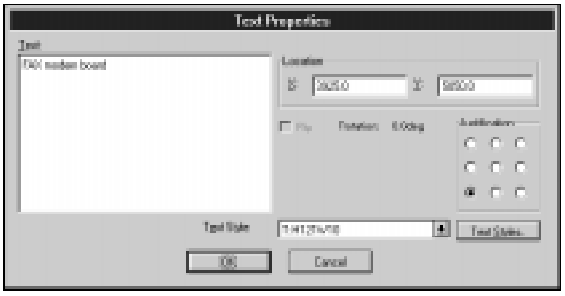
The Arc Properties dialogs in Schematic and PCB are the same, giving you pinpoint control over an arc's radius, width, starting and ending angles, and center point.



modify text properties

From the Text Properties dialog try changing the text contents, justification, and style of some placed text.

change text style, content or justification in the Text Properties dialog box



modify part and component properties

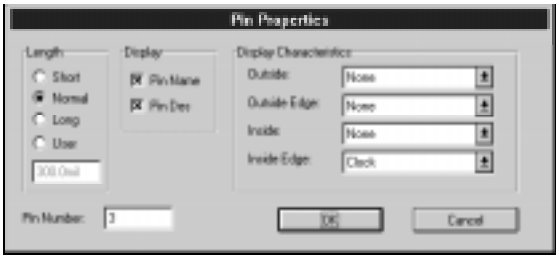
The Properties dialogs for Schematic parts and PCB components allow you to update similar kinds of data. Try changing a RefDes and notice that the display is automatically updated. Additional options are discussed in the Schematic and PCB Design Sessions.

change characteristics of a part with the Part Properties dialog box

modify pin properties

Pins can be changed in a variety of ways using ACCEL Schematic, as seen in the Pin Properties dialog.

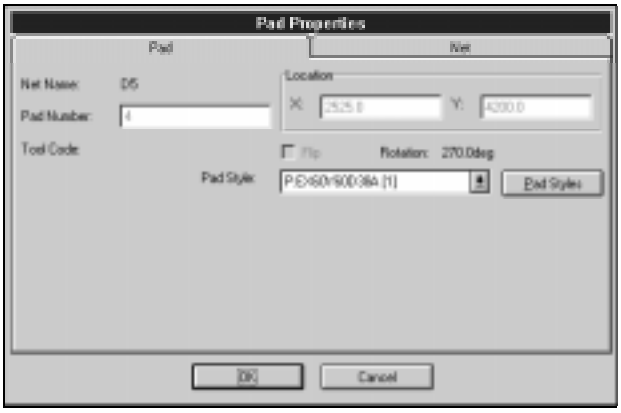
control pin properties from a single dialog



modify pad and via properties

The property dialogs are similar for PCB pads and vias. Select a new style or edit an existing one to modify these objects.

change a pad style in the Pad Properties dialog box



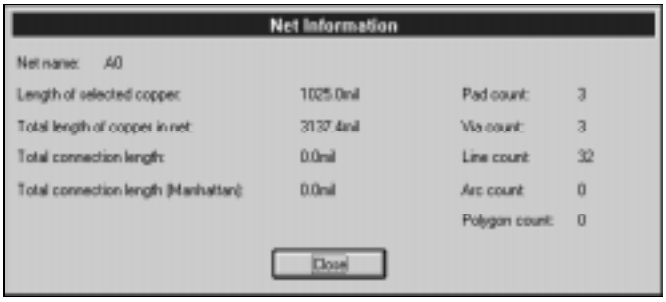
other changes

The visibility of net and bus names, and a port's type and net name are controlled from the Wire, Bus, and Port Properties Schematic dialogs. Also, we'll create and modify a copper pour, split plane, and dimension in the PCB Design Session.

net information

Display the net information of a net object (e.g., wire, via, trace) by selecting it, clicking the right mouse button, and choosing **Net Info** from the pop-up menu. The data provided differs between Schematic and PCB, but you access it the same way.

the Net Information box tells all about a given net in your PCB design

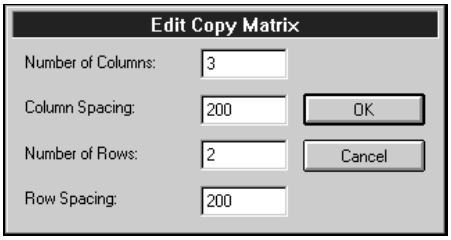


copy matrix

To quickly duplicate selected objects in the X and/or Y direction, use the Copy Matrix command. This command is particularly handy when creating new Schematic symbols or PCB patterns.

The following example shows how a 3 x 2 matrix of pads is easily created when starting with a selection of just one pad. Pins for a symbol can be duplicated in the same manner.

duplicate objects with Edit Copy Matrix



duplication result

alignment

With a single command, you can align placed components or parts vertically, horizontally, to a grid, or to be equally spaced. Select one or more items. Click the right mouse button and choose the **Selection Point** option from the pop-up menu. Press the left mouse and drag to locate a point of alignment. Then click right mouse again and choose **Align**. Set the desired options. Practice using the different options. Alignment onto the current grid can be done without choosing a selection point.

move by RefDes

ACCEL EDA comes with a speedy way to move a part or component if you know the item's reference designator. With the Select Tool active, choose the Move by RefDes command from the Edit menu. After picking the desired RefDes from the combo box, the part or component is selected and placed at the cursor location when you click the left mouse button. Recall you can enter exact cursor coordinates on the Status line and flip or rotate the item with the shortcut *F* and *R* keys.

section review

In this section we have shown you how to:

- Place various objects in your design.
- Select objects using a variety of techniques.
- Edit, move, modify, delete, copy, and perform other operations on selected objects.

Now that you understand the basics of placing, selecting, moving, deleting, copying, and changing objects within ACCEL EDA, you are ready to design a simple Schematic or printed circuit board on your own. In the next section, we'll show you how to put it all together. You're well on your way to sophisticated board designs with ACCEL EDA.

SECTION 4

A Schematic Design Session

With basic ACCEL EDA concepts under your belt, you are now ready to step through ACCEL Schematic to create a small schematic design. In this design session, you will:

1. Set up your design preferences: workspace, display, title block, and libraries.
2. Create a simple schematic with parts, wires, buses, and ports.
3. Learn to work with your design: traverse sheets, locate and modify items, and obtain information.
4. Perform an electrical rules check.
5. Generate output: reports, netlist, and printed artwork.

Setting up your design

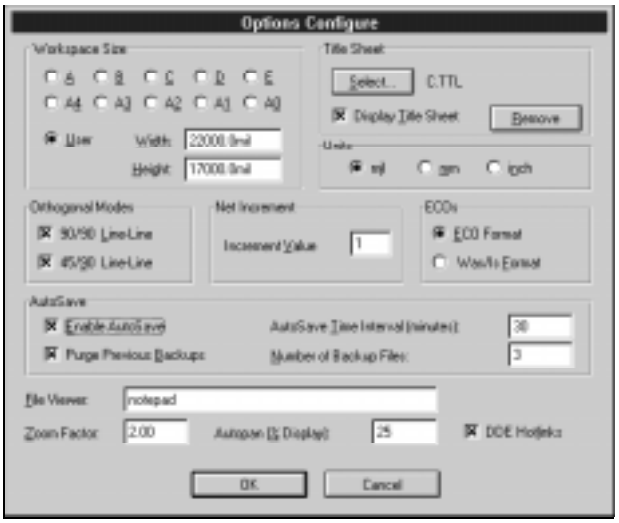
design configuration

After starting ACCEL Schematic, choose the Options Configure command to set up your work area and operating options. For this design, an A-size drawing will be adequate. There's no need to fret over the sheet size decision; at any time just return to Options Configure and select another size. You can even change to a smaller sheet if all the items fit in the smaller area.

Click **A** in the **Workspace Size** box; the **Width** and **Height** are automatically assigned. Click **Select** in the Titles box to choose the `a.ttl` title file, located in the eval's Titles subdirectory (e.g., `c:\acceval\titles`). Enable the **Display Title Sheet** checkbox to make the border visible, if it is not already enabled.

Now is a good time to view the impact of switching units. Toggle between mils, mms, and inches, watching the **Width** and **Height** values change. ACCEL EDA's 32-bit database enables accurate conversion of all data. Set the **Units** to **mils**.

set your configuration options with the Options Configure command

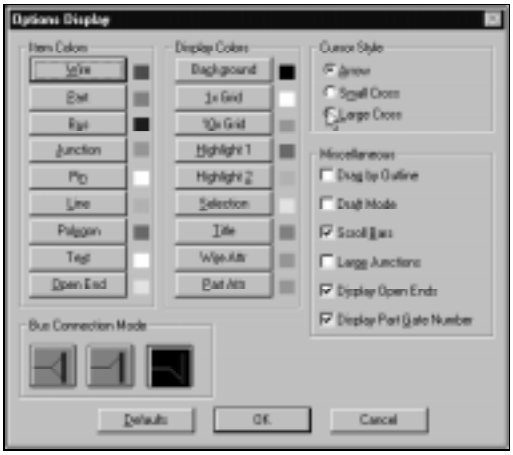


Enable all **Orthogonal Modes**, **ECO Format**, and **DDE Hotlinks**, and set the **File Viewer**, **Autopan (% Display)**, and **Zoom Factor** values to your preference. Notice this is the command used to set the AutoSave options in the licensed version of the product. Click **OK** to exit.

display options

Setting your display and color options is done with Options Display. Choose this command from the menu or keyboard.

easily change colors and display options



To modify the color for an item or display, click the *item's* push button then choose a basic color from the palette. You can also control the cursor style and select miscellaneous display options from this dialog. Choose your preferred cursor style and bus

connection mode, and enable the **Display Open Ends** and **Display Part Gate Number** options. The latter toggles the reference designator display between Part only (e.g., U1) and Part:Gate (e.g., U1:A). Click **OK** to set your selections.

title block and fields

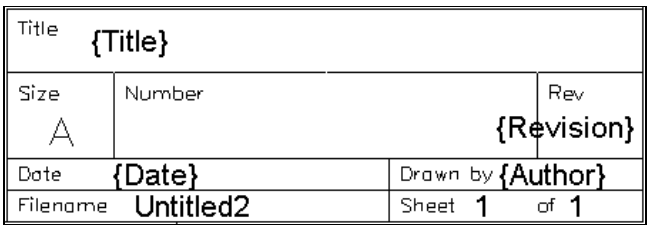
You can fill out your title block using fields. Fields reduce maintenance because each instance is updated automatically when the field's data changes.

add TrueType fonts to your design

Let's create a new TrueType font style to use. Choose the **Add** push button in the Options Text Style command dialog box. Type a **Style Name** and click **OK**. Within the displayed Text Style Properties dialog, choose the **True Type Font** radio button, and then the **Font** push button. Select any **Font** with a **Size** of 12 (points). Return to your design by clicking **OK** or **Close** to exit the dialogs. Make the new style current.

Now zoom in on the title block. Using the Place Field command place **Title**, **Revision**, **Date**, **Author**, **Filename**, **Sheet Number**, and **Number Of Sheets** fields into appropriate sections of the title block. Values are filled in for fields known to ACCEL EDA. Fields in braces (e.g., {Title}) have undefined values.

fields always contain current information



status line magic

If you had trouble placing your fields accurately, the grid spacing is probably set too large. Let's switch to a finer grid. Instead of using the Options Grids command, type a new spacing (e.g., `25mil`) directly into the grid box on the Status line. With a carriage return, the new grid value is made current. Select and drag your fields to center them between the lines.

Let's define the remaining values. Choose File Design Info. Fill in the text boxes, and click **OK**. Now redraw your screen using View Redraw and notice that the field values have been updated. Before opening your libraries, change back to a 100 mil grid by toggling the Grid Select button on the Status line. Use View All to display the entire sheet.

library setup

ACCEL Schematic is shipped with libraries containing over 20,000 components and you can add to this count by creating new ones. This evaluation comes with a small subset of components in a single library, DEMO.LIB. You can use these, create new components, or convert any P-CAD PDIF, Tango-Schematic (DOS), Schema, or Schemax library to ACCEL EDA format and use those components. For more information on using P-CAD files with ACCEL EDA, see Appendix A.

To open DEMO.LIB, choose Library Setup and click **Add.** Locate the file in the eval's Demo subdirectory, then click **OK**. You now have access to any component in that library. ACCEL EDA allows multiple libraries to be opened at the same time, facilitating component organization.

Creating a simple schematic

We'll start our schematic by creating a second sheet and then showing you a few ways to place parts and make connections.

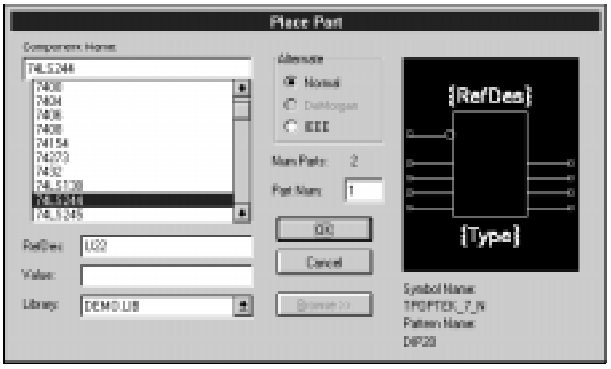
more status line magic

In preparation of needing a second sheet, create one by choosing Options Sheets. Click the white box to the right of the current sheet name on the Status line to access the dialog without going through the menus. New sheets can be created any time during the design. Enter a new sheet name and click **Add**. Leave Sheet1 as the current sheet and close the dialog.

placing parts

Now, we're ready to place a few parts on the schematic. Choose the Place Part icon, then click in the workspace. Choose the **Browse** button to graphically view the available parts and make sure you select the correct one.

browse library parts prior to placing them



Pick 74LS244 from the **Component Name** list or start typing in the box and see how the list automatically scrolls to display parts having the given prefix. Notice **Num Parts** is set to 2, indicating two of these parts fit into one component package. Click **OK**.

Click in the workspace and drag the ghosted part below and to the left of the sheet's center, then release. Remember that your Zoom Window (*Z*), Zoom In (*+*), Zoom Out (-), Zoom Center (*C*), flip (*F*), and rotate (*R*) shortcut keys can be activated to control your display during placement.

The placed part was given a reference designator of U1:A. The Info box on the Status line indicates the next available RefDes is U1:B. Reference designators are assigned automatically and distinguish the multiple parts in a single package. Parts labeled U1:A and U1:B indicate they are two parts of the U1 component.

hotkeys let you change the RefDes on the fly

By default the next 74LS244 part placed in the design is given the RefDes of U1:B. However, hotkeys are available to change it before placement. Press *P* and notice the part number on the Status line is sequentially incremented. *Shift+P* decrements the number. Similarly, *D* increments the RefDes and *Shift+D* decrements it. Press *Shift+D* until the RefDes returns to U1:B.

multi-part components are numbered automatically

Now, click in the workspace again, drag, and release to locate the second 74LS244 to the right of the first. Click the right mouse button or the *ESC* key to complete the placement.

drag and drop copy without extra keystrokes

Make a copy of one of the parts using drag and drop. Press *S* to invoke the select tool, then select U1:A. *Ctrl*+click left, drag to place a copied part above the first two parts, and release. Notice the copy is labeled U2:A, indicating it is the first part (A) of a new component (U2).

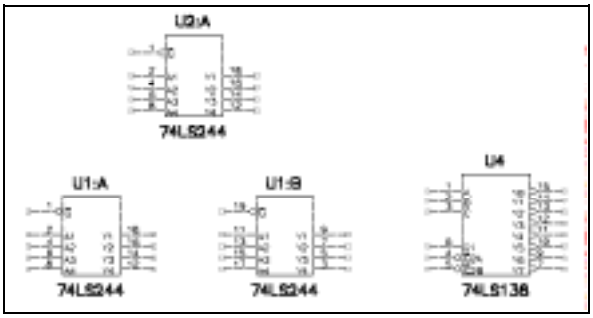
toggle between sheets using the status line

Let's place our next part on the second sheet. Toggle using the sheet Select or Scroll button on the Status line.

Use Place Part again, but this time choose 74154. Place it in the left half of the sheet and terminate by clicking the right mouse button. Note the reference designator is automatically set to U3.

Toggle back to Sheet1 and place a 74LS138 to the right of U1:B. Your design on Sheet1 should now look something like this:

ACCEL Schematic automatically assigns reference designators for multi-part components



placing wires

Next we'll add a few connections. Choose the Place Wire tool from the Toolbar. Start at U1:B, pin 9 and connect U4, pin 1. In creating this connection, drag the wire diagonally and use the *O* and *F* keys to find the correct orthogonal mode and flip to the desired orientation. Notice on the Status line the wire is given a default name of NET00000. Finish your connection with a right mouse click. Add more wires to connect the input data lines for component U4: connect pin 7 of U1:B with pin 2 of U4, and pin 12 of U1:A with pin 3 of U4.

Now let's rename these nets to be clearly identified as data nets. Select the Utils Rename Net command and click in the workspace to bring up the Utils Rename Wire/Port dialog. Enter DATA1 as the net name and enable the **Increment Name** checkbox. Click **OK**. In turn, click a wire in each of the three nets you just created. This will re-name them DATA1, DATA2, and DATA3. A right mouse click (or *ESC)* terminates renaming.

ACCEL EDA allows you to start or end a wire without a pin. Choose the Place Wire icon again and place a wire starting at the left side of the sheet and ending at pin 1 of U1:A. A square should be displayed on the open end of the wire since we previously enabled the **Display Open Ends** option in Options Display. We could rename the net, but let's leave it set to the default.

sub-select the net name to move it effortlessly

Make the net name visible by double-clicking the wire to bring up the Properties dialog, and enabling the **Display** checkbox. Using sub-selection, move the name to a new location. To do this, press the *Shift* key at the same time you click the name. Release the *Shift* key and drag the name to the desired location.

placing GND automatically names the net

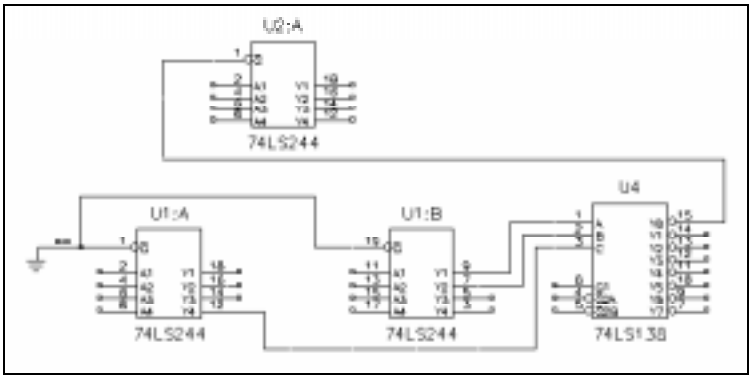
Place a GND part on this open end. The box disappears, indicating the connection is complete. Notice the wire's net name was automatically changed to GND. This is accomplished because GND is defined as a Power part, and Power parts have an automatic net naming feature.

automatic junctions indicate net connections

Starting somewhere along the ground wire, use Place Wire to connect this net to U1:B, pin 19. Notice that a junction is automatically placed and the new wire is added to the ground net. Junction size can be changed from small to large with the Options Display command.

Now connect U4, pin 15 with U2:A, pin 1. Make the connection as shown, so we can later see how to move multiple items.

in just a few steps, your schematic is taking shape



placing buses

Next we'll add a data bus. Choose the Place Bus icon and add a horizontal bus below the placed parts. Next, place three separate wires to tie pins 2 and 4 of U1:A, and pin 11 of U1:B to the bus. Start or end your wire anywhere along the bus. There's no need to terminate with a right click; a bus entry is automatically placed. The entry style is the one previously selected using the Options Display command.

placing ports

Two of the wires just placed belong to signal IN1. These wires are not physically connected, but carry the same signal. Ports are used to identify such unconnected subnets of a single net. They also allow you to explicitly identify subnets on one or more sheets, and their use prevents unintentional net merges. Choose the Place Port command and click in the workspace to view the dialog. Set the Net Name to IN1 and disable the **Increment** checkbox.

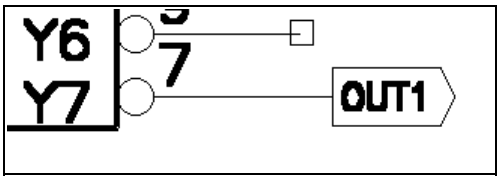
To place ports on the vertical wires, select options to create ports with two pins and a vertical orientation. Notice the preview box allows you to view the port's display before it is placed. After clicking **OK** to close the dialog, click and drag the port to the wire connecting pin 2 of U1:A with the bus. Place a second port on the wire connecting pin 11 of U1:B. Terminate placement with a right mouse click or *ESC* key.

Working with your design

Cowabunga! We've nearly forgotten the part on our second sheet. Before we head over there, place a port directly onto pin 7 of U4, naming the net `OUT1`. Choose a port with one pin, horizontal orientation, and shaped to identify it as an off-sheet connector. Select the port and drag it away from the pin.

abutment wiring speeds design work

Notice a wire was automatically added to fill the gap! This technique, called abutment routing or abutment wiring, can also be used to wire parts together without using the Place Wire command. You simply move the pins of one part on top of the pins of another, then separate the parts. Wires are added, connecting the once-overlapping pins.



moving to other sheets

We could toggle to the second sheet, but let's jump there instead. Choose Edit Parts and select `U3` from the list. Click **Jump**. The sheet will change automatically and the cursor will be placed at the reference point of U3.

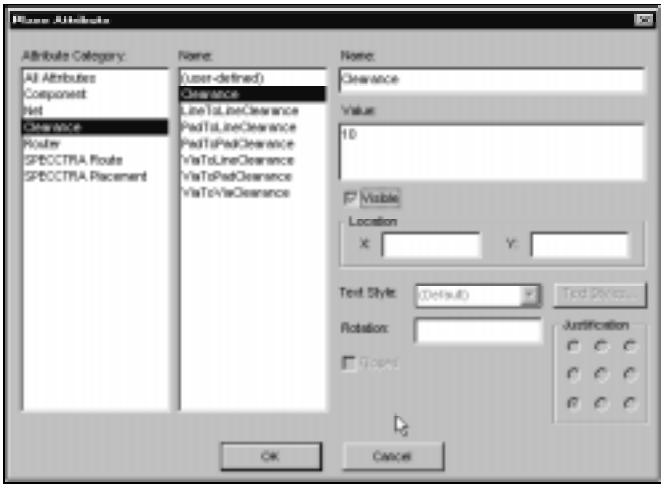
Place another port at pin 23 of U3, using the same `OUT1` net name, and a port type that identifies it as an on-sheet connector. Recall that the *R* key can be used during placement to rotate a port. Select and drag the port to the left, away from the pin.

adding net attributes

Now, let's add attributes to this net. Select the wire, click right, and choose **Edit Nets**. `OUT1` is already selected. Click the **Edit Attrs** button. The box lists current attribute names and values. It will be blank. Press **Add** and examine the list of predefined

attributes available for placement. (User-defined) attributes may be added with any name and value you desire. These are useful when generating your own reports or interfacing to external programs. Choose the Clearance Attributes **Category**, pick the Clearance attribute **Name,** and enter a **Value** of `10`.

net attributes assigned in the schematic can be used in the PCB



Press **OK** and you will see the newly added entry in the list. Net attributes are transferred in the ACCEL EDA netlist from the schematic to the PCB, where many are used for operations such as DRC, pin and gate swapping, and routing. Press **OK** and then **Close** to exit the dialogs.

We can speed attribute assignment by grouping similar nets into a class, and assigning rules to the class. Using the Options Net Classes command enter `DATA` as the **Class Name** and press **Add**.

apply design rules to a class of nets

Select the DATA* nets in the **Unassigned Nets** box (use the *Shift* key to select a range, or the *Ctrl* key to select individual nets) and press the **<-Add** button. Similarly, add the IN1 and OUT1 nets to the class. Click **Edit Attrs** to present the familiar Attributes dialog box. Assign a **Clearance** attribute of 8 to the class.

Holy cow... net OUT1 has been given two conflicting clearances! Which one would be used for DRC? Ten, and here's why:

a hierarchy simplifies design rule assignment

ACCEL EDA maintains a design rule hierarchy to simplify design rule assignment. You add global rules, then need to define only the exceptions. Exceptions can be given for a group of nets, a single net, or between groups of nets. Precedence for assigned rules is given in the following order:

- class-to-class (highest precedence)
- net
- net class
- design level (lowest precedence)

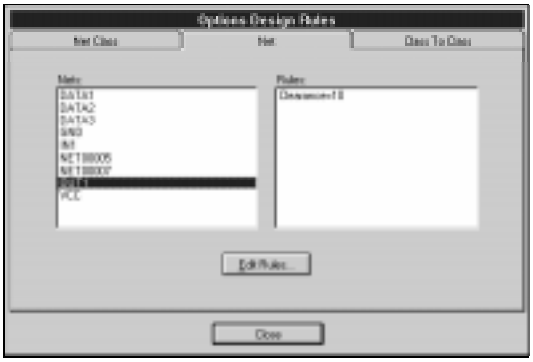
Rules assigned at the higher precedence level are used whenever there is a conflict. In our design, the Clearance value of 10 applied directly to the net will be used because net rules have a higher precedence than net class rules.

clearance rules from the schematic are used for routing and DRC

Clearance attributes assigned to any level of the hierarchy and carried to the PCB using the netlist are recognized for design rule checking (DRC), manual and interactive routing, and the SPECCTRA routing and placement products.

To view or edit hierarchical assignments, choose the Options Design Rules command. Look at our recent DATA net class and OUT1 net rule assignments. Use this command to view, add and edit design rules at any level.

design rules are accessed using one command



add a clearance to all two-node nets

One additional shortcut we'll introduce here is to select nets having a given number of nodes. This is helpful when applying rules to single- or double-node nets or the large nets as a group. With ACCEL EDA, it is easy to find these nets.

In the Edit Nets command dialog box, enter a **Min** value of 2 and **Max** number of 2 nodes. Click **Set Nets By Node Count** and notice all double node nets are identified in the **Net Names** box. Attributes can be added to all of these nets at the same time. Notice you can also use this command to highlight, select, and delete the identified nets.

probing nets across sheets

Nets and buses are easily probed across sheets. Use the Edit Parts command again, except this time choose U3 in the list and then click **Highlight Attached Nets**. The OUT1 wire is highlighted in the first highlight color. Toggle back to Sheet1 to easily locate OUT1 as the highlighted net on that sheet as well.

selecting a subnet or an entire net

Select any segment of the IN1 net; the one attaching U1:B to the bus. Click right and choose the **Select Contiguous** option. Notice only the physically connected wires are selected. Click right again, this time choosing the **Select Net** option. Notice now that the entire net is selected.

viewing the nets in a bus

If you ever need to recall what nets are attached to your bus, this information is readily available. Choose Edit Nets and select **Bus** in the **Type** box. Choose BUS00000 from the list of buses and its attached nets are then in the **Nodes** box.

making changes

Let's go back now and change our design to move U2:A closer to U4. Block select U2:A and the two wire segments closest to its pin 1. If you miss any of these, add to your selection with a *Ctrl*+click on the missing item. Move the items to the right so that U2:A is above U4. The long horizontal segment shortens automatically, maintaining connectivity.

moving multiple objects

If the component needs to be moved up to make space, the "horizontal" segment becomes non-orthogonal. Move your selection up a grid point. Adjust the display by selecting the diagonal segment and moving its left endpoint down a grid point to again create a 90-degree corner. Actually, you could have avoided the diagonal altogether if you had added the horizontal line to the selection (*Ctrl*+click) before moving the items up!

connectivity is maintained

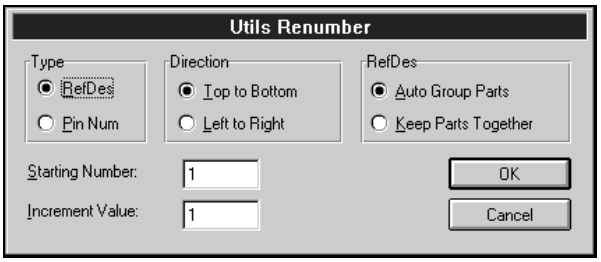
Another facet of moving wires can be seen by selecting the vertical wire segment you had previously selected and moving it to the left and back to the right. Watch how connectivity is maintained. Remember that when moving items, you can always Undo (by pressing the *U* key or Undo Toolbar icon) to return them to their original locations.

renumbering designators

Before we verify our design and generate output, we should renumber our reference designators. To get a better idea of how renumbering works with different types of parts, place a few RES500 resistors on your sheet.

To renumber reference designators, choose the Select tool then use Utils Renumber.

renumber easily from top to bottom or left to right



Leave the dialog settings as they are and click **OK**. Your reference designators will be renumbered in top-to-bottom order within prefix types. In particular, your resistors are renumbered starting with R1, and the IC's are renumbered starting with U1. Notice also, renumbering of U3 and U4 was done across sheets.

adding values after placement

Select one or more resistors, then click right, and choose **Properties** from the pop-up menu. Enter a **Value**. Click **OK** and notice the Value field is updated for each part selected.

deleting parts

The resistors were added for practice and are extraneous. Use the Options Block Selection command to select only the RES500 resistors for deletion. Click the **Clear All** button. Then toggle the **Part** checkbox until it is gray and the **Part** push button is enabled. Click the push button to bring up the Part Selection Mask dialog. Enter `RES500` in the **Type** box and click **OK**. Choose the **Outside Block** selection mode and then **OK** to exit the dialog. Now click and drag in the workspace to create a block away from all resistors. All of your resistors should be selected. Delete them

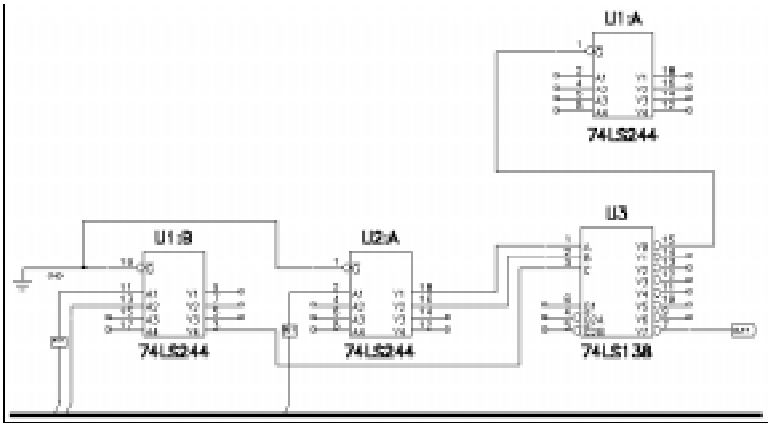
select all resistors on your sheet using block selection

with the *delete* key, or by clicking the right mouse button and choosing **Delete** from the pop-up menu.

It is important to reset block selection using the Options Block Selection command. Choose the **Set All** push button and enable the **Inside Block** mode.

At this point, your design should look something like the following. If it does, congratulations! If not, you've been exploring on your own!

sheet 1 of 2 of your first design using ACCEL Schematic



making more changes

Before moving on to check the design and generate output, there are a few more things to know about editing your Schematic that will simplify your life.

Block Select the left portion of your design capturing everything to the middle of U2:A, including U1:B, its attached wires, the entire GND net, both IN1 lines, the ports, and part of the bus. Add a selection point at a coordinate that is easy to work from (e.g., at (2000, 2000)). This point is optional, but useful for making changes that require precise movement of selected items, as we'll see below. Click the right mouse, choose the Selection Point option, and move the cursor to the desired location as shown on the Status line. Alternately locate the point exactly by entering X and Y coordinates in the Status line edit boxes (press the *J* key to jump there, *Tab* to move between X and Y, *carriage return* to accept the values). Click left to place the point.

the Selection Point simplifies accurate editing

Using *Ctrl+drag*, copy the selected block to an empty area. Watch the coordinates on the Status line to see the exact distance moved. Zoom in to easily view the copied block.

Probe the wire names by selecting them (check the Status line for the name) or displaying their names, and notice that naming of copied items follows well-defined and consistent rules:

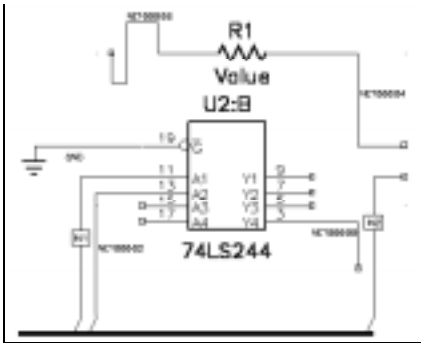
- Global nets maintain their original names. Global nets include nets with ports (e.g., IN1), nets attached to power parts (e.g., GND), and hidden power nets.
- Nets that are not global are assigned unique default system names (e.g., NET00002).
- Components are given unique reference designators.

Net names are also consistently assigned when a net is split. Insert a RES resistor in the horizontal GND wire above U1:B and probe the wires on both sides. Note that the GND net has been split and a default name was given to the newly created signal. Other methods of splitting a net include deleting a middle wire segment and renaming a subnet. To try these, first delete the vertical GND wire at the junction and notice that the GND net was again divided. Then choose Utils Rename Net, setting the name to IN2 and the **Domain** to **Contiguous Wire**. Click on one of the IN1 wires and notice only the selected subnet is renamed.

Double-click the resistor to bring up its Properties dialog. The resistor can be changed to an alternate type. Change RES to RES500 in the **Type** field list box. The component's type is updated and connectivity is maintained. This powerful feature requires parts to be defined equivalently. It must be used with caution to avoid mismatching pins and pads.

add extra corners with the Rewire Manual command

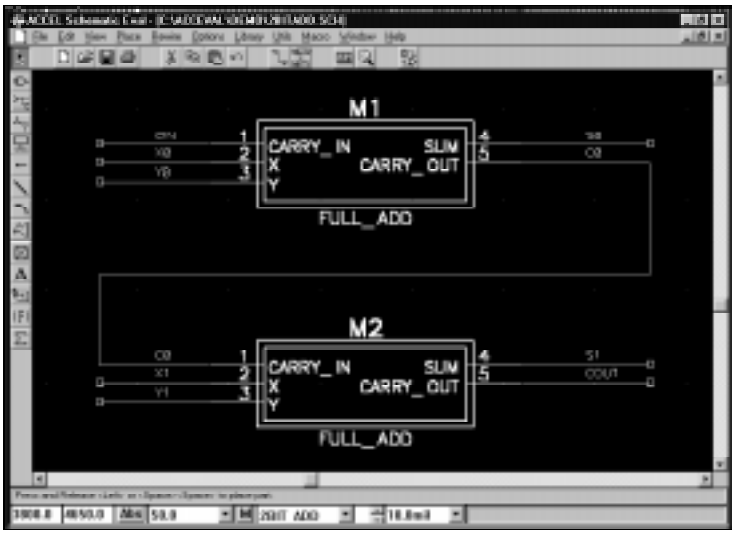
Finally, you will want to experiment with rewiring a net. Choose the Rewire Manual command then click a wire to pick it up. Subsequent clicks add vertices. We used the horizontal wire attached to the resistor. Here's what we ended up with:



traversing a hierarchical design

Let's take a detour to look at creating and using sub-circuits in ACCEL Schematic. 2BITADD.SCH is a multi-level hierarchical design. Load it, from the eval's Demo sub-directory.

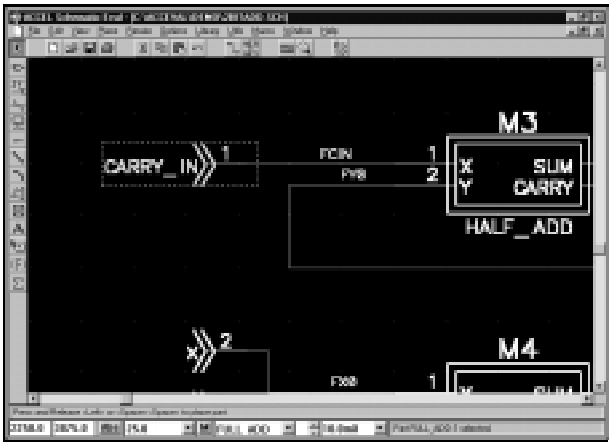
modules M1 and M2 abstractly represent full adder circuitry



Examine component M1 or M2 on sheet 2BIT_ADD. The M reference designator prefix indicates it is a module; a *black box* component that abstractly represents a sub-circuit. It has three input pins and two output pins, each representing an input or output of the sub-circuit.

descend the hierarchy to view a module's circuitry

To look at the sub-circuit's definition, descend the hierarchy: select M1, click the right-mouse button, and choose Descend. After picking any pin number and pressing **OK**, you are taken to the designated input or output symbol of the sub-circuit.

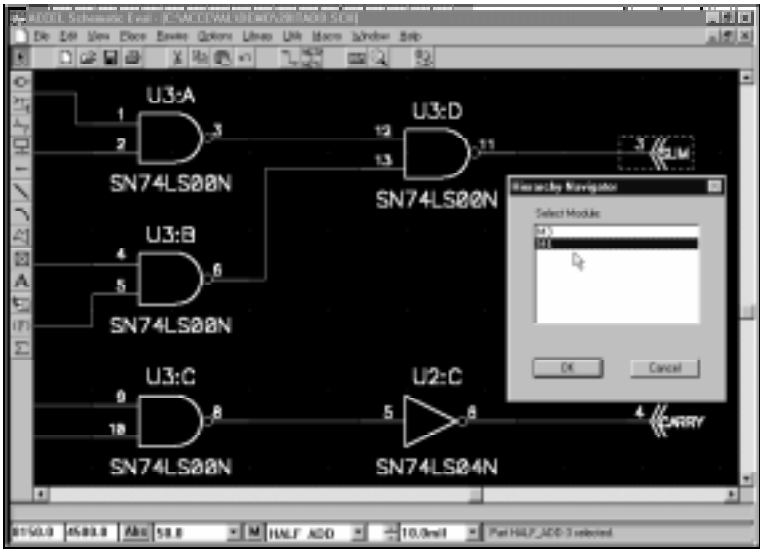


CARRY_IN, X, Y, SUM, and CARRY_OUT are the interface symbols, or “links”, for the full adder. These interfaces are special parts: they link the abstract, higher-level module to this lower-level sub-circuit definition.

The full adder is created using two half adders, as seen on the viewed sheet. Select one of them and again descend to view its sub-circuit logic. The circuitry on this HALF_ADDER sheet is completely defined with no other hierarchy levels to descend.

To see all instances of where this sub-circuit is used select any of the links (e.g., SUM), click the right-mouse button, and choose Ascend. You will be shown a list of modules linked to the circuitry.

it’s simple to locate where a sub-circuit is used



Select a module and press **OK** to ascend. In the same manner, ascend once more, to the highest level of the hierarchy, back to sheet 2BIT_ADD. Zoom out to leave space for adding a new module.

creating a hierarchical design

To build a hierarchical design you must take the following steps:

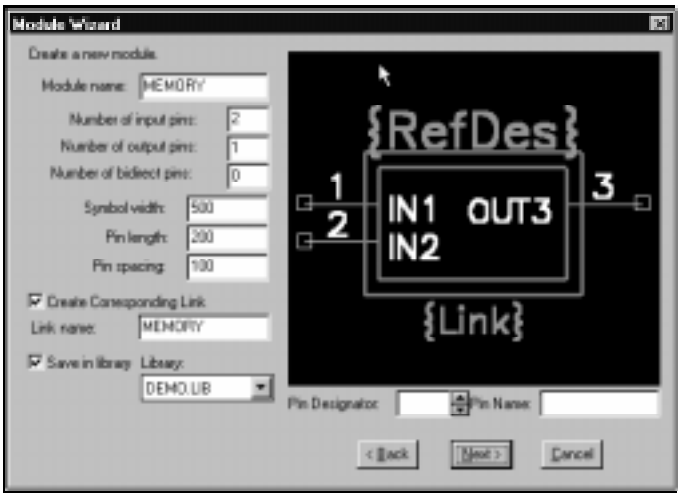
- Create a module and its link (or reuse an existing module).
- Place the module in the design.
- Resolve the hierarchy.

Select the Utils Module Wizard command and choose the option to **Create a new module and its link**. Then click the **Next >** button.

A Module Wizard dialog is presented for specifying the module and link parameters.

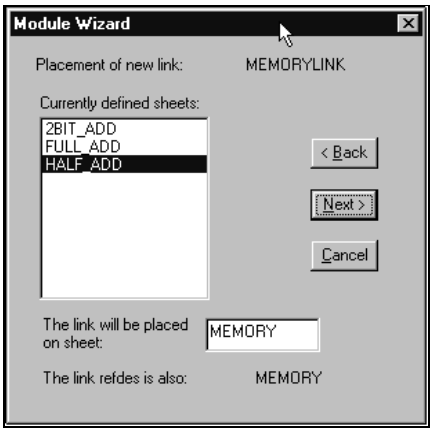
Watch the preview window to see changes in the module's display as parameters are entered. As shown below enter values to create a MEMORY module with 2 input pins and 1 output pin, having a width of 500 mils, a pin length of 200 mils, and pin spacing of 100 mils. To set up for defining the logic within our memory module, enable the **Create Corresponding Link** checkbox and enter MEMORYLINK as the link name. Finally, enable the **Save in library** checkbox and set the library name to DEMO.LIB.

the Module Wizard's preview window displays the module as it is built



Press **Next >** and then enter MEMORY as the name of the sheet on which the links (and your sub-circuit logic) will be placed.

a sheet is added for your sub-circuit logic

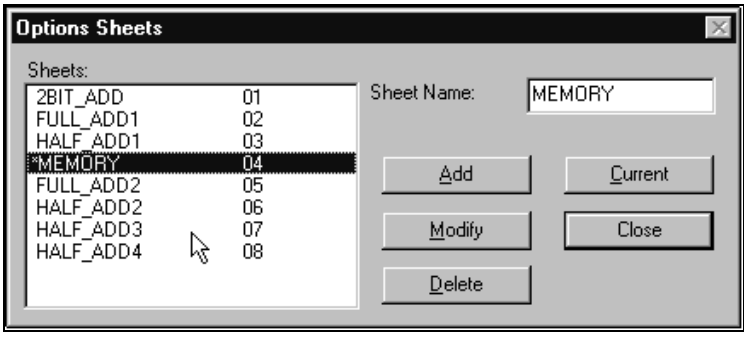


Press **Next >** again to move to the final Wizard dialog, where you have a chance to change the default reference designator. Press **OK** and you are ready to place your module! Click left-mouse to locate the module in the workspace. Select the newly placed module. Right-mouse click and descend from the module to its links on the MEMORY sheet, where you would complete the sub-circuit logic.

resolving the hierarchy

Before performing ECOs or generating netlists (not available in this eval) you must "resolve the hierarchy". This process flattens the hierarchical structure of a design to give every instance of every component a unique reference designator. In the case of a multi-level hierarchy, a sheet is added for each instance of sub-circuit logic.

Although you'll get warning messages because the module pins aren't connected and the sub-circuit logic was not completed, run the Utils Resolve Hierarchy command to see the results of the process. Press **NO** in response to saving the file and ignore the warnings of unconnected modules and links. Instead, focus on the list of sheets now available. Run the Options Sheets command and see a sheet has been added for each sub-circuit instance.

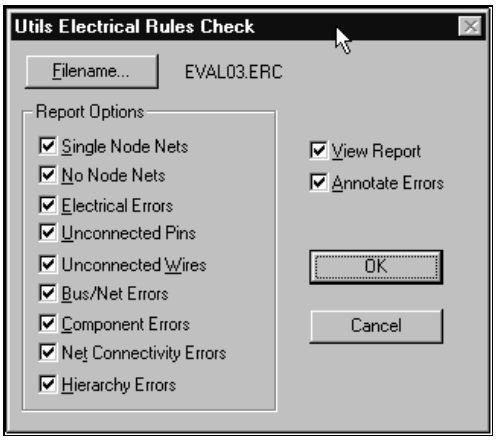


In particular notice the two full adder sheets and four half adder sheets (two for each full adder). Looking at these closer, you'll see reference designators have been uniquely assigned to the components.

Design verification

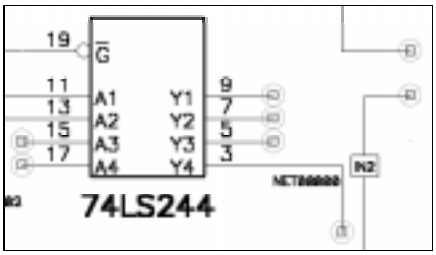
ACCEL EDA offers a range of electrical rules checks (ERCs). To access these and check your design, use Utils ERC. For this example, enable all **Report Options**. Also, enable **View Report**, so an on-screen report is presented, and **Annotate Errors**, so error indicators are placed to graphically identify violation locations. Click **OK** to start the check.

ACCEL EDA electrically checks your design



The ERC report is opened using the File Viewer specified in Options Configure. Window's Notepad is the default. Reports are viewed, edited, or printed from that utility. Several errors will be reported including missing input and output pins, bus violations, unconnected pins, and a single node net. Toggle back to your design and notice that indicators have been placed.

view the location of errors on-screen



Each marker contains error data and an output report reference number. Block Select the indicators, right click, and choose **Properties** to view the descriptions. **Next** and **Previous** buttons are available if multiple indicators are selected. Close the dialog and delete the indicators by pressing the *Del* key. Running Utils ERC with the report options disabled also clears the old markers.

Output is the ultimate goal of your design work, and another area in which ACCEL EDA excels. All Schematic reports are accessed from File Reports. Choose this command and enable all **Report Options** so you can see the format and contents of each report. Select the Report **Style Format** and send the reports to the screen. Choose your desired **Page Format** options, filling in the text boxes for a header and footer if you choose to include them. When you click **Generate**, the reports are created and presented using the File Viewer specified in Options Configure. Each report is given a unique file extension.

your design information is captured in ACCEL EDA reports

printing your schematic

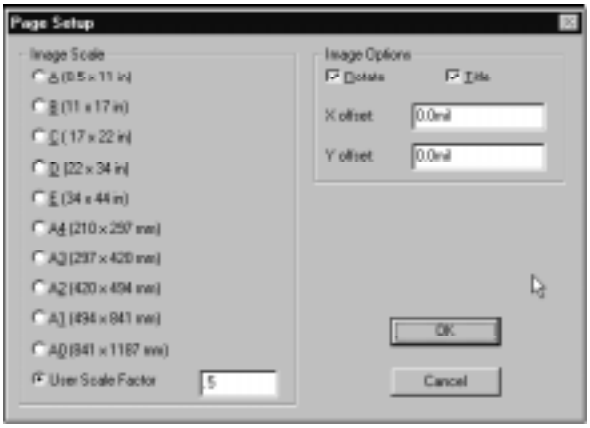
The eval software doesn't allow you to cut or copy data to the clipboard for preparing design documentation or generating design output. However, you *can* print files created in the licensed package if they have not been edited in the evaluation. Open DIGDEMO.SCH from the eval's Demo subdirectory.

setting up the printer is standard Windows

The File Print Setup command brings up the standard Windows Print Setup dialog box. Choose your printer, paper, resolution, orientation, and so on.

Choose the File Print command to set up your image and printing operations. Notice you can print the entire design, contents of the current window, or the selected region. Click **Page Setup**. Here you can specify the image scale, rotation, offset, and use of a title. Enter a user scale factor of `0.5` and enable the **Rotate** checkbox so the file prints on a single page. When you are finished, click **OK** to return to the File Print dialog.

set your printing image options in the Page Setup dialog box



Click the **Print Options** to access the familiar looking Options Display dialog. Note the option to **Display Part Gate Number**. The display for printing may differ from the on-screen display. Colors and options are limited to those supported by your printer. Select the desired colors and options, and click **OK** to complete the setup for printing.

Back in the File Print dialog, select the sheets you want to print, then click **Generate Printouts** to start printing.

netlist generation

We are now ready to take the final step and generate a netlist. Choose Utils Generate Netlist, click **Netlist Filename**, and enter an output filename. ACCEL ASCII, Tango, P-CAD, FutureNet Netlist, FutureNet Pinlist, EDIF 2 0 0, and PSpice netlist formats are available. Select the ACCEL ASCII format (it includes your attributes) and click **OK** to generate the output.

section review

In this section you have completed the following:

- Workspace, display, title block, and library setup.
- A simple, two-sheet schematic.
- Editing a schematic.
- Result verification using rules checking.
- Report generation, netlist creation, and printed artwork.

With our output generated and artwork completed, we have come to the end of our ACCEL Schematic tour. You've seen how easy ACCEL Schematic is to use, so start your own creations or move ahead to create your own PCB design.

A PCB Design Session

In this section we'll take you through the steps to create a small PCB design with ACCEL P-CAD PCB. But don't worry, we've done most of the work for you. You'll see how to:

1. Set up your design by customizing the settings for your workspace, display, layers, line width, pads and vias, grids, and libraries.
2. Lay out a small printed circuit board design; place an outline, automatically load components into the workspace, and move them into position.
3. Manually route connections, then modify your traces.
4. Finish your design with copper pours.
5. Verify your design and generate reports.
6. Print and produce CAM output.

Routers play an important role in the productivity gains achieved with today's design automation tools. We've reserved the discussion of autorouting for the next section.

Setting up your design

With the Options commands -- Configure, Grids, Display, Preferences, Current Layer, etc. -- you may set ACCEL P-CAD PCB's extensive options to suit your own tastes and needs. The settings you establish are saved with your current design, and become the new defaults for subsequent design sessions.

setting up the workspace

ACCEL EDA comes with a complete set of title blocks. After starting ACCEL P-CAD PCB, we'll load an A-size border. Using the File Open command or drag-and-drop operation, open TITLE_A.PCB from the eval's Titles subdirectory (e.g., `c:\acceval\titles`). Maximize the window.

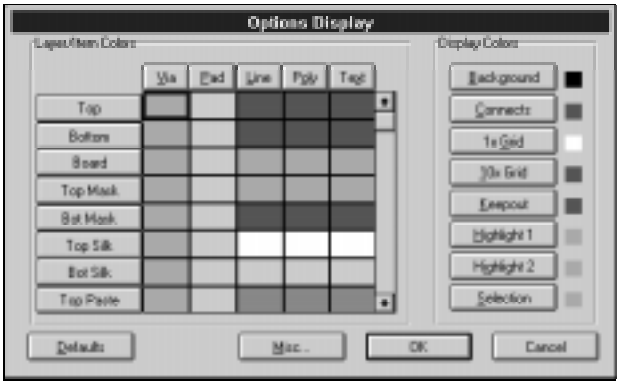
Choose Options Configure and toggle between **mils** and **mms** in the **Units** box. Notice your workspace size changes to match the units. Leave **mils** selected. Enable all **Orthogonal Modes** checkboxes then click **OK** to continue.

set assorted configuration options with the Options Configure command

display control

Use Options Display to choose your favorite colors and other display options. Click an item name, a layer name, or a color button to set the color for the associated object. A Color palette is presented, from which you can choose a new color.

choose colors to suit your taste with the Options Display command

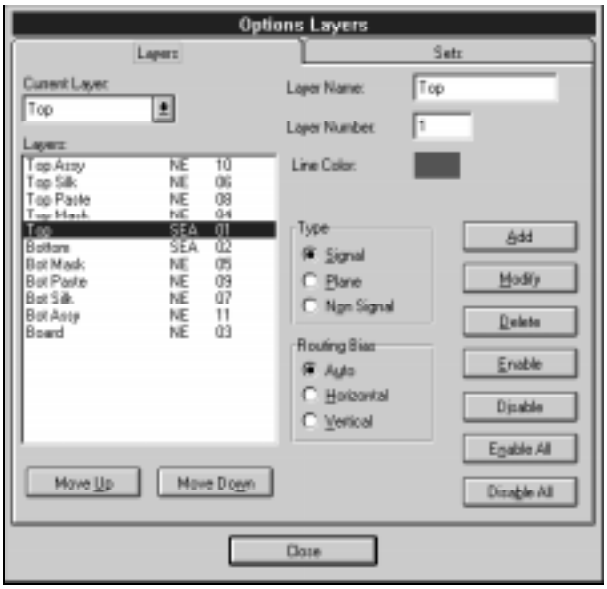


setting up layers

Choose the Options Layers command and notice that the range of options includes adding, deleting, ordering, and enabling layers for your design. The existing design layers are listed in the **Layers** list box. ACCEL EDA allows up to 99 layers; 11 *predefined* and 88 user-defined layers.

The **Current Layer** can be set in the dialog or, usually more quickly, from the Status line. Single layer items (e.g., lines, arcs, some polygons, copper pours, split planes, attributes, text, fields, dimensions) are placed on, and selected from, the current layer.

configure up to 99 layers with the Options Layers command

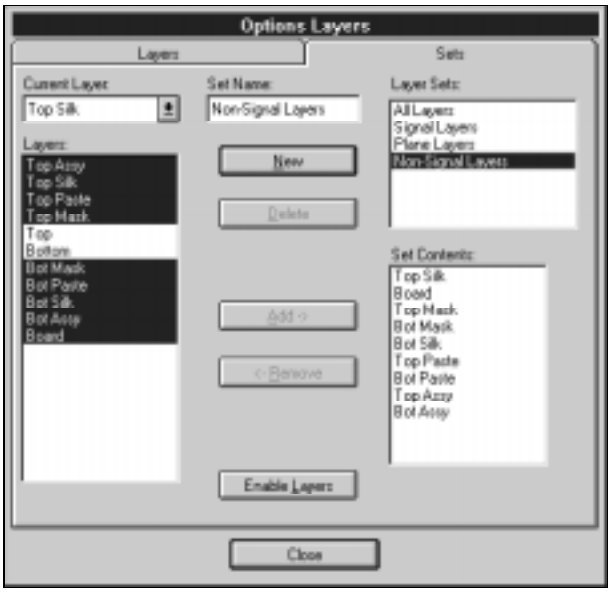


The letters between the layer name and layer number in the **Layers** box signify (in the case of the Top layer) **S** for Signal layer, **E** for Enabled, and **A** for a Routing Bias set to Auto. Other codes you will see are **P** for Plane, **N** for Non-Signal, **D** for Disabled, **H** for Horizontal, and **V** for Vertical.

The **Move Up** and **Move Down** buttons reorder signal layers between the top and bottom of your board. Ordering is important for pad and via stackup, DRC, and many manufacturing and other output operations. Enabling and disabling layers affects their display and, for signal layers, their availability for routing.

Under the **Sets** tab is the dialog for establishing layer sets. Select the various entries in the **Layer Sets** list and notice how the **Contents** change. Using this dialog box any grouping of sets can be defined to facilitate display, printing, Gerber, NC Drill, and DXF Out operations.

establish sets of layers to facilitate output generation



For this tutorial, no changes are needed. Click **Close**.

setting line width

The width of lines placed on the board is determined by the current line width shown on the Status line. You can add a new width using Options Current Line, but it is faster to enter it directly. Type 8 in the line width edit box on the Status line.

pad and via stacks

Let's take a detour to look closely at pad and via stacks, including blind and buried vias. Load ACCSAMPL.PCB, provided in the eval's Demo subdirectory.

ACCEL EDA supports both *simple* and *complex* pads and vias. Surface mount pads and uniform, through-hole pads and vias are considered *simple*. Since these types are predominant in a design, we offer special dialogs that can be used when dealing with them. This makes it easier for you. To view a 60 mil x 60 mil round through-hole pad, choose Options Pad Style, select P:EX60Y60D38A in the **Current Style** list box, then press **Modify (Simple)**.

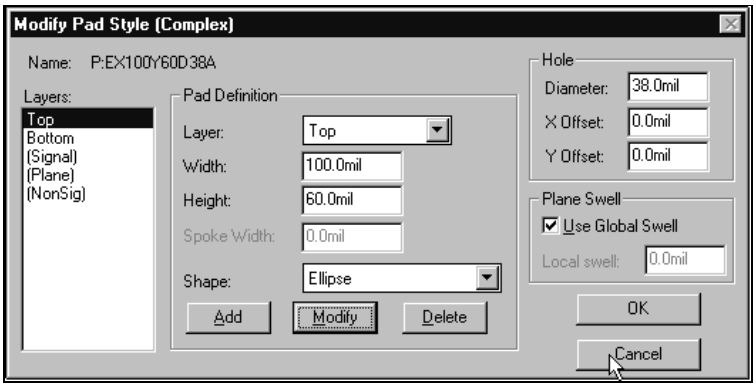
a simplified dialog is presented for surface mount and through-hole pads

Look at the definition but leave that style unchanged. We'll look more closely at *complex* pads and vias. ACCEL EDA lets you define different shapes and sizes on the various layers in a design. This feature, called *pad stacks*, helps you route tough designs and allocate more clearance on certain layers.

A similar feature, called *via stacks*, allows you to set up different styles of vias on a layer-by-layer basis and void vias on certain layers, creating blind and buried vias.

Zoom in to area 4 on the sample board where we have created a pad stack, via stack, blind via, and buried via. Double-click the pad labeled **Pad Stack** to bring up the **Pad Properties** dialog. The 100x60x38 style is shown in the **Pad Style** box as P:EX100Y60D38A. Click **Pad Styles** then **Modify (Complex)** to access the dialog for changing the style definition. View the details of the style by clicking on each layer or layer group in the **Layers** list box. You'll see different sizes and shapes defined for the top, bottom, plane, and internal signal layers.

pad sizes and shapes can easily be varied layer-by-layer, creating pad stacks



Exit the dialog without making changes. Switch your current layer to the Top, Bottom, and a middle signal layer, choosing View Redraw after each layer change. Notice the shape and size of the pads on each layer matches the stackup definition.

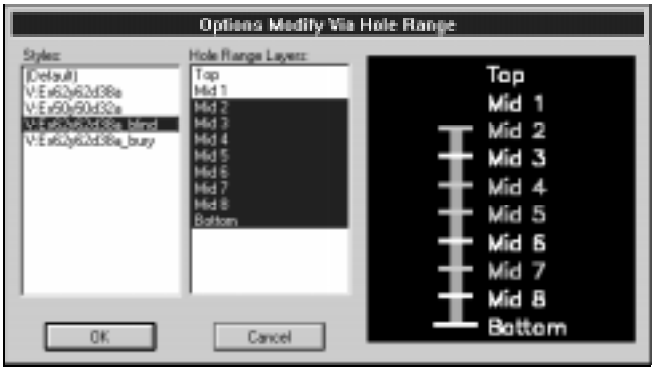
blind or buried vias are no problem for ACCEL EDA

Via stacks are created and defined the same way. You may want to probe the blind and buried vias provided. Double-click the blind via and press **Via Styles** to bring up the Options Via Style dialog. Choose **Modify (Complex)** to view the definition.

Our blind via was created by making the via size on the upper two layers zero by zero. Confirm this by clicking Top and Mid1 in the **Layers** box and examining the values in the **Via Definition** section. Then choose Bottom in the **Layers** box and notice the pad on the bottom is 80 mils round. Finally, pick (Signal) in the **Layers** box to notice all signal layers not explicitly defined are round and have a diameter of 62 mils. This includes layers Mid2 through Mid8. The via feeds from the bottom through internal signal layers Mid8 through Mid2, but does not penetrate the uppermost two layers. An 18 mil hole has been assigned.

Exit that dialog by pressing **OK**, and choose **Modify Hole Range** to view the style's cross section. It's easy to visually confirm this is a blind via stackup with a larger pad on the bottom and a hole connecting the desired layers.

the via stackup is visually verified using the Via Hole Range dialog



When manually routing from one layer to another, ACCEL EDA will alert you if you try to insert a via between layers that the current via style does not support. For instance, you'll be warned if you try to route from the Top to Bottom layers when our blind via style is current.

The buried via style on the board connects only internal layers. You may want to examine it as well.

As you can see, “complex” pad and via styles are simply a definition of pad shapes and sizes on each signal (and plane) layer, with a hole connecting them. Once you understand this, it is easy to create a new one. Are you ready?

create a blind via with ease

You create new pad and via styles by copying an existing style then changing it. We’ll make a new blind via using the existing one as a base. Choose the Options Via Style command and press the **Copy** button. Enter a unique **Via Name**, select the blind via style in the **Copy Of** list box, and exit that dialog. Click your new style name in the **Current Style** box and then press **Modify (Complex).**

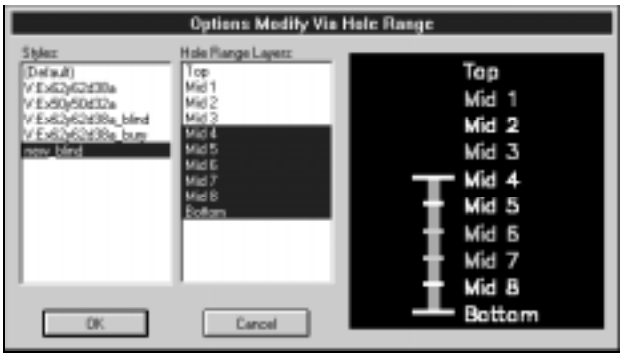
We’ll modify the new style to feed from Mid4 to the Bottom and have different pad shapes and sizes. First we need to explicitly define zero-sized pads for layers Mid2 and Mid3. Currently pads on these layers follow the generic “(Signal)” layer definition. Select Mid2 from the **Via Definition Layer** pick list. Set the **Width** and **Height** to be zero, and press **Add**. Notice Mid2 now shows up in the **Layers** box indicating a pad on that layer has been defined explicitly. Repeat to create a zero-sized pad on Mid3.

Similarly, explicitly define an 80 mil x 60 mil rounded rectangle pad on Mid4. We’ll leave the Bottom layer alone, but let’s change the pads on all other signal layers to be 40 mils square. Click (Signal) in the **Layers** box, choose Rectangle as the **Shape**, update the **Width** and **Height** to be 40 mils, and press **Modify**. Press **OK** to save your changes and return to the Options Via Style dialog.

From there, press **Modify Hole Range** and notice that the hole extends too far. To correct this, click Mid4 in the **Hole Range Layers** box and press the *Shift* key while clicking Bottom.

This defines the via hole from Mid4 through the bottom of the board. Visually compare your new blind via against the original one by alternately clicking the two style names. Press **OK** to save your hole range change, and close the remaining dialogs.

visually check the hole range and relative pad sizes of your new via



Set your new via current and place one. Toggle to each layer and redraw to verify your construction. Note that you "see through" to layer Mid4 when the top layers are current, since no pads are defined for those layers. The pads should look like this on Mid4, Mid5 - Mid8, and Bottom:

Now that you're an expert at creating complex pad and via stacks, toggle back to your own design by clicking the TITLE_A.PCB name in the Window menu. Here, the **Default** 40 mil round through-hole via style is current.

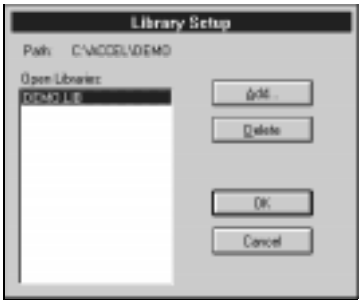
setting grids

A 100 mil grid works well for placing through-hole components. This allows maximum flexibility when later selecting a grid for routing. If the current absolute grid is not set to 100, set it by typing `100` into the grid edit box on the Status line.

setting up libraries

To place components, you must first open the libraries that contain the components you will use. Add DEMO.LIB, from the eval's Demo subdirectory, to the list of open libraries using Library Setup or *drag and drop*.

use Library Setup to open component libraries for placement



Initial board layout

create a board outline

To start a design, create an outline on the board layer. Recall that lines and arcs are non-electrical entities, but they do create copper and will affect design rule checking if you place them on signal layers. Make the **Board** layer current using the layer controls on the Status line. Place lines and arcs to draw a shape approximately 5" x 2.5" in the lower part of the workspace. Remember to use your *O*, *F*, and *backspace* keyboard shortcuts.

We've provided an outline for your convenience. To view or use it, load DEMO1_O.PCB from the eval's Demo subdirectory.

load a netlist

To design a PCB on-the-fly, you would place patterns one at a time and then add the connections using Place Connection. However, most designs today are first created as a schematic, from which a netlist is generated. A *netlist* lists components and their electrical connections. Each set of connections carrying the same signal is a *net*. Connected component pins are defined as *nodes.*

Loading a netlist into ACCEL P-CAD PCB has two effects:

1. Components in the netlist are automatically placed in the workspace, if they are found in the libraries currently open.
2. Electrical connections between nodes are made, forming the *rats nest*.

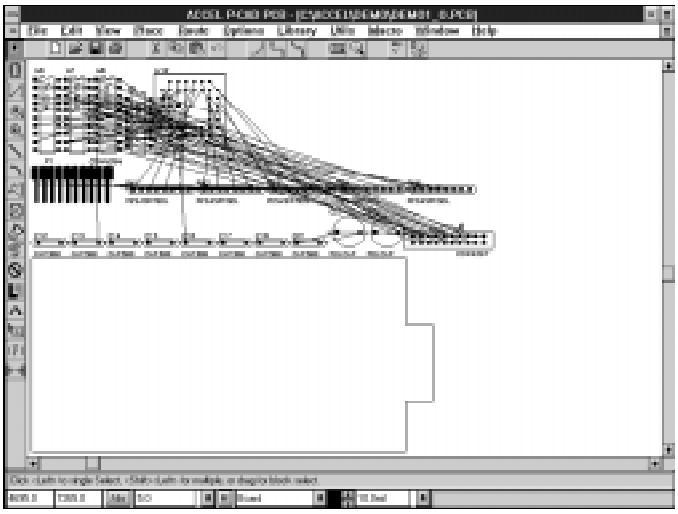
Recall that the libraries from which the components are placed must be opened. Run the Library Setup command to verify DEMO.LIB is opened, and add it if it is not. Exit the dialog.

automatically load components into your workspace

Now load the netlist DEMO1.NET from the eval's Demo subdirectory using *drag and drop*. Alternately choose the Utils Load Netlist command. Click **Netlist Filename** to locate DEMO1.NET and choose ACCEL ASCII as the **Netlist Format**. Click **OK** to exit the dialog, and again to start netlist loading.

ACCEL PCB scans the open libraries, retrieves the patterns, and places them in the workspace above your board outline. Then the *rats nest* of net connections is created.

board outline, placed components, and rats nest of connections



locate your components

Once the netlist assisted placement is complete, you typically move the components into position within the board outline. Achieving optimal placement is a crucial foundation to designing high-quality, manufacturable printed circuit boards.

The rats nest provides a visual clue of the board's densities. You can control the display of nets with the Edit Nets command. This is useful for focusing on a set of connections, such as address lines or your power and ground nets.

connectivity is always maintained

When selecting and moving several components into position, the connections *rubberband* to maintain the established nets. Remember you can zoom during editing, rotate and flip the components (using the *R* and *F* keys), and move the mouse freely without having to keep the left button depressed (with *Alt*+click).

move a component by its reference designator

To quickly pick up the connector for placement, choose the Edit Move By RefDes command and type `P1` into the **RefDes** box. Click in the workspace to attach the component to your cursor and drag the connector to the right side of the board.

align components

wildcards are used to select specific items

To align the resistor packs near the connector, select all five of them. We'll practice using a Block Selection filter, although it isn't really necessary here. Choose Options Block Selection and clear all items. Next, click the Component checkbox until it is grayed. Press the **Component** push-button and type `RN*` in the **RefDes** text box. Exit those dialogs and block select across the entire design. Only the resistors should be selected.

Press the right mouse button and choose **Selection Point** from the pull down menu. Click near the resistors to locate a vertical alignment point. Right click again and choose **Align**. Enable the **Vertical About Selection Point** and **Space Equally** options. Type `300` as the **Spacing** and press **OK**. The resistors are stacked vertically. Click and drag them near the connector.

align and space components quickly with ACCEL EDA

finite rotation

32-bit accuracy offers precise rotation without round-off errors

The form factors in today's electronic products often call for odd and circular shapes. ACCEL EDA's 32-bit database provides the precision to rotate objects down to 0.1 degree, without round-off errors. This means, for example, that a component rotated 7.5 degrees 48 times, will be returned to its exact original position.

Set a custom **Rotation Increment** in the Options Configure dialog. Select one or more components (remember to clear your filter if you are using Block Selection!) then press *Shift+R* to rotate selected items in the custom increment amount.

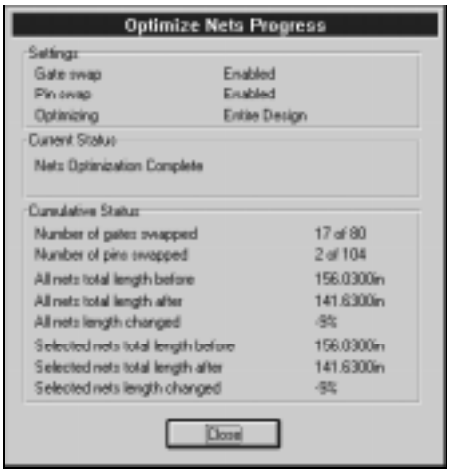
replace components

Next we'll replace a component with a similar one. Locate a polar capacitor; they're the ones with a round footprint. Double-click it and change POLCAP to CAP_POL_H in the **Type** field list box. The pattern is updated and connectivity is maintained. This powerful feature requires parts to be defined equivalently. It must be used with caution to avoid mismatching pins and pads.

optimize nets

pin and gate swapping available in Optimize Nets

As components are moved, the connections may have become less efficient than when they were originally placed. Use the **Auto** option of ACCEL P-CAD PCB's Utils Optimize Nets command to re-optimize the connections. Enable the **Pin Swap** and **Gate Swap** options to exchange equivalent pins and gates for effective routing. Equivalence is defined within the Library Manager and covered in Section 7 of this guide. Press **OK** and notice the connections change as each net is evaluated and shortened.



Manually route connections

setting up for routing

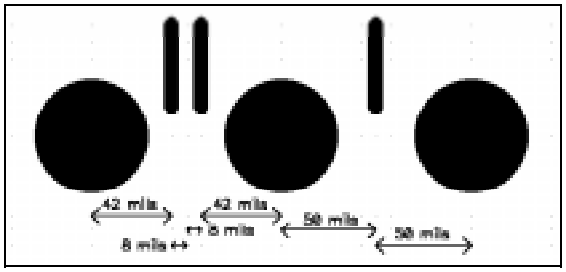
For routing, we will change some settings so we can route two lines between pads, establish clearances, and reach all signal layers. Then we'll step you through manual routing and discuss the changes that can be made to existing traces.

setting layers

Load DEMO1_U.PCB from the eval's Demo subdirectory (e.g., `c:\acceval\demo`). Use Options Layers to enable all of the layers to be used for routing plus others, like the Board layer, you would like displayed. In our case this is **Top** and **Bottom**. Routing is only permitted on enabled signal layers.

non-uniform routing grids

We previously set our grid to 100 mils for optimal placement. *Non-uniform grids* are also supported to easily route multiple tracks between pads, and for autorouting. A 42 8 8 42 grid (mils) means that grid points are located in a pattern of 42 mils, 8 mils, 8 mils, and 42 mils apart, starting at the origin. This spacing is convenient for routing one or two 8 mil traces between 60 mil pads, using 8 mil clearances, as shown:



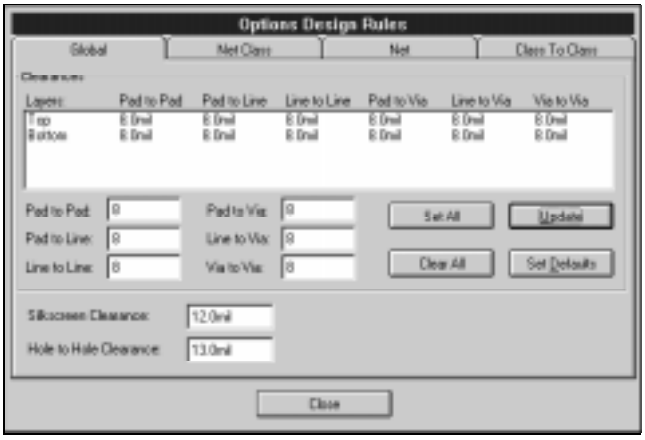
Setting a non-uniform, relative grid can be done directly on the Status line. However, because we will also be changing the relative grid origin, we need to bring up the Options Grids dialog. Choose this command and click **Relative** Mode. Type **42 8 8 42** in the **Grid Spacing** box with the values separated by spaces. Click **Add**. If you are working in mms, unit overrides must be typed for each value (e.g., 42mil 8mil 8mil 42mil).

Disable the **Prompt for Origin** checkbox, and enter an origin at **X**=`25.0`, **Y**=`0.0`. This is needed to align the relative grid with component pads (most pads are 25 mils off of a 100 mil grid with origin at (0, 0)). Click **OK** to continue.

setting clearances

To set the default global clearances to 8 mils, choose the Options Design Rules command. Click **Set All** to highlight all entries, then set the Pad to Pad, Pad to Line, Line to Line, Pad to Via, Line to Via, and Via to Via values to 8 mils. Per layer clearances are used for design rule checking, manual and interactive routing, ACCEL PRO Route, and SPECCTRA products. Click **Update**.

set up global clearances



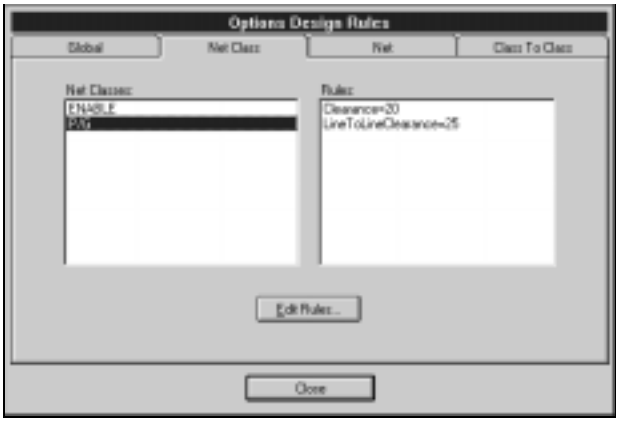
Notice the tabs reflect the hierarchy of design rules. Rules at all levels of the hierarchy may be transferred from the schematic to the PCB design in the netlist. Turn to the Schematic Design Session for a detailed description of the design rule hierarchy. The information is not repeated here.

Clearance attributes assigned to any level of the hierarchy are recognized for design rule checking (DRC), manual and interactive routing, and the SPECCTRA products. We'll look at assigning values to all the levels here.

Let's set a 20 mil clearance for the VCC and GND nets to override the 8 mil global clearance. Knowing these nets have similar attributes, we conveniently created a P/G net class (using the Options Net Classes command). Instead of assigning attributes to each net, we can assign the override clearance to the net class. Recall that net class rules take precedence over global rules. Choose the **Net Class** tab. Select the P/G class, press **Edit Rules**, and then **Add**.

ACCEL EDA's many pre-defined attributes have been placed in categories so they are easier to find. Pick the Clearance Attributes **Category** and choose the Clearance **Name**. Enter a **Value** of 12. Press **OK.** Similarly, add a 25 mil line to line clearance to the same class (choose the LineToLineClearance **Name** after pressing **Add**). This allows 25 mils between traces in the P/G class and other net traces. Exit the Attributes dialog.

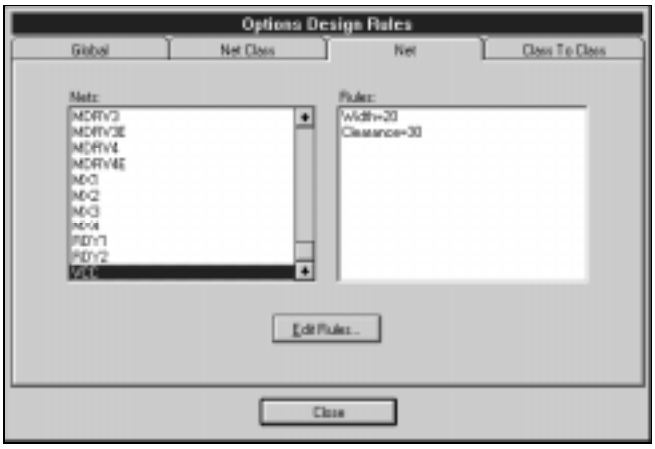
add design rules to a class of nets



Next, choose the **Net** tab and pick the VCC Net. Notice a 20 mil Width attribute was assigned to VCC so it is routed using a wider trace. Double-click Width=20 in the **Rules** box to see Width is listed in the Net Attributes **Category.** Net Attributes applied to individual nets are used for manual and interactive routing, PRO Route, and SPECCTRA products. Cancel to return to the Options Design Rules dialog.

Choose **Edit Rules**. Add a 30 mil clearance to the VCC net. The procedure is exactly as described for net class attribute assignment. Even though VCC is a member of class P/G, and that class has a different clearance, the 30 mil clearance will be used because net rules take precedence over net class rules.

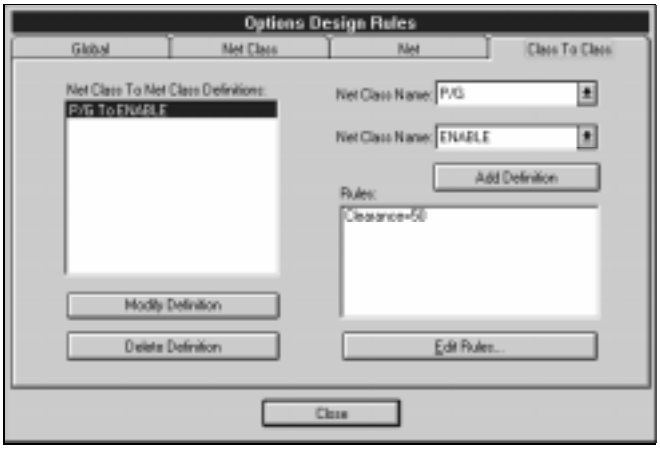
rules on nets override global and net class rules



Levels in the design rule hierarchy can be skipped. For instance, you could assign an 8 mil Width to the D7 net even though D7 does not belong to a net class.

Rules specific to the interaction of two net classes are at the highest precedence level and override all other rules. Choose the **Class To Class** tab from the Options Design Rules dialog. Add a 50 mil clearance between any net in the P/G class and any in the ENABLE class. To do this, select P/G as one **Net Class Name** and ENABLE as the other. Press **Add Definition** then **Edit Rules** to add a Clearance attribute of 50 mils, just like you did when setting the other clearances.

class to class rules have highest precedence



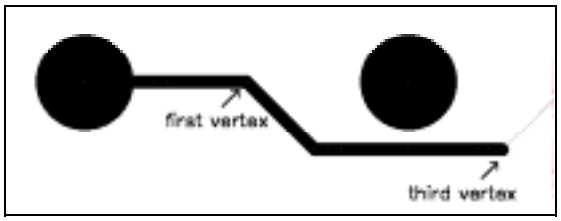
routing the connection

We're ready to route! Follow these steps and you'll be on your way to route the connections on any board:

1. Zoom so you can easily select unrouted connection lines. Rows and columns of grid points may be seen between pads, displaying convenient routing channels.

2. Select the Route Manual tool.

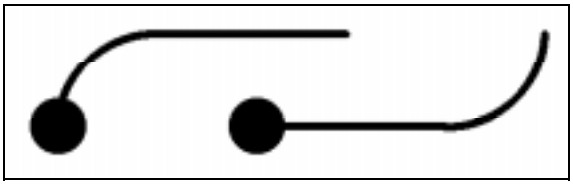
3. **Enable On-line DRC** for routing by clicking the DRC icon.
4. Change to the **Top** signal layer, using your layer shortcuts.
5. Click directly over a connection *near a starting pad.* Drag and release at a location where you want the first vertex. Then click at the location you want for the *third* vertex.



6. When the mouse is down, press the *O* key to access the desired orthogonal shape and the *F* key to toggle the vertex. Release the mouse. Notice the second vertex is added for you. The orthogonal modes include arcs, 45 degree diagonals, and 90 degree angles.

use curved trace routing for analog and high speed designs

Analog and high speed circuit designers will be amazed how easy it is to route curved traces with ACCEL PCB. Press the mouse down again to locate the next segment. Press *O* to reach the arc orthogonal mode, release the mouse, and you're placing curved traces like a pro!



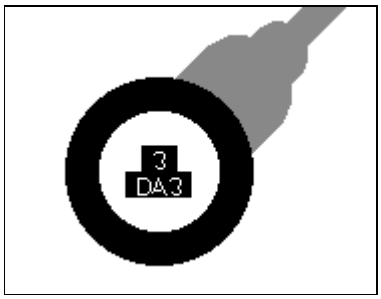
a via is placed automatically when you change layers

7. Change to the Bottom layer (press the *L* or *Shift+L* key, or use the Status line controls) to route any segments where you need to cross a blockage. Zoom in and out as needed. A via is automatically placed to connect the layers.

change line widths on-the-fly

8. Change the line width while routing a connection, before starting one of the segments. Pressing *W* (or *Shift+W*) toggles to the next (or previous) width in the list. This is convenient, for instance, to neck down when exiting a pad.

   Hint: Arrange the line width list so the line sizes used for necking down are adjacent. Then you can press consecutive Ws (or *Shift+W*) *without searching through all width entries.*

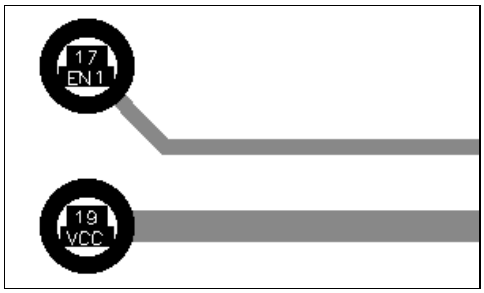


9. Create obvious clearance violations by routing too close to pads, vias, or signals. The machine beeps and an error indicator is placed for each violation. Press the *backspace* key (←) to *unwind* the offending trace. Notice that the trace and the error indicators generated by the trace are deleted. Each press of the *backspace* key backs up to the previous point. Leave at least one error in the design.

10. Press either *slash* key (\ or /) to terminate routing without completing the connection. Note the current layer has been reset and a connection line is added to show the remaining unrouted portion of the net. If the **Optimize Partial Route** option is enabled in Options Configure, the remaining connection line is optimized to connect the two closest vertices in the net that close the circuit.

    Start routing again by clicking on the connection line and, after routing close to the destination pad, click the right mouse button to complete the route all the way to the pad.

11. Route a VCC or GND connection to see how a line width assigned directly to the net is automatically routed correctly.



12. Continue practicing with orthogonal modes, placing one or two traces between pads, toggling between layers, and creating t-routes by terminating a trace on another one in the same net. Don't worry if you fall short -- DRC warns of incomplete connections. When you route directly to the destination pad a diamond shape appears, indicating routing is complete with a zero length connection.

status line information

While routing, look at the status information portion (right side) of the Status line for the measurements of your route. Routed arcs are also accurately measured.

interactive routing

Choose the InterRoute tool and select any unrouted connection at the point it attaches to the pad. Click the right mouse button and choose **Complete**. InterRoute completes the connection, avoiding obstacles, hugging adjacent traces, and adhering to design clearance rules. Notice you can also suspend or cancel the route from the same pop-up menu.

interactively complete your connection

Try another connection, this time moving the mouse away from the pad while holding the left mouse button down. InterRoute calculates a path and displays the traces in ghosted form. As you move the cursor, the ghosted tracks are moved around obstacles, maintaining proper design rule clearances. A visual indication is provided when you are bumping into another object. Traces are placed when the mouse button is released. Each subsequent click commits the ghosted traces, thus allowing you to interactively guide the path towards the destination pad.

While interactively routing, you can change layers, vias, line widths, and orthogonal modes on-the-fly the same way you do for manual routing. InterRoute allows you to erase extra copper by adding a line segment on top of an existing segment. You can always unwind segments by pressing the *backspace* key.

changing routed connections

Routed segments can be changed in a variety of ways:

- **Reroute.** Rerouting a segment is done by using the Route Manual command. Click over the segment to be changed; it becomes a ghosted connection that can be manually routed as previously described. Click to locate each new vertex, press *O* and *F* to change orthogonal modes, press the *backspace* key ← to unwind.

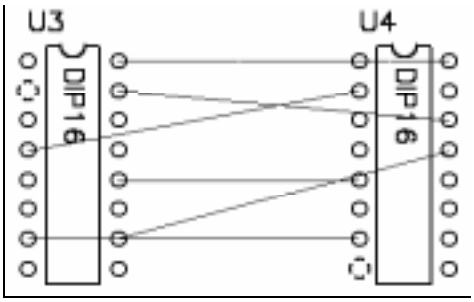
- **Mitering routes.** Route Miter turns 90-degree corners into arcs or 45-degree angles. Choose it from the menu or Toolbar. After selecting the cornering style, each left click over a 90-degree corner allows you to move the corner into a mitered angle or arc. To get optimum results, choose a finer grid than your normal routing grid before mitering.
- **Move.** Select a routed segment, then click and drag it (or its corner) to a new location. Notice that the adjacent segments are stretched to maintain connectivity.
- **Line Properties** and **Arc Properties.** Using the Select tool, double-click on any line or arc segment and change its width. Alternately select multiple nets or an entire net and use Edit Properties to change their widths all at once.
- **Delete route.** Select a segment, click right button, and choose **Delete** from the pop-up menu or press the *Del* key. The route reverts back to a connection.
- **Delete connection.** After you delete copper and it reverts to a connection, you can select and delete the connection itself. This is a drastic edit and should be used with caution.
- **Move to Layer.** Select one or more segments routed on the Top layer. Change the current layer to Bottom and choose the Edit Move To Layer command. Vias are added and deleted as needed.

Nothing beats ACCEL EDA for ease in changing the placement and shape of routed connections!

Split planes

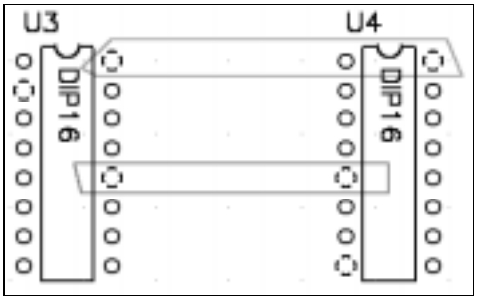
With ACCEL EDA it is simple to split a power or ground plane to support multiple signals on one plane layer. Toggle to ACCSAMPL.PCB using the list in the Window menu to practice. Zoom to the display of net connections in Section 2 of the design.

Choose Options Layers. Add a new plane layer, being sure to set the **Type** correctly before pressing **Add**. Attach net A0 and make the new layer current. After exiting the dialog, notice that pad 2 of U3 and pad 8 of U4 (both attached to net A0) indicate a thermal connection has been automatically made.



With the plane layer still active, select the Split Plane tool and create a polygon around the pads of net A1 (upper connection line) adding a new grid if necessary (see upper polygon in the diagram below). Modify the split (activate the Select tool and double-click in the area) to set the **Net** to A1 and change the **Net Plane Color**. Notice the pads in A1 are automatically tied to the split.

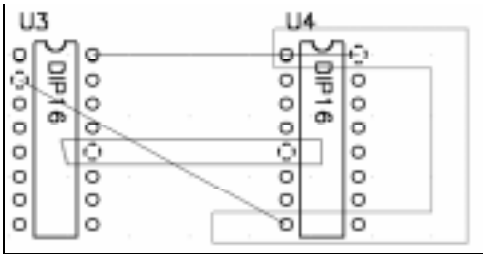
assign multiple nets to a power or ground plane with ease



Create a second rectangle around the pads of net A3 (the net connecting pad 12 of U3 with pad 5 of U4). Again modify the split, this time setting the **Net** to A3. Any number of splits can be similarly created and assigned. For clearer viewing, the extra connection lines have been hidden in the following picture.

To see that connectivity is automatically maintained, move or modify a split or move a component. Redraw the screen. A thermal is automatically displayed *only* when a net assigned to the split matches the net of the pad. Connection lines are added wherever connectivity is broken. To get the following result we modified the shape of the A1 split to exclude one of the A1 pads and include an A0 pad. Note that connection lines are added to indicate connectivity is no longer maintained.

connectivity to split plane areas is always correct - no workarounds needed!



Copper pour

One of the most powerful features in ACCEL P-CAD PCB is *copper pour*, the ability to lay down areas of copper with a back-off from tracks and pads within the area. This is commonly required for shielding. The properties for each pour are independent of other pours and can be modified individually. Creating a copper pour is a two step process. First, you place the outline using the Place Copper Pour command or icon, then modify its properties and pour it.

Move to Section 3 where we have a small design with copper pour ground planes, one on the top and one on the bottom. The planes cover most of the board area and are ready to be poured. All pour characteristics are set in the Copper Pour Properties dialog. Set the Top layer current and double-click within the pour's boundary.

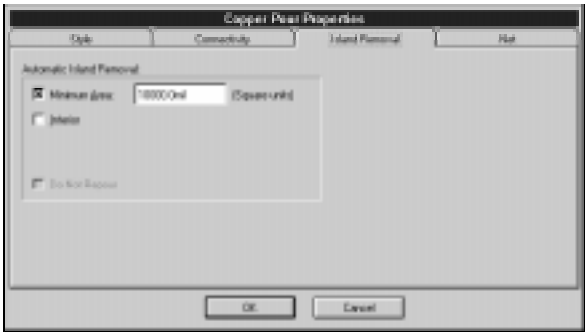
Press the **Net** tab and verify the pour is attached to the GND net. You can view or set net attributes from this dialog.

assign any net to the copper pour

When a net is assigned to a pour, component pads in that net are attached to the pour by solid or thermal relief connections. Choose the **Connectivity** tab to make the choice and set the spoke width.

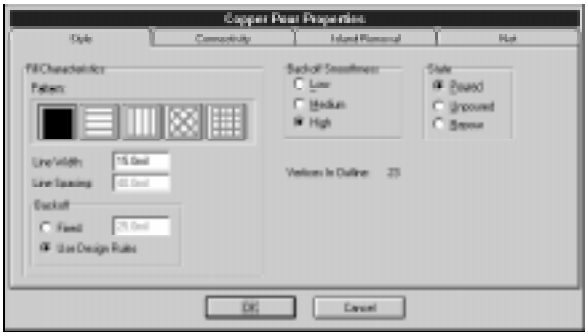
Next choose the **Island Removal** tab to indicate the desired handling of copper islands. Islands are poured copper areas that are electrically isolated from the net because of required clearances. Small islands are difficult to connect and the preferred choice is often to delete them. Enable the **Minimum Area** checkbox and enter `18000` in the **(Square Units)** edit box to automatically delete islands smaller than that area. Enabling the **Interior** option deletes all islands without an edge on the copper pour's boundary. Leave this option disabled.

control copper island removal by area, interior location, or sub-selection



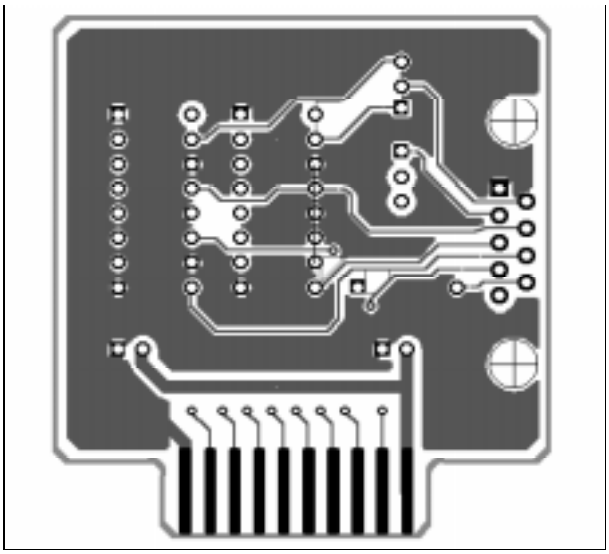
To complete the custom definition of the pour, choose the **Style** tab. Set the **Use Design Rules** option for backing off according to the hierarchy of design rules. The clearance rules for this design are simple: 12 mils for all nets except VCC which has a 30 mil clearance. Set the **Backoff Smoothness** to **High** to yield the best approximation of the pour around round pads. Low smoothness

gives a coarser representation, but is faster to process and produces smaller Gerber files.



Finally click the radio button marked **Poured** and the **OK** button, then watch ACCEL EDA work.

ACCEL EDA offers automatic island deletion, thermal connections, design rule backoff, and correct connectivity for copper pours



manually delete islands using sub-selection

ACCEL EDA also allows you to sub-select islands. Press *Shift* and select any of the remaining islands in the middle of the design. You can then delete it by pressing the *Del* key.

Zoom in to examine the pour more closely, including its thermals and the way the copper is backed off from pads and traces. The copper pour or its boundaries can also be moved.

plowing tracks, cutouts

It sometimes becomes necessary to route a track through an area where copper has been previously poured. This is a snap in ACCEL EDA. Just route the track through the copper pour and the pour's boundaries are recalculated locally. The newly added track will appear with the defined clearance around it.

To create an unpoured area within a pour, add a cutout. Use Place Cutout, then select the pour to modify and re-pour it. Copper will be poured around your cutout. ACCSAMPL.PCB includes cutouts within the copper pour on the bottom layer. These provide another method for preventing copper from being poured into intricate areas, thus avoiding unwanted islands.

Cutouts are different from keepouts. Keepouts restrict ACCEL PRO Route from autorouting within the specified area.

Design verification

Despite all of the automation controls and on-going error checking, completed designs should always be verified prior to generating final artwork and CAM files. ACCEL P-CAD PCB provides a variety of tools to help check your design against the original schematic and against your mechanical design rules.

To try out a few of the following operations, open the routed board RDEMO1_P.PCB found in the eval's Demo subdirectory.

netlist compare

At any point in the design cycle you can compare the current design against a previously generated netlist. This important step checks if any critical net or component changes were made since the netlist was generated. To see how this works, we'll make a critical change to the design and use the tools to detect it.

First change the GND signal's WIDTH from 20 to 50.

- Choose the Edit Nets command.
- Highlight GND in the **Nets** list box.
- Press the **Edit Attrs** button.
- Highlight the WIDTH attribute; press the **Properties** button.
- Enter 50 in the **Value** edit box.
- Press **OK** to exit the Attribute Properties dialog, **OK** to exit the Attributes dialog, and **Close** to return to the design.

Now let's have the tools find the discrepancy:

- Choose the Utils Compare Netlist command to locate the netlist against which to check. Press the **Netlist Filename** button and select DEMO1.NET from the eval's Demo subdirectory. Press **OK** to return.
- Set the **Netlist Format** to ACCEL ASCII if it is not already.
- Highlight the Clearance, Component, and Net **Attribute Categories** in the list box, then press the >> button to indicate these should be included in the comparison.
- Press **OK** to initiate the comparison.

An error file indicates the design's GND signal WIDTH attribute doesn't match that in the netlist. The design or netlist could be updated to remove the error. With the ACCEL EDA netlist format, any or all attributes can be verified. If the net attribute category wasn't selected, no errors would have been found.

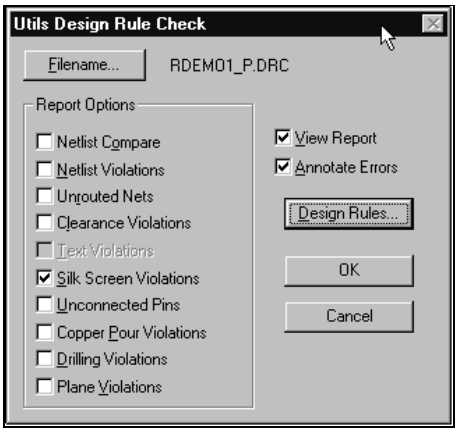
design rule checking

A complete design rule check, both electrical and physical, can be performed on the board. Choose the Utilities DRC command. The DRC check generates a comprehensive report that is output to a filename you specify by clicking the **Filename** button.

The design rules to be checked are specified by enabling specific **Report Options**. A description of each rule check can be found in the on-line help. Notice you can access the Netlist Compare utility through this dialog.

Our demonstration board has silk screen violations that we need to find. Enable **Silk Screen Violations** to catch these violations, **View Report** to output the results on-screen, and **Annotate Errors** to place error indicators for helping spot and fix problems quickly.

check your board using ACCEL PCB's comprehensive design rule check



Click the **Design Rules** button to set the **Silkscreen Clearance** to 12 mils. Close the design rule dialog boxes and choose **OK** to begin checking.

On completion, the DRC output report is opened using the File Viewer specified in Options Configure. Window's Notepad is the default. Reports can be viewed, edited, or printed from the chosen Viewer. Toggle to your design and notice that indicators have been placed at error locations. Each marker contains information including a numbered reference to its report entry. Select several markers and view their descriptions by choosing **Properties** from the right-click pop-up menu. **Next** and **Previous** buttons are available if multiple indicators are selected.

on-screen error indicators provide convenient access to design rule violations

silkscreen cleanup is simple with sub-selection

Silkscreen is easily moved using sub-selection. Switch to the Top Silk layer and press Shift when selecting the outline or RefDes to be moved. Click and drag to a new location.

In working with a real design you would resolve each error and delete the indicators one by one. We'll skip that step here and just delete them. Either block select all of your DRC Errors items and press the *Del* key, or rerun Utils DRC with no reports enabled. Rerunning the command clears the old markers.

Reports and output

We recognize that the value of your design is locked in the ability to generate high-quality output including reports and accurate artwork for board production. ACCEL EDA excels in this area with its powerful, easy-to-use features; like those you've already seen for placement and editing.

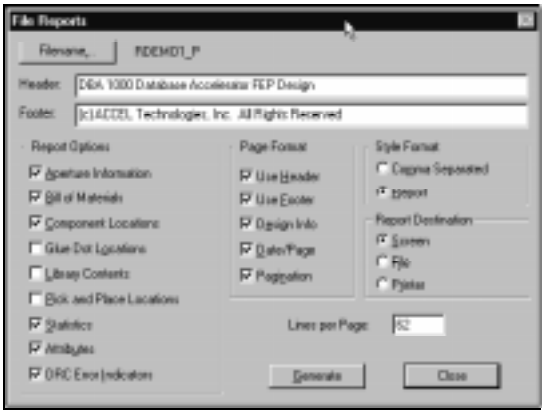
In the eval, output can only be generated for unmodified designs. If you make changes to the supplied PCB files before generating output, you will be notified that output can't be generated. Close the modified design, and open the original again.

reports

ACCEL PCB generates a variety of comprehensive reports to help you verify the integrity of your design and document your work. The format and content of the available reports were designed by PCB designers and service bureaus.

Reports can include custom headers and footers, date/page output, and data from the File Design Info command. Other options specify format, pagination, and the output medium.

generate ACCEL EDA reports to document your design professionally



Choose File Reports and enable a **Report Options** box for each report you wish to generate. Choose the **Report** format and send the output to the **Screen**. Click **Generate** to produce the reports.

Comma-separated ASCII report files can be output for loading into your favorite word processor, database manager, or spreadsheet for further editing or formatting.

printing your artwork

In ACCEL EDA, we've paid particular attention to generating the highest quality artwork for the wide variety of devices supported by Microsoft Windows as well as Gerber-format photoplotters. Our straightforward approach and intuitive dialog boxes take the mystery and frustration out of generating artwork, photoplot files, and N/C drill files.

ACCEL PCB provides all you need to print exactly what you want. First you'll set up the printer, then create a print job for each piece of artwork to be generated. Finally, you select any number of print jobs and generate the output.

We'll demonstrate using our sample board ACCSAMPL.PCB. Make it current by choosing it from the list of open designs provided under the Windows menu. Use the File Printer Setup command to choose your printer, paper size and source, orientation, number of copies, and other print options.

setting up your print jobs

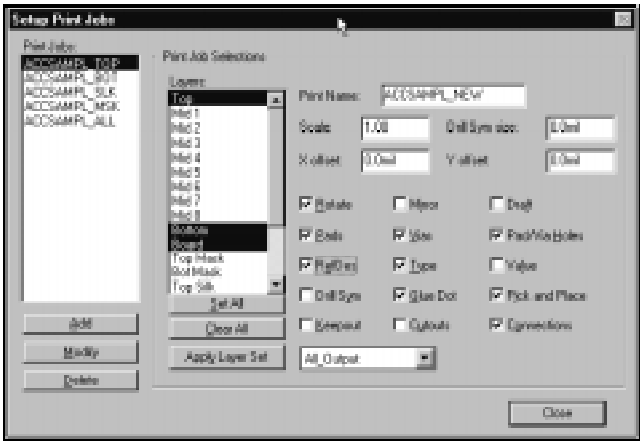
Choose the File Print command. The **Print Jobs** list box shows the jobs that are already defined for our sample board.

select print jobs to output in the File Print dialog box

We designed this dialog box to make it easy to examine or change an existing job, or to create a new one. Notice you can print the entire database, the contents of the current window, or the selected region. The push buttons on the right are positioned in the order that you would use them. Click **Setup Print Jobs**. Here you set up your print options and items to be including in the output.

Select ACCSAMPL_ALL in the list box. You'll see the characteristics defined for that job on the right. To change the job, update the options and click **Modify**. Creating a new print job is just as easy: choose your options, type a new job name in the **Print Name** box, and click **Add**.

set your printing options in the Setup Print Jobs dialog box



layer sets speed layer selection for output, routing, and display

Before exiting the dialog we should take a look at layer sets. Sets of layers can be created in Options Layers to activate nets that are frequently used together for routing, display, or output generation. Several layer sets are pre-defined for you.

Pick a set name from the combo box next to the **Apply Layer Set** button, then apply the set. Notice in the **Layers** box that a pre-defined set of layers are activated. Multiple jobs can be set up before you press **Close** to return to the File Print dialog.

auto drill assignments speed output generation

Next, click **Drill Symbols**. We could manually assign each hole size to a drill symbol. Instead, click **Automatic Assign** to assign them all instantly, then exit the dialog.

ACCEL EDA Tip

One important note on drill drawing output is that you must select *exactly* those layers to be drilled for each print job. The output must match the required manufacturing steps. For example, on a four layer board with one through-hole and one buried via, two jobs would be needed. One drill job should have only the middle two layers selected. A second job would be defined with all four signal layers selected. This would match the manufacturing steps of laminating the middle layers and drilling them to create the buried via, and then adding the outer layers and drilling again to create the through-hole via.

Set your output colors using the dialog accessed by clicking the **Colors** button. Return to the File Print dialog. Click to highlight the names of jobs to run. Then, click **Generate Printouts** to produce the print jobs on your printer.

CAM file generation

The process for generating Gerber-format photoplot files is very similar to that for generating prints. You determine the contents of the photoplot files, select one or more of them, and generate the output. With Gerber files, however, you must make an extra step of mapping apertures to items on your design. ACCEL EDA's automatic aperture assignment makes this easy and quick.

Gerber output

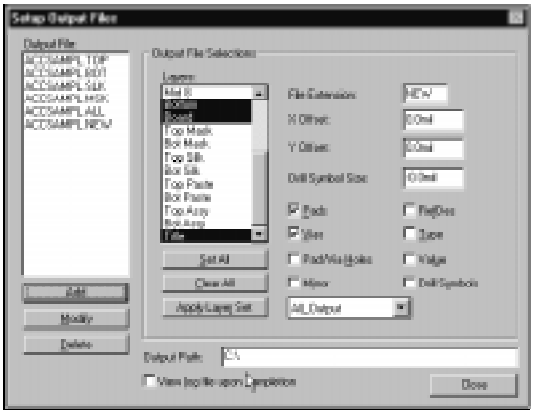
Choose the File Gerber Out command. Again, the buttons on the right of the dialog box are positioned to lead the designer through the step-by-step process of generating photoplot files.

all of the functions for generating photoplot files are accessed from one handy dialog box

setting up photoplot files

Click on **Setup Output Files**. Notice how similar the dialog is to the one we just visited. Create a new output job by setting output file options, including the file extension, and click **Add**.

set your options for photoplot files in the Setup Output Files dialog box



Click **Close** to return to the File Gerber Out dialog box.

setting up apertures

Next, click on **Apertures** to assign a photoplot aperture to each item on the board. To save time and hassles, just click **Auto** in the **Automatic Describe/Assign** section of the dialog box. ACCEL EDA will automatically assign an aperture to each item. You can then edit any of the assignments if you wish. Click **Close** to complete aperture definition.

automatic aperture assignment saves time

File Gerber Out also provides access to assigning drill symbols. These were already assigned for printing and don't have to be redefined here. Click **Gerber Format** to set the format for your output. Finally, select one or more of the output files by highlighting those names in the **Output Files** list box. At this point you would click **Generate Output Files** to produce the photoplot files. Gerber generation has been disabled in the eval.

viewing photoplot files

Perhaps no other function in ACCEL EDA provides a good night's rest as much as the photoplot file viewing facility. By viewing the files just generated on-screen, you can be assured that your aperture selection and options were correctly set.

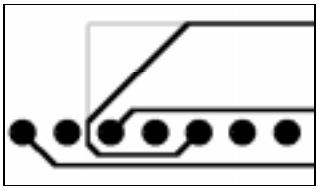
view your Gerber output and your original design at the same time

A particularly powerful feature is ACCEL EDA's ability to *slide* a Gerber file into a layer while the original design is open. As with superimposing two supposedly identical overheads, discrepancies become quickly obvious. You can also read in multiple Gerber files to view a composite of the design.

A Gerber input file can be loaded into any design that shares aperture assignments. If you want to load Gerber into an empty design, start with one that has matching assignments and use File Clear. This command deletes items but keeps the environment, including your aperture assignments.

Open RDEMO1_P.PCB again. Assign Gerber apertures by running File Gerber Out, clicking the **Apertures** button and then **Auto**. After your apertures are set, choose File Gerber In and load RDEMO1_P.TOP or RDEMO1_P.BOT from the eval's Demo subdirectory. The contents of each Gerber file are written to a separate layer. By viewing a design layer and its associated Gerber data, you can tell if anything has been changed since the Gerber output was generated. Be sure to look at both views: when the design layer is current and when the Gerber layer is current. This will show if data is missing on either of these layers.

identify changes made since Gerber generation



generating N/C Drill files

N/C Drill files are also easily generated. This procedure is very similar to that for creating prints and photoplot files.

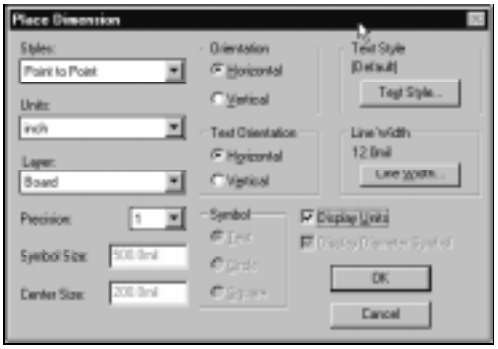
Choose the File N/C Drill command. Set up output files, assign tools, and set the drill file format all from this one dialog box. Recall the ACCEL EDA Tip (a couple of pages back) on selecting layers for getting proper drill output.

Select the output files, click the **Generate Output Files** button, and watch ACCEL EDA go to work.

fabrication and documentation

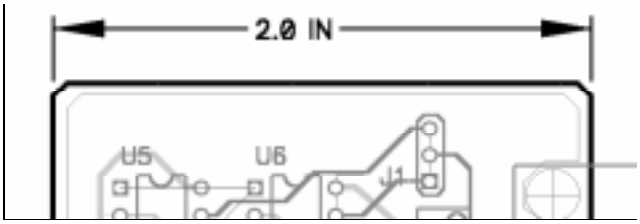
Adding dimensions for fabrication is done within ACCEL EDA. Return to ACCSAMPL.PCB and zoom to view Section 3 of the design. Choose the Dimension tool and click in the workspace to bring up the Place Dimension dialog. Make choices for the available options and press **OK**.

ACCEL EDA offers a variety of dimension styles



With the above choices, and picking the design's edges on the Board layer, we produced the following results.

clearly annotate your design for manufacturing



ACCEL EDA has the tools to complete your fabrication and assembly drawings, and generate reports for pick and place locations, glue dots, and a Bill of Materials. You'll find built-in DXF input and output commands for interfacing to mechanical design systems. The licensed version of ACCEL PCB allows you to cut portions of your design to the clipboard as a Windows Metafile bitmap for pasting directly into your design documentation.

section review

In this section we have shown you how to:

- Set up a design in preparation for component placement.
- Create a board outline and load a netlist to have components automatically placed in the workspace.
- Manually route connections with the various orthogonal modes, including curved trace routing, and edit them.
- Assign multiple nets to a plane.
- Add and update copper pours, with user defined backoffs, patterns, and net assignments.
- Verify your design with netlist comparison and DRC.
- Generate reports, printed output, photoplots, and N/C drill files. Also, view photoplot files on-screen.

As you can see, ACCEL EDA has the tools to help you lay out sophisticated printed circuit boards. In the next section we'll show you how to prevent hours of tedious labor by using ACCEL PRO Route, the optional high-performance autorouter.

SECTION 6

Integrated Autorouting

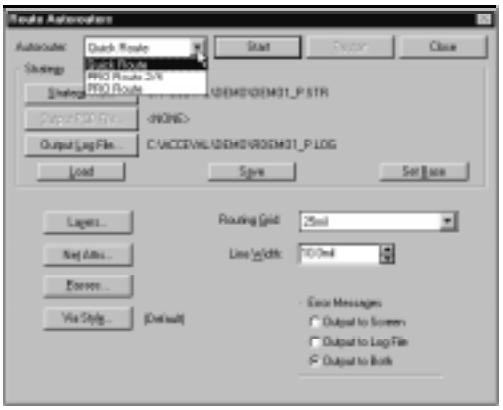
A wide range of autorouters, representing four different technologies, are accessed directly from within ACCEL PCB. There's one to meet your needs *and* your budget. You'll find our QuickRoute maze autorouter and our shape-based interactive router, InterRoute, built right into ACCEL P-CAD PCB. The ACCEL PRO Route and SPECCTRA high-completion autorouters are powerful options available for enhancing your layout system further.

In this section, we'll introduce each of the autorouters and then demonstrate our high performance, rip-up and reconstruct router, ACCEL PRO Route. Each is just a few mouse clicks away, making it easier than ever to iterate towards a completed design.

A Common Router Interface

Load DEMO1_P from the eval's demo subdirectory if it is not already loaded. Choose the Route Autorouters command. This context-sensitive dialog box is your entrance to all of the autorouter interfaces found within ACCEL PCB. We'll examine each in turn.

set all autorouting options in one handy place with the Route Autorouters command



Click the drop down **Autorouter** list box and notice interfaces are available for QuickRoute, PRO Route, PRO Route 2/4, and SPECCTRA. Cycle through the choices to see how the context-sensitive lower portion switches to present options available to the selected router.

This common interface simplifies learning and makes it easy to switch between the routers as routing demands change within a project or from project to project.

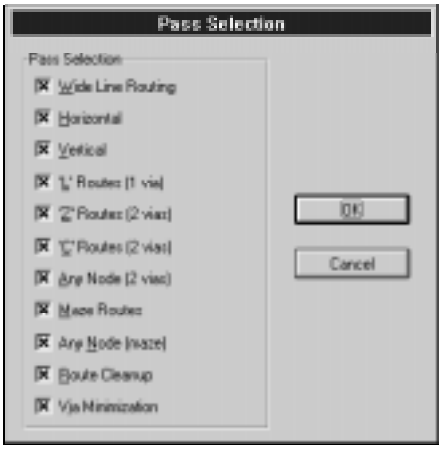
QuickRoute

QuickRoute is a gridded maze router included with ACCEL P-CAD PCB and ACCEL Tango PCB at no additional cost. This basic utility offers tremendous productivity advantages over manual routing. It's a handy tool for verifying placement feasibility, completing boards of moderate complexity, or initially routing more complex designs. QuickRoute also has separate manufacturing passes to improve the design after traces have been placed.

Choose **QuickRoute** from the Autorouter list box. In turn, examine the dialogs accessed by pressing the **Layers**, **Net Attrs**, and **Via Style** push-buttons. These are the familiar ACCEL PCB dialogs, provided here as a convenience during routing. The data is shared with PCB; changes made here will be reflected in the dialogs accessed through other ACCEL PCB commands, and vice versa.

Press the **Passes** push-button. Separate passes are available for routing wide traces, cleaning up the design, and via minimization.

select routing passes in the Pass Selection dialog



QuickRoute allows routing with pre-set combinations of trace width, clearances, and routing grids. Additional information is provided in the on-line Help for the Route Autorouters command and will not be covered here.

When all options are assigned as desired, simply press **Start** to set the autorouter in motion! QuickRoute is enabled in this evaluation and although we will not be guiding you through a demonstration, you can experiment with it on your own. Of course, this version will not save the routed results.

SPECCTRA Autorouters

Cooper and Chyan Technology, Inc.'s (CCT's) SPECCTRA shape-based batch and interactive routers represent the latest in autorouting technology. Available as optional companions to ACCEL PCB, the AutoRoute products are extremely efficient in real-estate usage, often reducing layer requirements for a design. In general, shape-based routing requires less memory than grid-based routers and is, therefore, the preferred choice for boards that are physically large and those with many layers. SPECCTRA offers a particularly rich set of router commands and design options, all accessed from within ACCEL PCB.

The SPECCTRA AutoRoute products vary in the number of layers and pins that can be handled. SP4P is for designs having up to 4 layers and 4000 pins. SP2 routes boards of one or two layers and any number of pins. Finally SP10 has no practical layer or pin limit.

Options are available for Advanced, DFM/DFT, Hybrid, and Fast Circuit needs. Contact ACCEL Sales for more information or for a full-capability evaluation copy of these products.

interactive route editing allows plowing, shoving, and ghosting

ACCEL also offers CCT's powerful Interactive Routing module, EditRoute. EditRoute revolutionizes the editing process with plowing, shoving, and ghosting. Pushing wires aside and routing around pins during placement, shoving wires and vias (even if they must jump over other pins and vias), and multi-level undo are all part of EditRoute. EditRoute is available in the same unlimited, and two and four layer versions as AutoRoute. The interface is also shared.

To examine the autorouter interface, choose **SPECCTRA** from the **Autorouter** list box.

the context-sensitive Route dialog presents options applicable to the selected autorouter

The SPECCTRA autorouters are controlled by router commands supplied in a DO File. Click the **DO Wizard** push-button for help in creating a command file. Select various commands from the drop down **DO Commands** list box and notice the right portion of the dialog changes to display valid arguments for each selected command. This context-sensitive dialog helps ensure your command arguments are valid and syntactically correct.

the DO File Wizard puts SPECCTRA commands at your fingertips

You add a new router command to the DO File by selecting the command from the list box, filling in the arguments in the right portion of the dialog, and pressing **Add Before** or **Add After**. The new entry is added to the **DO File** list box.

Since SPECCTRA command documentation is not provided with this eval, you do not have sufficient detail to complete a DO File manually. Instead, press the **Auto Create DO File** button and notice the **DO File** list box is automatically filled in. Entries can then be added, modified, or deleted. Press **OK** to exit the dialog.

Next, press the **Net Classes** button to view or create named classes of nets. You'll find a couple of classes have already been added to this design.

Back in the main Autorouters dialog, you may also want to examine the options available in the **Command Line** dialog. This autorouter is not included with this evaluation.

ACCEL PRO Route and PRO Route 2/4

ACCEL PRO Route and ACCEL PRO Route 2/4 are sold as optional autorouters for ACCEL P-CAD PCB and ACCEL Tango PCB. They may be installed with the PCB program or added later as an upgrade. With these autorouters, you'll iterate towards an optimal design faster than you ever imagined.

ACCEL PRO Route 2/4 is ACCEL PRO Route technology for designs having one or two signal layers, or those with up to 4 layers and 4000 pins. With that exception, the products are identical and any description applies to both.

Some of ACCEL PRO Route's advanced features include:

- Expert-system technology to select optimum routing configurations for you automatically.
- Reconstruct algorithm iterates towards 100% completion.
- Intelligent cleanup algorithms produce high-quality, manufacturable designs.
- True multi-layer autorouting with simultaneous routing on all enabled layers (not just layer pairs).
- Uniform and non-uniform grids with off-grid capability for enhanced performance and greater pad placement freedom.
- True diagonal routing, a sophisticated capability provides high completion, reduces the number of vias and connection inches, and produces more manufacturable results.
- Intelligent via placement for higher completion rates, and automatic via placement for surface pads and edge connectors on multi-layer designs.
- Surface mount design with fine-line routing, routing to both top and bottom pads, and smart via fanout.
- Comprehensive report detailing the results of each session.
- Integration within ACCEL PCB for convenience and enhanced productivity.

A minimum of 16 MB of memory is recommended for ACCEL PRO Route. Memory requirements increase with larger and more complex design.

We will now step through a full demonstration of ACCEL PRO Route. We think you'll be impressed with the output quality and how quickly ACCEL PRO Route completes your designs. The eval version will not save the routed results, but all of the routing statistics can be found in the resulting report file.

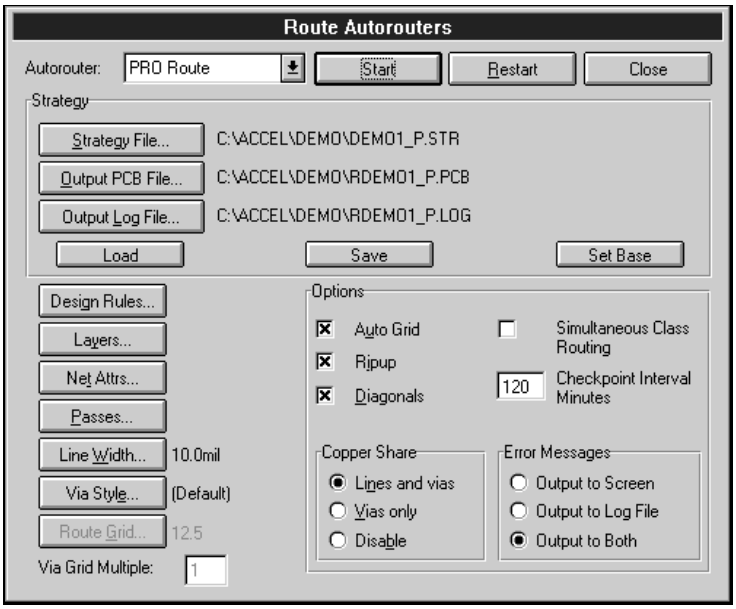
Setting up ACCEL PRO Route

We took the demo board from the last section and pre-routed power and ground for you. Open DEMO1_P.PCB, from the eval's Demo subdirectory (e.g., `c:\acceval\demo`).

pre-routes and keep-outs

If you have done any manual routing on a board, don't worry. ACCEL PRO Route will respect your work as pre-routes. You can also designate keepout areas (where the router will not route) on any layer by using the Place Keepout command.

Choose the Route Autorouters command, and select PRO Route from the **Autorouter** list box. From here you have direct access to dialogs that set up design rule clearances, line widths, routing layers, via styles, net attributes, passes, and routing grids.



Many of the sub-dialog boxes will look familiar. That's because ACCEL PRO Route uses the same dialogs to set up grids, line widths, clearances, and layers that ACCEL PCB provides for manual routing and rule checking.

route configuration

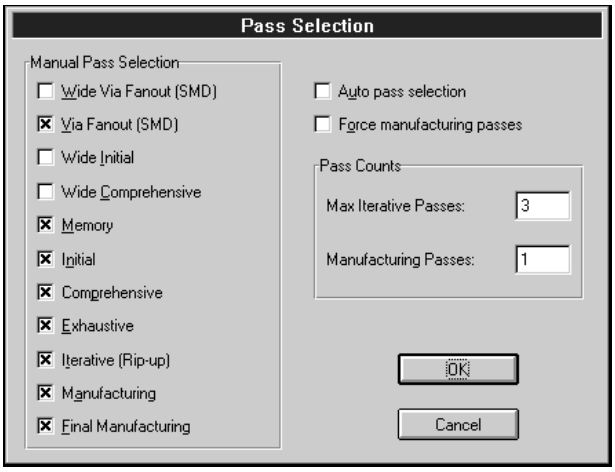
The following is a brief description of each item in the Route Autorouters dialog box for PRO Route.

- **Strategy File.** Your routing options can be saved in a strategy file which can later be loaded for re-use. This is particularly helpful for testing different routing strategies on the same board. For our example, the default strategy file DEMO1_P.STR is presented in the dialog since we have DEMO1_P.PCB loaded.
- **Output PCB File.** The file name for the routed design. Your current design is autorouted and automatically saved to this file name. *Note: not enabled in the eval version.*
- **Output Log File.** ACCEL PRO Route produces a comprehensive statistical autorouting report that is written to the file specified with this button.
- **Load.** Loads a previously saved strategy file.
- **Save.** Saves route strategy data to a file for later reference.
- **Set Base.** Automatically sets the Strategy, Output PCB, and Log file names, using the design file name as a base.
- **Clearances.** This is the same dialog used for DRC in PCB. Pad to Pad, Pad to Line, Line to Line, Via to Line, Pad to Via, and Via to Via clearances can be set per layer.

experienced users have total control over routing strategy, while beginners can simply choose "Auto" and let ACCEL PRO Route's expert system technology do the rest

- **Layers.** This button is also shared with PCB. Plane layers are specified and signal layers are enabled for routing. The autorouter will not route on disabled layers. You can also establish a routing bias for signal layers, either **Horizontal**, **Vertical**, or **Auto** (the router chooses the best direction).
- **Net Attrs.** Choose this button for the Edit Nets dialog box, where you can set routing widths, via styles, maximum vias, ripup, and routing control per net.
- **Passes.** Click this button to indicate the type and number of passes desired. Check **Auto Pass Selection** to have the router choose routing passes for you, or clear the checkbox to manually select the pass types. You can also set the number of iterative and manufacturing passes in this dialog.

set up your own strategy for routing passes or click Auto



- **Line Width.** This is used to set the default line width for all routing except where you establish an alternate width using the **Net Attrs** option.
- **Via Style.** This button accesses ACCEL PCB's via style dialog. Choose the via you wish to use as the default to be placed during autorouting. Alternate via styles can be set per net with the **Net Attrs** option.

ACCEL PRO Route will route on a uniform or non-uniform grid, plus off-grid when needed, to achieve superior results

- **Route Grid.** This button is used to manually set a grid. It is not used if the **Auto Grid** option is set. You can choose a uniform or non-uniform routing grid from the list or click on **Add** to add another grid to be used for routing. The autorouter uses the Absolute routing grid. Non-uniform grids offer the same routing power using fewer grid points, so the router can use less memory and autoroute faster.
- **Via Grid Multiple.** ACCEL PRO Route allows for vias to be placed on a coarser grid than tracks, thus eliminating blockage of routing channels. You can choose the via grid as a multiple of the routing grid. For example, if you are routing on a 25-mil grid and choose a via grid multiple of 4, vias will only be placed on a 100 mil grid. This option is not available if the **Auto Grid** option is enabled.
- **Copper Share.** Copper sharing (also called T-routing) is a routing technique that saves connection inches, increases completion percentages, and reduces via count. You can enable copper sharing to lines and vias, or vias only, in the **Copper Share** box.

- **Options.** Enable **Auto Grid** if you want ACCEL PRO Route to choose the optimal routing grid for you. It will select the routing and via grids based on the type of components on the board, their pad size and pitch, the placement grid, your selected line width, and design rule clearances. Check **Ripup** to allow the router to globally rip-up and reconstruct your pre-routes; leave it unchecked if you want your pre-routes to remain fixed. Check **Diagonals** to enable 45-degree routing; leave it unchecked for 90-degree routing. Enabling the **Simultaneous Class Routing** box routes multiple net classes in the same pass. This is used in special cases to achieve higher completion rates. The **Checkpoint Interval Minutes** value is the maximum amount of time the router will work before it creates a checkpoint file.

Go ahead and click the options to view their respective dialog boxes. Save your desired configuration in a strategy file, by clicking **Save**. Then choose **Close** to exit the dialog.

Running ACCEL PRO Route

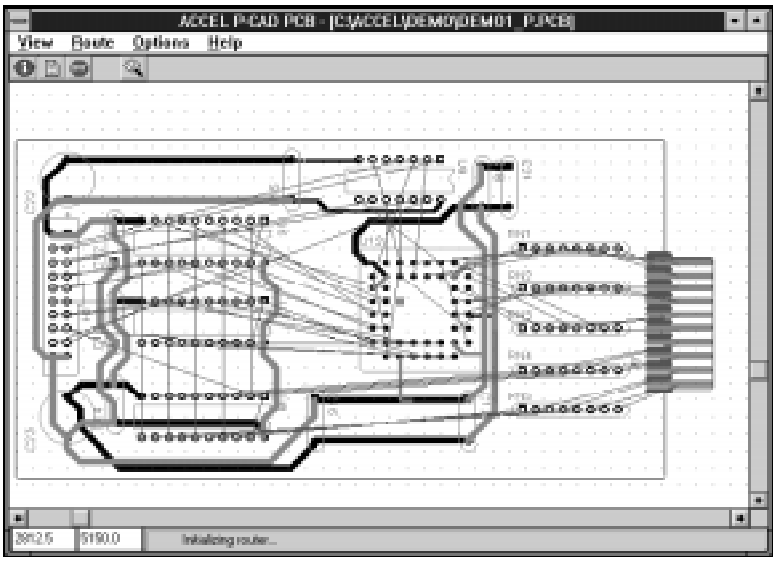
Now we are ready to route and roll! Choose the **Start** command to get things going. Sit back and enjoy your coffee, but don't go away. This board will route to 100% completion with three manufacturing improvement passes in under 3 minutes (on a 90 MHz Pentium computer).

When the router begins a new menu and Toolbar is displayed, providing commands that are accessible during routing. These include commands to control the display of your board, track route performance, and control the autorouter itself.

the ACCEL EDA Route toolbar

The Toolbar includes buttons for the most common operations during routing. From left to right, they are: **Info**, presents a dialog with current statistics on the routing job; **View Log**, used to view your output log file while routing continues; **Cancel**, provides a variety of options to control routing and save the routing results (licensed version only); and **Zoom Window**, for zooming in on the board during autorouting.

the menu and Toolbar offer autorouting options when ACCEL PRO Route is running



Watch the Status line for messages. It keeps you informed of ongoing routing activities. You'll first see initialization and pre-pass messages. Next, the various routing passes begin.

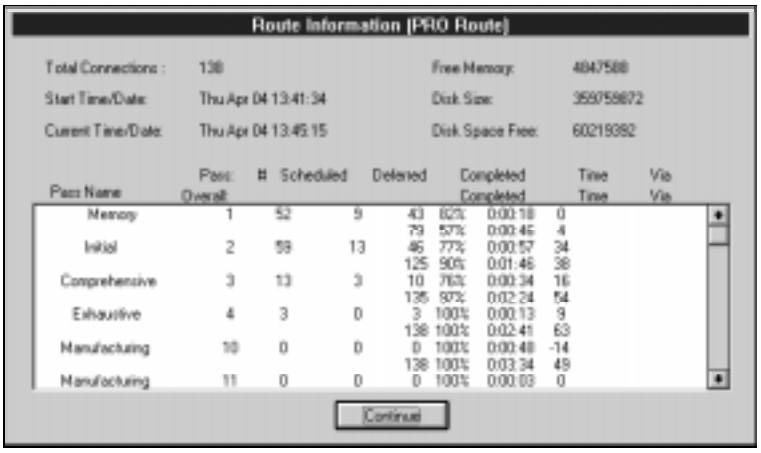
ACCEL PRO Route has three basic phases of routing (each with their own passes): a *constructive* phase that adds traces to the board; an *iterative* phase that removes and re-places connections to converge on 100% completion, and a *manufacturing* phase that improves the board for manufacturing.

like an experienced designer, ACCEL PRO Route creates boards which look clean and are highly manufacturable

The intelligent cleanup algorithms in ACCEL PRO Route create high-quality routed boards that are cost-effective and reliable. The program straightens traces and uses true diagonals to create improved manufacturing yields with fewer vias and shorter total trace lengths. Other manufacturing functions include trace spreading, acute angle removal, and improved pad entry (through the corners of square pads and the ends of rectangular or oval pads). True memory patterns on a single layer are generated. These routing characteristics improve electrical performance, lower cost, and result in enhanced board aesthetics.

During routing, press the **Info** button from the Toolbar to view ACCEL PRO Route's pass information.

view the status on your route job at any time with the Info command



temporarily pause and resume autorouting

ACCEL PRO Route is fully interruptible. Any route job may be paused and resumed later. If you want to temporarily halt the router, use the Route Pause command. While paused, you can still zoom and examine router status. The paused autorouter frees resources for other Windows programs. Choose Route Resume to resume routing.

If you wish to stop the router to make changes to the placement or to edit routed tracks, choose the Route Cancel command from the menu or Toolbar. In the licensed version of ACCEL PRO Route, Cancel also allows you to suspend the route. The resulting checkpoint file can later be restarted by pressing **Restart** from the Route Autorouters command. When routing is complete, the ACCEL PCB editor screen is restored.

In the eval, autorouted results cannot be saved. The report file, however, can be. Select Route View Log or click the Toolbar button to view the report file during routing or after a routing job is done. It includes your selected strategy, a complete rundown on the results of every pass, and final board statistics. The report file holds the key to measuring the productivity gains you'll enjoy with this autorouter.

what makes ACCEL PRO Route such a good router?

Now that you have seen ACCEL PRO Route operate, you may be wondering what it is that makes the program produce better boards in less time than the competition.

reconstruct achieves 100% completion and also provides manufacturing improvement

ACCEL PRO Route's *reconstruct* algorithm tends to solve simple blockages by making changes in close proximity to the blockage and solves larger problems with a more global topology approach. The software analyzes various sets of signals that can be moved to solve the blockage, and chooses a set that handles the problem. The router removes the chosen set of signals, and re-places them in a way that removes the signal blockage, often selecting a completely different path. No connection is ever removed without being re-placed. The results: the percentage of the board completed never goes backward, and the task of producing a quality design is accomplished significantly faster than with competing rip-up or push-and-shove autorouters.

The reconstruct technology also requires significantly fewer iterations to automatically route 100% of a PCB. And, the manufacturing improvement phases insure that trace lengths, vias, and layers required are minimized.

put ACCEL PRO Route to the test by running the benchmark boards or your own designs

Several boards, with a variety of technologies, are included with this evaluation package so you may fully appreciate the power, speed, and resulting quality of designs routed using ACCEL PRO Route. We encourage you to autoroute these, or designs of your own, and compare the results to any other autorouter you may have seen or used.

section review

In this section we have shown you how to:

- Use the common autorouter interface
- Set up QuickRoute
- Set up SPECCTRA autorouters
- Set up ACCEL PRO Route for optimum autorouting results
- Run ACCEL PRO Route and study its results.

At this point in a typical PCB layout job, the designer reviews the work done by the autorouter, tweaks any tracks that are not optimum, and manually routes any connections left uncompleted by the autorouter. A design rule check is done on the completed layout. Then the artwork (plots, prints, or photoplots) and CAM files are generated.

In the next section, we will review some of the powerful integration features of ACCEL EDA, including ECOs, cross-probing, and shared libraries. After that, we'll call it a day.

SECTION 7

Linking the Pieces

The integration features of ACCEL EDA make it particularly valuable for creating complex designs. Forward and backward ECOs, cross-probing, and shared libraries all allow you to iterate more quickly and accurately towards your final design solution. Here we'll see how ACCEL Schematic and ACCEL PCB are tightly linked.

Engineering change orders (ECOs)

ACCEL EDA offers forward and backward ECO capability

One of the most difficult, yet crucial, aspects of PCB design is keeping the schematic and PCB synchronized throughout the iterative design cycle. ACCEL EDA offers full forward and backward ECO capability to help you make sure your documents remain matched. In this section we'll show you how to make changes to the schematic and have them reflected in the PCB. ACCEL EDA will work equally well in the opposite direction; making changes to PCB that are taken back into the schematic.

ACCEL EDA records the following activities:

- reference designator changes
- net name changes
- net addition and deletion
- net node addition and deletion
- part addition, deletion, and modification
- component addition, deletion, and modification
- attribute addition, deletion, and modification

Matching Schematic and PCB design files have been provided in the eval's Demo subdirectory (e.g., `c:\acceval\demo`). Open DIGDEMO.SCH in ACCEL Schematic and DIGDEMO.PCB in ACCEL PCB. If these files were opened and modified, bring up clean copies. Use Library Setup to open DEMO.LIB in both, if they're not open. Then maximize ACCEL Schematic.

exercise #1: creating ECOs

We will rename a net, add a net connection, and delete and add a capacitor. The activities will be recorded and imported into PCB.

1. Enable the ECO recorder to capture changes important to PCB. In ACCEL Schematic, press the ECO Toolbar icon or choose Utils Record ECO and turn the **ECO Recorder On**.
2. To rename a net use Edit Nets. Check that the **All Nets** filter is enabled. Scroll to find NET00116, select it, and click the **Rename** button. Enter PWROUT_1 as the new name, then close the dialog.
3. Next, we'll add a connection. Set the current sheet to Sheet1 and the current grid to 100mils. Zoom in to the lower rightmost parts on the sheet. Using Place Wire, connect U24, pin 17 and U20, pin 7.
4. Finally, let's replace a non-polar capacitor with a polar one. Using the Edit Parts command, select part C5 in the parts list and click **Jump**. Delete this capacitor and the wires connecting it to the horizontal power nets.

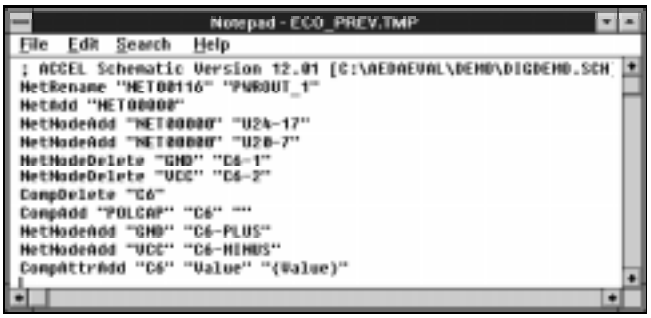
parts can be automatically wired to existing nets

Place a POLCAP in the same location, rotating as needed, but with its pin touching the upper horizontal wire. Select the capacitor and move it down so the lower pin touches the lower wire. Move it again to a center position. Notice the capacitor was automatically wired to the power nets. The reference designator was also reassigned as C5, the first available designator.

Now we need to export the changes to PCB. Turn off the ECO recorder (answer **Yes** to the warning message). Choose Utils Export ECOs and click **View Pending ECOs**.

In the report, a semi-colon (;) indicates the line is a comment or an ECO that has already been applied. Look for requests to rename a net, add a net with two net node connections, delete a non-polar capacitor and its two net node connections, and finally add a polar capacitor with its two connections.

view your engineering changes before applying them



After viewing, close the File Viewer and choose the **Save ECOs Now** button, clicking **Yes** in response to the warning message. Accept the default filename, then click **Append ECOs to File**.

exercise #2: importing ECOs

Toggle to the PCB to import the changes. You might want to locate the original capacitor, C5, since it will be deleted and impossible to find later. Choose Utils Import ECOs. Select the ECO file you just created (e.g., DIGDEMO.ECO) and click **OK**. Four things happen:

1. The original C5 capacitor and its adjacent connections are deleted. You would want to clean up remaining unconnected copper.
2. A new capacitor is added to the workspace in the upper left corner outside the board outline. Connection lines tie the pads to appropriate nodes in the nets. Move this onto the board using a 100 mil grid, making space and cleaning up adjacent silkscreens as necessary. Your new connections will have to be manually or automatically routed.
3. A connection line has been added between U20, pin 7 and U24, pin 17. This would also have to be routed.
4. Net NET00116 has been renamed to PWROUT_1, as seen by scanning **Net Names** in the Edit Nets command.

back annotation

ECO updates are just as easy when changes are made in PCB and brought back to Schematic. This is a handy facility that might typically be used to renumber components in a PCB design and update the data back in Schematic. New items are placed on an ECO sheet (instead of outside of the board outline as in PCB), and can then be cut and pasted onto any sheet of the Schematic. This eval does not support cutting and pasting, so this feature cannot be demonstrated here.

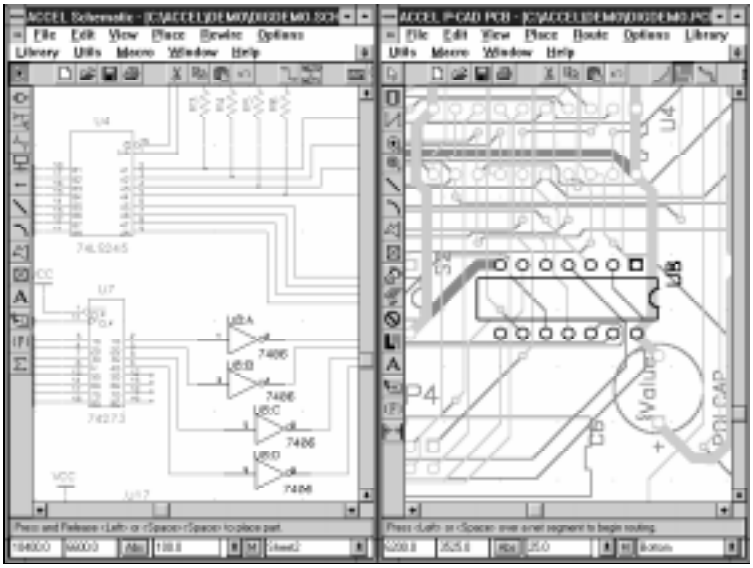
Cross-probing

Resize the PCB and Schematic applications to view them both at the same time. One Windows shortcut is to iconize or close all applications except ACCEL Schematic and PCB. Double-click in the Windows background and choose Tile.

For this exercise you must be running the evaluation versions of both applications. Mixing a full package with an eval may not allow cross-probing to work properly. Use the View Extent commands to view the full schematic and entire layout. In both applications, choose the Options Configure command and enable **DDE Hotlinks,** if they are not already enabled. This verifies that links are established for exchanging data.

Select any component in PCB, and highlight it by clicking right and choosing **Highlight**, or by using Edit Highlight. The corresponding Schematic part (or parts) will be immediately highlighted. Zoom in for a better view.

cross-probing lets you easily locate components and nets across applications



Two highlight colors are used interchangeably. Highlight the component a second time, and notice the color change. Next, select a net by selecting one trace segment, clicking right and choosing **Select Net**. Highlight these items and notice the corresponding wires in the Schematic are highlighted.

Highlighting is cumulative. To clear the last highlight, use Edit Unhighlight or click right and choose **Unhighlight.** Clear all highlights with Edit Unhighlight All.

Cross-probing works in the opposite direction as well. In ACCEL Schematic, select any combination of parts and wires. Highlight to find the corresponding items in the PCB.

Shared libraries

ACCEL EDA's libraries are set up and maintained with the various ACCEL Library Manager commands. The following is an overview of ACCEL EDA's library management scheme.

A *component* is an entity, such as a 7400, which references both a *pattern* from ACCEL PCB and a *symbol* from ACCEL Schematic. Patterns are drawn in the PCB editor. Symbols are drawn in ACCEL Schematic. Components are created in the ACCEL Library Manager by assigning pin information, and attaching a pattern and a symbol.

The ACCEL Library Manager ships with ACCEL PCB and ACCEL Schematic, so it is not necessary to own both applications to create a component. Components with only a pattern or a symbol are still functional within their respective programs. Library integration across Schematic and PCB layout is, however, a compelling reason to have both products from the same vendor.

In ACCEL Schematic, the process to create a new symbol is as follows:

1. Create a symbol from scratch by placing pins (Place Pin), symbol lines (Place Line), reference designator and type (Place Attribute), and a reference point (Place Ref Point). Other items, such as a Value attribute, are optional.

   A faster method is to create a new part based on an existing one. You must first *explode* an existing part into its original, individual entities. Try this by placing and selecting a POLCAP capacitor, then choose Edit Explode Part. You can then add, delete, move, or otherwise modify the primitives.

2. Use the Utilities Renumber command to assign pin numbers to each pin. The Select tool must be active. Toggle the **Type** to **PinNum** and select each pin in the order you want them defined. Be consistent with your numbering to make it easier later when mapping the symbol pins to pattern pads.

3. Select all items and run the Library Symbol Save As command to save your symbol to the current library. If the **Component Create** checkbox is enabled, a component (with only a symbol) is added to the library for immediate use. The symbol and component do not have to be given the same name; symbols can be assigned to multiple components. For this exercise, disable component creation.

In ACCEL PCB, the process to create a new pattern is as follows:

1. Create a pattern from scratch by placing pads (Place Pad), a silk-screen outline (Place Line), reference designator and type (Place Attribute) and various reference points (Place Point). Make sure you are placing them on the desired layer. Other items are optional.

   As with Schematic, a faster method is to create a new pattern based on an existing one. Try this by placing and selecting a POLCAP capacitor, then choose Edit Explode Component. You can then add, delete, move, or otherwise modify the primitives. Make changes consistent with the symbol you just created (e.g., match the number of pads and pins).

2. Choose the Select tool and change the current layer to a signal layer. Pad renumber will not work unless the pad is defined (non-zero) on the layer. Use Utilities Renumber to manually assign pad numbers. Toggle the Type to **PadNum** and select each pad in order. Again, number your pads consistently to make the mapping of pins and pads easier.

3. Select all items and choose Library Pattern Save As to save your pattern to a library. If **Component Create** is enabled, a component (with only a pattern) is added to the library for immediate use. The pattern and component do not have to be given the same name; patterns can be assigned to multiple components. For this exercise, disable component creation.

To integrate the symbol and pattern into a component, launch the Library Manager by choosing Utils ACCEL Lib Mgr or double-clicking on the icon found in the ACCEL EDA program group.

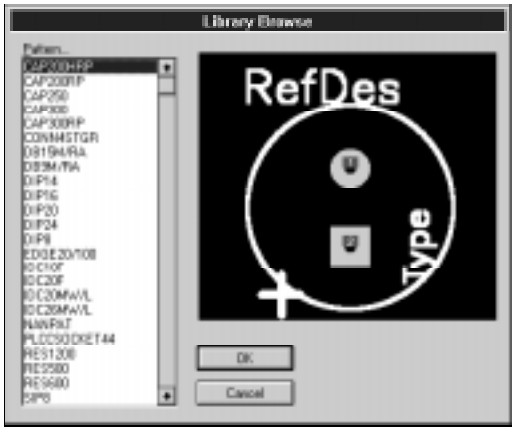
The Library Manager offers multiple views matching the data it manages for pins, patterns, symbols, and the component. To define the component we must:

- select a component pattern
- define the packaging of gates
- choose symbols for each gate and view desired
- complete the pin and pad mapping.

To create a simple, integrated component follow the steps below:

1. Choose Component New. Open the library in which your pattern and symbol were saved.
2. The Component Information dialog is presented. We'll first attach a pattern to the new component. Press **Select Pattern** and choose your newly created one from the list. It must be compatible with the symbol you will be selecting so that pins and pads can be mapped correctly. Exit the dialog.

visually locate the desired pattern

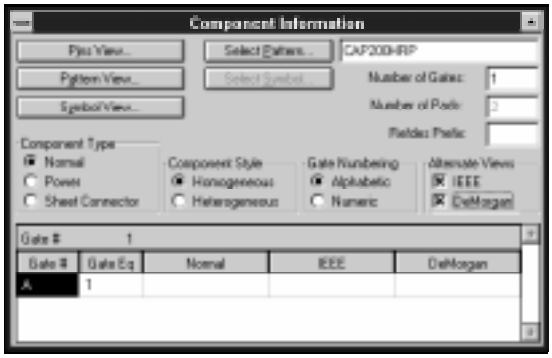


3. Our component will have one gate per package and two pads. Set the **Number of Gates** and **Number of Pads** accordingly. A **RefDes Prefix** can also be added.
4. Expand the dialog box to view the spreadsheet at the bottom. It includes one line for each gate indicated. The column labeled **Normal** is reserved for the symbol to be displayed for the gate.

alternate views are easily defined in the Library Manger

Enable the **IEEE** and **DeMorgan** options and notice extra columns are added to the spreadsheet. Alternate symbol names can be added in these columns and will be displayed instead of the Normal representation when requesting IEEE or DeMorgan notation.

easily attach symbols for each gate within a component



Our symbol will not have the IEEE or DeMorgan alternate views, so disable those checkboxes.

multiple part components are readily accommodated

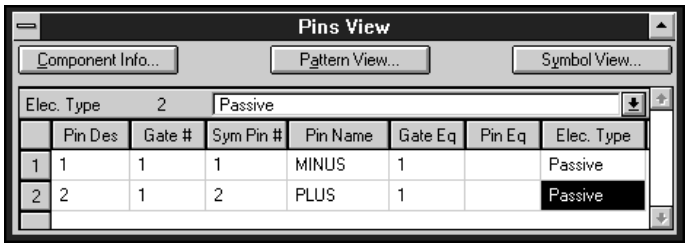
Multiple part components (those with more than one gate) can have all parts the same (**Homogeneous**) or not (**Heterogeneous**). The same symbol must be assigned for each gate of a homogeneous component, but different ones can be assigned to each gate of a heterogeneous component.

Double-click the box in the spreadsheet's column titled **Normal** (or click that box and press the **Select Symbols** push button) to attach your symbol for the gate. Browse your symbols and choose a symbol name from the list box. For multiple part and alternate view components, you would similarly assign symbol names for each view (Normal, IEEE, DeMorgan) of each gate.

5. Choose the **Pins View** button. Here, electrical data is entered and logical attributes are specified. A physical pad is mapped to a symbol pin using a pin designator.

   The spreadsheet supplies necessary pin to pad mapping information. Fill the spreadsheet to match the specs of your new component. Many editing capabilities are built into the Library Manager spreadsheets such as cut (*Ctrl+C*), paste (*Ctrl+V*), sliding selections up or down (*Ctrl+Up, Ctrl+Down Arrow*), and typing initial letters. You can try these out on our example or a more complex component in the library.

the Library Manager's pin/pad mapping spreadsheet simplifies data entry



The Pins View spreadsheet includes one row for each pad of the component. The rows are in pad order (e.g., the first row is for the first pad). This may be more than the number of pins in the attached symbol (in the case of a multiple part component). The columns are briefly described below:

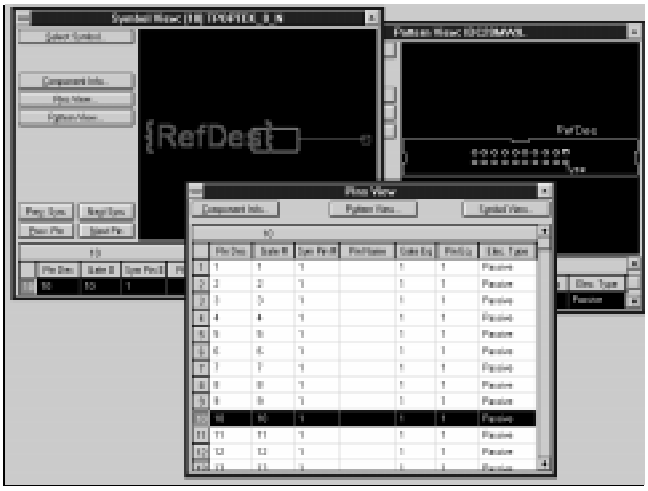
- **Pin Des.** The actual pin numbers of the component's pins. This is used in Schematic, net lists, etc.
- **Gate #.** The numbered parts within the component, represented by one or more symbols with their pins.
- **SymPin #.** This is the numerical identification of a symbol's pin. Each pin is uniquely and sequentially numbered when the symbol is built.
- **Pin Name.** The textual name given to each pin in the Schematic part. This is required for Power pins. Visibility is set on the pin during symbol placement.
- **GateEq.** This is used to indicated gate equivalence. A part represents a gate, a logical element of a component. Enter a common number at every pin of each gate that is equivalent.
- **PinEq.** Used to indicate pin equivalence. Enter a common number at each pin that can be swapped *within* a gate.
- **ElecType.** A description of the pin's electrical function. To set the value, click the arrow of the combo box (above the spreadsheet) and select a type.

7. Save the completed component using Component Save.

To view information about an existing component choose Component Open. A listing of library components is displayed. Scroll to select the one you want to examine or choose another library from which to pick.

ACCEL EDA's integrated library allows you to examine symbol, pattern, pin, and component information at the same time. Press **Pins View**, **Pattern View**, and **Symbol View** buttons. Arrange the dialogs to see the pins, pads, and much of the spreadsheet. Notice how the corresponding pattern pad, symbol pin, and spreadsheet row gets highlighted when clicked in the other views. This simplifies what can otherwise be a complex task.

view pin definitions while component, pattern, and symbol data is also visible



section review

In this section we have reviewed the features of ACCEL EDA linking Schematic and PCB, including:

- Keeping your Schematic and PCB designs in sync with engineering change orders.
- Locating items between applications by cross-probing.
- Library management, with an overview of how to create a new component.

Your evaluation has been diligent and your dedication admirable. Stay tuned for just a brief commercial message, and then you are free to celebrate your new status as an ACCEL EDA expert.

Taking the Next Step

This concludes the formal part of our presentation. Again, we would like to thank you for taking the time to evaluate the ACCEL EDA products. You have made a wise investment of your time because the purchase of CAE/CAD software is a very difficult and important decision. We hope this tour of ACCEL EDA has helped you form a better understanding of the schematic design and PCB layout processes in general, and of our products in particular.

how to justify your ACCEL EDA investment

The money spent on electronic design software is but a small percentage of a company's investment in design automation. Hardware, library and design creation, and personnel training all add up. An investment in ACCEL EDA provides outstanding return for these reasons:

1. **Ease of Use.** Tremendous thought and designer input went into ACCEL EDA. The result is a product that is easier to learn the first time and quick to pick back up later.
2. **Productivity.** You and your department will get more work done in less time using ACCEL EDA than any other PCB design tool. We guarantee it.
3. **Quality and Cost.** With its many automated features, and comprehensive verification and output capabilities, ACCEL EDA helps you produce quality boards at lower manufacturing costs.
4. **Performance.** ACCEL EDA's advanced features allow you to design the most sophisticated boards being built today and in the future. You can be confident that ACCEL EDA will deliver, as you "push the limits" on your electronic designs.

call to arrange a personal demonstration

The next step is up to you. Join us at one of our regional seminars to see how ACCEL EDA can make you more productive or call us to arrange a demonstration of ACCEL EDA at your own site. Be sure to ask how our application programming interface (API) can help meet your custom development needs. Complete software packages may be available for evaluation.

ACCEL also offers top-of-the-line CAM and auto placement tools, and floating network licenses. Contact ACCEL Sales or your local ACCEL reseller for more information or to take a closer look at ACCEL EDA.

Your investment in ACCEL EDA software also includes:

- **Regular software updates** and **responsive technical support** provided via phone or FAX by experienced application personnel at ACCEL or your local ACCEL reseller. It's free for the first 90 days, and available for reasonable maintenance fees thereafter.
- **Clear, concise documentation** furnished both on-line and in illustrated manuals.
- **ACCEL-BBS**, our 24-hour on-line bulletin board service.
- **Our newsletter**, *Design Today*.

You'll find user-friendly customer service at ACCEL Technologies and your local ACCEL reseller. We invite you to give us a call with any additional questions regarding ACCEL EDA, P-CAD Master Designer for DOS or UNIX, Tango for DOS, or any of the other products offered by ACCEL. We understand that every engineer's design requirements are unique, and we're happy to discuss your particular needs at length.

Order today and join the thousands of users who enjoy the benefits of powerful, yet easy-to-use electronic design tools.

APPENDIX A

Using P-CAD Schematic Files

This chapter discusses using P-CAD binary files, or databases, and PDIF files in ACCEL Schematic. Here you learn:

- how to load P-CAD binary files.
- how to load and save and PDIF files.
- the considerations for P-CAD binary files and PDIF files.
- helpful tips for fine-tuning your design after loading it into Schematic.

The terms “P-CAD” and “Master Designer” are used interchangably.

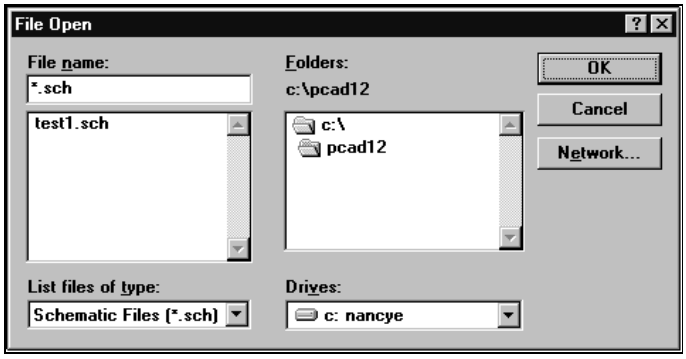
ACCEL Schematic and PCB let you load P-CAD binary files (.PCB and .SCH) directly. You can load any P-CAD binary files created in Master Designer versions 8.0 and 8.5. To load P-CAD databases created in Master Designer versions 7.0 or older, or to load P-CAD databases created in Associate Designer, use File PDIF In.

Loading P-CAD Binary Files

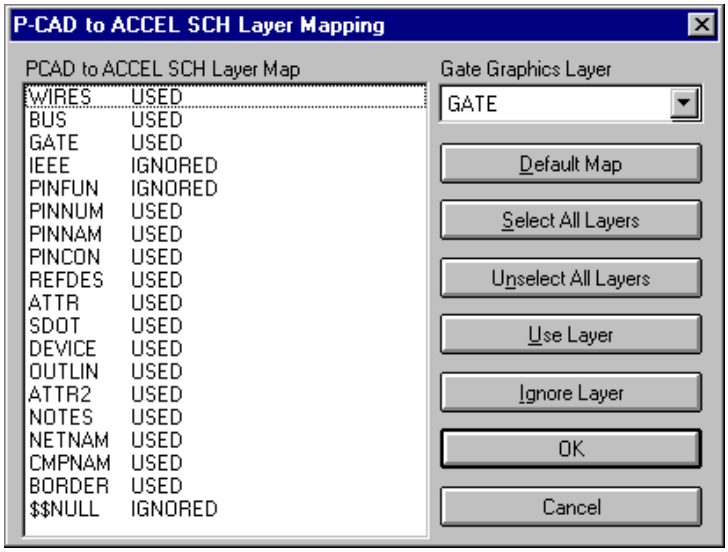
To load a P-CAD binary file, follow these steps:

1. Choose File Open. The Open dialog appears.
2. At the **Files of type** field, select the type of file to load. You can select either Schematic files (as shown below) to load a single sheet schematic, or select P-CAD CFG Files if you want to load a multi-sheet design. We recommend that you select P-CAD CFG

Files if your schematic design is a multi-sheet design to preserve the netlist information.



3. In the **File Name** box, enter the name of the desired .SCH file. You can also select the desired .sch file from the file list.
4. Click **OK**. The P-CAD Cross-Reference dialog appears. The P-CAD Cross-Reference file contains power and ground pin assignments. It also attempts to group heterogenous components.
5. Click **Cross-Reference** to specify a Cross-Reference file, or click **OK** if there is none. The P-CAD to ACCEL SCH Layer Mapping dialog appears, as shown below:



6. Select the desired layers and map them accordingly. Then click **OK**.

While loading, Schematic displays several messages on screen, indicating the system's progress. After Schematic loads the file, a message box appears indicating if there were any errors or warnings. If there are none, you can click **OK**.

If there are errors or warnings while loading the file, Schematic creates a log file *design-name*.err, where *design-name* is the name of the P-CAD binary file you loaded. In this case, a dialog appears, prompting you to view the log file. Schematic displays the log file using the viewer selected with the Options Configure command. The default viewer is Notepad.

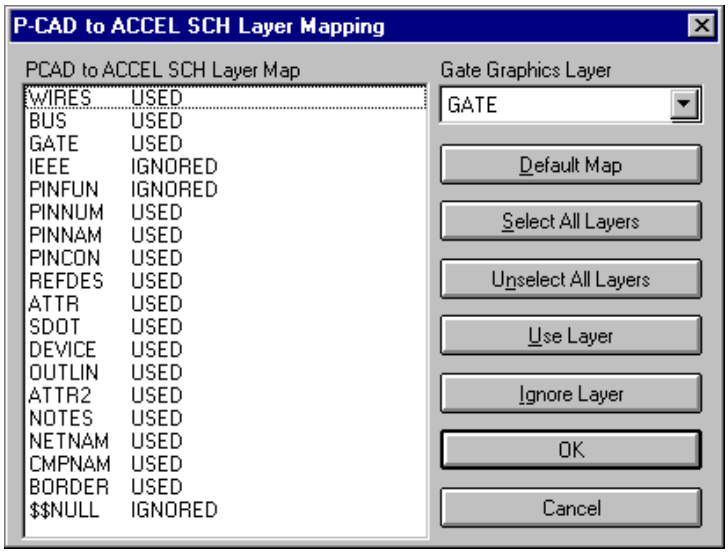
It is a good idea to examine the log and correct any errors that show up. For details about any problems that could occur, see Appendix C, P-CAD System Messages.

Mapping Layers From P-CAD Binary Files to ACCEL Schematic

ACCEL Schematic now lets you map layers when you import a P-CAD Schematic design file, just as you already

do in ACCEL PCB. Though ACCEL Schematic already translates most data directly from a P-CAD schematic design, graphic data on the IEEE, PINFUN, and BUS layers do not translate directly. To correct this, ACCEL Schematic lets you map layers and control which layers are visible. This means you can map graphics on the GATE and/or IEEE layers to the normal graphic representation of the symbol.

Just as in ACCEL PCB, you map layers when opening a P-CAD schematic design in ACCEL Schematic by using the layer mapping dialog:



This dialog lets you select which layers to map, map the desired layers, and specify a Cross-Reference file.

- **Gate Graphics Layer:** Lists the target layers available for normal gate representation.
- **Default Map:** Assigns all P-CAD layers to a default layer mapping structure.
- **Select All Layers:** Selects all layers set to MAPPED or IGNORED.
- **Unselect All Layers:** Deselects all layers set to MAPPED or IGNORED.

- **Set Layer Mapped:** Instructs ACCEL Library Manager to map this layer and translate its data.
- **Set Layer Ignore:** Instructs ACCEL Library Manager to ignore this layer and any data on it.
- **OK:** Confirms your selections.
- **Cancel:** Cancels the layer mapping and aborts loading the schematic design.

Loading Multi-Sheet Designs

If you're loading a design.cfg file, Schematic translates all the binary files into a single multi-sheet design. In the design, each sheet has its own window. To toggle between sheet windows, select the desired sheet from the Sheet Display Combo Box on the Status Line.

Saving a P-CAD Design as an ACCEL Binary File

When you save an updated P-CAD binary file, Schematic displays a message box asking you if you want to overwrite the original P-CAD binary file.

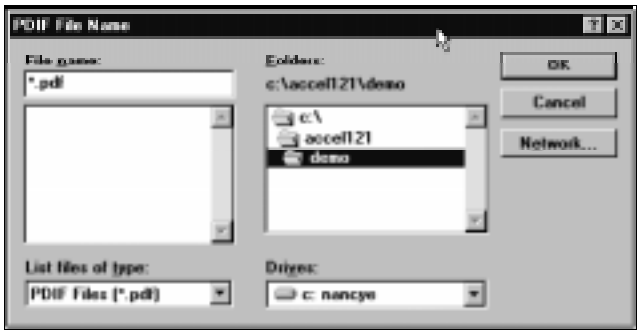
If you select **Yes**, Schematic overwrites the existing P-CAD binary file in ACCEL Schematic format. Once you overwrite this file, you can't use it in Master Designer again. If you select **No**, Schematic displays the Save As dialog and prompts you for a new filename. If you select **Cancel**, Schematic aborts the save process.

Importing PDIF Files

Importing PDIF files to Schematic is similar to loading P-CAD binary files, except that you can either load a PDIF (.pdf) file, or load the design.cfg file for your schematic.

To import a PDIF or design.cfg file, follow these steps:

1. Select File PDIF In. The PDIF File Name dialog appears:



2. Select the type of file to load. You can either select PDIF Files if you want to load a .PDF file, or select .CFG Files if you want to load a design.cfg file for a particular schematic. We recommend that you load the design.cfg file if your schematic design is a multi-sheet design.
3. Type, or select from the list, the name of the file you want to open in the **File Name** box.
4. If the file you want is not in the current directory, then either type the directory name in front of the document name, or select the directory from the **Directories** box.
5. Click **OK**. Schematic loads the selected PDIF file.

Loading Multi-Sheet Designs

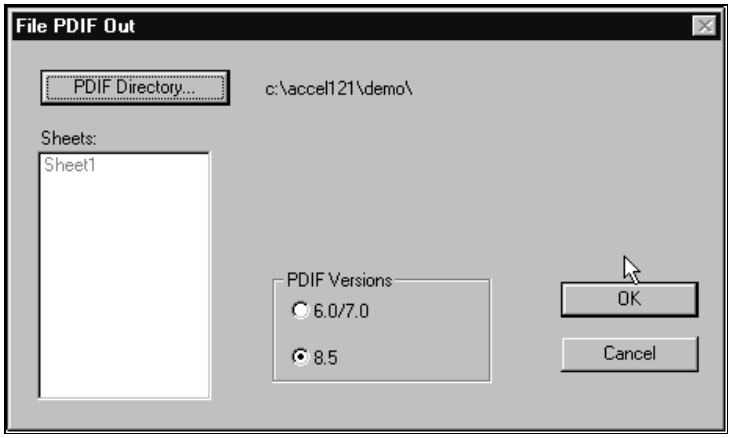
If you're loading a design.cfg file, Schematic translates all the PDIF files into a single multi-sheet design. The loaded design is unnamed, but contains all the sheets in your design. Each sheet has its own window. To toggle between sheet windows, select the desired sheet from the Sheet Display Combo Box on the Status Line.

Generating PDIF Files

Schematic lets you save your design to PDIF format so you can use it with the latest version of Master Designer.

To generate a PDIF file, follow these steps:

1. Select File PDIF Out. The PDIF File Out dialog appears, as shown below:



2. Click the **PDIF Directory** button. The PDIF Directory dialog appears.
3. Select a directory in which to save the file. To save the file in a different directory, then either type the directory name in front of the document name, or select the directory from the **Directories** box.
4. Click **OK**. Schematic returns you to the File PDIF Out dialog.
5. Select the **PDIF Version** you want to create.
6. Click **OK**. Schematic generates the PDIF file and saves it to the selected directory.

ACCEL Schematic supports multi-sheet designs as a single database, while PDIF supports only one sheet per design file. Therefore, when exporting multi-sheet designs, ACCEL Schematic writes a single PDIF file for each sheet and writes a Master Designer-compatible design.cfg file, which binds the sheets into a single design. All these files are placed in the directory specified in the PDIF Directory dialog.

For multi-sheet designs, P-DIF Out uses the sheet name as the filename. If the sheet name exceeds eight characters, it truncates the sheet name.

While generating the PDIF file, ACCEL Schematic displays several messages on screen, indicating the system's progress. When ACCEL Schematic finishes generating the file, a message box appears indicating if there were any errors or warnings. If there are none, you can click **OK**.

If there are errors or warnings, ACCEL Schematic creates a log file *design-name*.err, where *design-name* is the name of the PDIF file you created. In this case, a dialog appears, prompting you to view the log file. ACCEL Schematic displays the log file using the viewer selected with the Options Configure command. The default viewer is Notepad.

Design Considerations

When using either a P-CAD binary file or a PDIF file in Schematic, you need to be aware of certain design differences between P-CAD and ACCEL Schematic designs. This section addresses the design differences you may encounter.

P-CAD Binary Files and PDIF Files

The considerations below apply to both P-CAD binary files and PDIF files:

- **Internal components (PDIF only):** All component information must reside in the PDIF file. External component references are not supported.
- **Power pin net assignments:** These can be specified either through a cross reference file or the component's PWGD attribute. If you choose the cross reference file, the file must reside in the same directory as the P-CAD binary file or PDIF file and have the same base name, but with a .FIL extension. For example, if the design you wish to load is called C:\PCAD\TANGO\SHEET1.PDF, then the cross reference file must be C:\PCAD\TANGO\SHEET1.FIL. On the other hand, if you are using the PWGD attribute to define the power pins, a cross reference file is not required. The PWGD attribute will be used

for assignment before searching the cross reference file.

If you want to load a multi-sheet design, you can specify the cross reference file name to be used when you load the design.cfg by entering the filename in the **Cross-Reference** field in the Design Maintenance dialog of the Design Manager of P-CAD Master Designer.

- **Component attribute visibility:** Since Master Designer does not have the ability to hide and show individual attributes of a symbol, all “normal” (i.e. not power nor sheet connector) Schematic symbols exported will have visible Refdes and Type attributes. Power and sheet connector parts will always have hidden Refdes and Type attributes when exported. This also applies to pin designators.
- **Single versus multi-sheet designs:** Loading a single P-CAD binary file or PDIF file creates a single sheet design. Loading the design.cfg file for a design will create a separate sheet (in a single design) for each P-CAD binary file or PDIF file specified in design.cfg. Master Designer creates a design.cfg file for each design you setup.
- **Auto port detection:** ACCEL Schematic attempts to translate net names into ports, provided the net name’s justification point is aligned (vertically or horizontally) with some wire in the net. The distance between the wire and the net name should be no more that 200 mils (you can override this in the sch.ini file with the MaxDistanceToPort keyword). If a net name could not be matched with a wire segment, the port may be added elsewhere in the net and the log file will tell you where.
- **Gates per Component:** ACCEL Schematic components can have no more than 255 gates per component.
- **Heterogeneous Components:** In Master Designer, heterogeneous components are grouped when you import them into Schematic and divided when you export them from Schematic. Only ACCEL Schematic and ACCEL Library Manager include special handling of heterogeneous components. For heterogeneous parts to be correctly supported in

ACCEL Schematic and ACCEL Library Manager you *must* have a cross reference file with entries for all the heterogeneous components in the design (single or multi-sheet). The cross reference file entries specify the following: number of gates in each homogeneous subsection, a common device type, a common part name, a common set of power pin/net pairs, and a unique symbol name. For example, the cross reference entries for the 74LS31 six part delay line component would look like this:

2 **74LS31 74LS31.PRT (16=+5V, 8=GND)** 74LS31AF.SYM

2 **74LS31 74LS31.PRT (16=+5V, 8=GND)** 74LS31BE.SYM

2 **74LS31 74LS31.PRT (16=+5V, 8=GND)** 74LS31CD.SYM

The columns that must match for the group to be considered a heterogeneous component are shown in bold. Because each component in the sheet has a different name, the device name (in this example: 74LS31) will be used in the Schematic design as the component type name. Components in a P-CAD sheet that reference gate numbers that are out of range given the number of parts defined in the cross reference file (in this example, 6) will produce warnings when loaded into Schematic and the component will not be loaded. The design still must have at least one symbol from each heterogeneous part group (parts A, B, C or F, E, D in the above example) placed in the design in order for the component to be complete in Schematic, and not tossed out because Schematic needs the symbol data for each part group. Library Manager uses the same logic and the component will not translate if incorrect. Schematic will not create components with missing symbols or symbol names.

After reading the cross reference file, and only if heterogeneous components are detected as described above, a dialog displays the names of the components that are thought to be heterogeneous. You can either select them or remove them from the list of candidates. At this point, Schematic loads the design file.

An example of cross reference file entries that would mistakenly be grouped as heterogeneous are these:

1 CAP CK06.PRT CAPH.SYM

1 CAP CK06.PRT CAPV.SYM

You would then select CAP and click **Remove**.

When you export an ACCEL Schematic design with the File PDIF Out command, it will *not* write a cross reference file per se, but will write a pseudo-cross reference file entry into the log file following some appropriate warning message about encountering the heterogeneous component. A sample log file entry might look something like this:

Warning: Component 74LS31 is heterogeneous and will be written as 3 separate component definitions. Cross reference file data follows:

2 74LS31 74LS31.PRT (16=+5V, 8=GND) 74LS31.SYM

2 74LS31 74LS31.PRT (16=+5V, 8=GND) 74LS31A.SYM

2 74LS31 74LS31.PRT (16=+5V, 8=GND) 74LS31B.SYM

If you need to load the design back into Schematic or package the schematic in Master Designer, you can paste the information in the log file into your cross reference file. The homogeneous subcomponents have a suffix letter added to the filename to indicate second or subsequent entries. The part name will be "unknown" if the component type name has more than eight characters. The symbol name will be "unknown" if not all symbols of a heterogeneous component are placed in the design.

PDIF Files

The considerations below apply only to PDIF files:

- **Blank pin names**
  Master Designer does not allow the pin name to be blank or left out. If a blank pin name is detected during an export to PDIF, the pin name will be set to the pin designator of the corresponding pin in the first part (part "A") of the component.

Import and Export Considerations

This section discusses the known considerations for importing and exporting with Schematic.

Importing P-CAD Binary Files and PDIF Files

- Since Master Designer uses a non-proportionally spaced font, text appears slightly different when viewed in Schematic.
- Schematic does not allow certain characters in names, such as '-', '[', etc., are converted to '_'. This affects reference designators, net names and component names.
- Tildes (~) in input files are not treated specially.
- Designs greater than 60 inches by 60 inches are not loaded into Schematic.
- Text can be a maximum of 5000 mils high in P-CAD. In Schematic, the limit is 1000 mils, or 1 inch.
- Line widths become either thin or thick.
- Wire labels are converted to ports if and only if the justification point of the text lines up perfectly (horizontal or vertical) with the wire. If it does not line up, the wire label is lost and a port may be created at some other point in the net.
- Dotted and dashed lines translate to thin lines, which are 10 mils thick.
- The SHEET attribute in multi-sheet designs is lost; ACCEL Schematic does not need this attribute.
- Net names that are 20 characters or more are not loaded.
- Non-homogeneous symbol names will come from the **device type** field in the PCAD cross reference file.
- Schematic supports rotations in 90° increments. Therefore, when you import a design with components rotated at 45° increments, Schematic rotates them clockwise to the next 90° rotation.

Exporting PDIF Files

- Component names are truncated to 8 letters. Unique names are maintained by adding letters or numbers to the end of the name. Also, some Master Designer components are represented as DOS files.
- Text stroke thickness is lost.
- Substring barring is not supported. A~B~C (A B-bar C) outputs as “A~B~C” verbatim.
- Text height cannot be smaller than 2 mils.
- Some pin electrical and display characteristics are lost.
- When running PDIF Out, some PRT attributes may not match with existing parts. This is due to the fact that Schematic allows PRT attributes greater than eight characters, and P-CAD only allows up to eight characters.

  To fix this, run the File PDIF Out command, then go into P-CAD. In P-CAD, select PDIF File header. At this dialog, click Create Components and run PDIF File header. Then bring the design into the Schematic editor and modify the PRT attribute for each part as needed.

PDIF File Cleanup Tips

This section lists some helpful tips for cleaning up your PDIF files and P-CAD binary file after importing it into Schematic.

Ports and Wire Labels

Schematic converts wire labels to ports if and only if the justification point of the text lines up perfectly (horizontal or vertical) with the wire. If it does not line up, the wire label is lost and a port may be created at some other point in the net. If this occurs, you may need to redisplay the wire labels and move some ports.

It is unlikely that you'd have to worry about cleaning up ports and wire labels. However, we recommend that you at least verify that your nets translate correctly.

You might also want to change the text styles using the Options Text Style command to improve your design's aesthetics. Selecting this command displays the Options Text Style dialog. From here, you can modify existing styles, add or delete text styles.

APPENDIX B

Using P-CAD PCB Files

This chapter discusses using P-CAD Binary files and PDIF files in ACCEL PCB. Here you learn:

- how to load P-CAD binary files.
- how to load and save and PDIF files.
- the considerations for P-CAD binary files and PDIF files.
- helpful tips for fine-tuning your design after loading it into PCB.

Note that in this chapter, the terms “P-CAD” and “Master Designer” are used interchangeably.

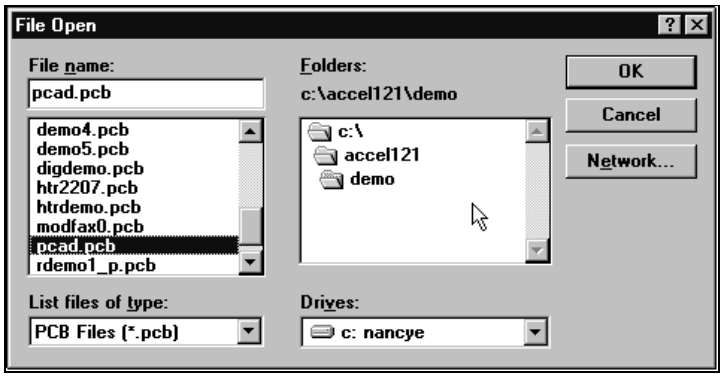
ACCEL PCB lets you load P-CAD binary files (.PCB) created using Master Designer versions 8.0 and 8.5. To load P-CAD databases created in Master Designer versions 7.0 or older, or to load P-CAD databases created in Associate Designer, use the File PDIF In command.

Loading P-CAD Binary Files

To load a P-CAD binary file, follow these steps:

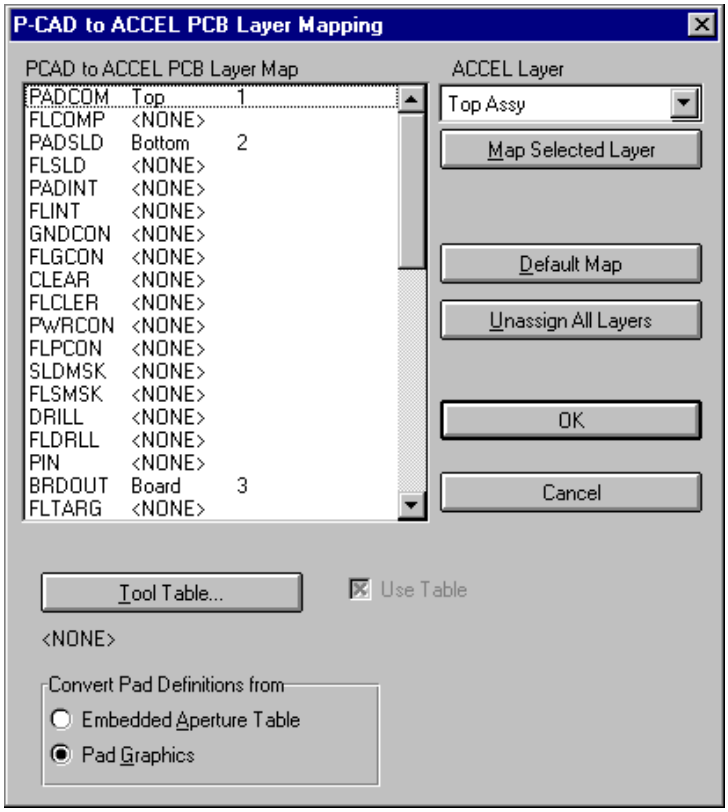
1. Choose File Open. The Open dialog box appears.

2. At the **List Files of Type** field, select .PCB Files as the desired file type.



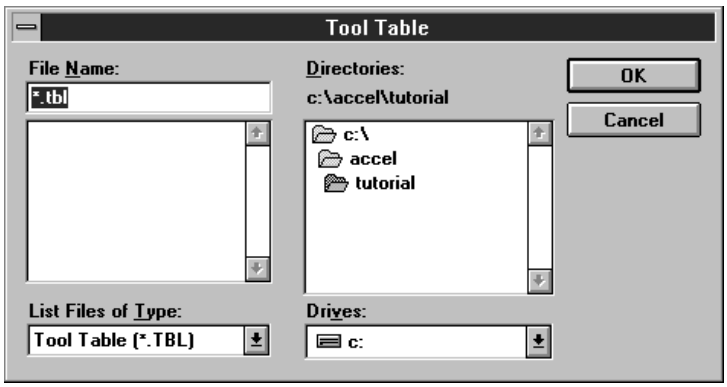
3. In the **File Name** box, enter the name of the desired .PCB file or select it from the file list.

4. Click **OK**. PCB automatically detects that you're loading a P-CAD binary file and displays the P-CAD to ACCEL PCB Layer Mapping dialog, shown below:



5. At the P-CAD to ACCEL PCB Layer Mapping dialog box, select the appropriate layer mapping assignments. For details about mapping layers, see the section “Mapping Layers from P-CAD Binary and PDIF Files to PCB.”

6. Specify a tool table by clicking the **Tool Table** button. The Tool Table dialog box appears, as shown below:



At this dialog box, select the desired tool table (.tbl) file and click **OK**. PCB returns you to the P-CAD to ACCEL PCB Layer Mapping dialog box.

PCB requires the tool table file because it contains hole size information that the P-CAD file does not have. You specify the tool table file to use at the tool table dialog box. If you do not specify a tool table file, PCB assigns two default hole sizes for you. The sizes are 20 mils for pads and 10 mils for vias. To change these sizes, open the pcb.ini file, go to the [PDIF] section, and edit the entries DefaultPadHoleSize and DefaultViaHoleSize.

If you load the design without specifying a tool table file, you must edit the hole size of all pad and via styles that have a hole size other than 20 mils and 10 mils. You can do this using the Options Pad Style and Options Via Style commands.

If a tool table file is specified but you do not want to load it, uncheck the **Use Table** checkbox. PCB uses the default hole sizes instead.

7. Specify how you want PCB to convert polygons by selecting **Copper Pour** or **Polygon**.

   A polygon is a large area of copper that can have net name information if there is a wire connected to it. However, you can't do things with a polygon that you can do with a copper pour, such as back off from pads, set thermal connections, and do pours.

You can convert polygons to copper pours or use them as polygons.

Select **Copper Pour** because these polygons can have cutouts (voids) and backoff from pads. Also, if you have padstacks with void definitions, you should select **Copper Pour**.

The only time you might want to select **Polygon** is if the P-CAD polygons have no cutouts (voids) in them. A P-CAD polygon with a void that is imported as a PCB polygon has the same net information. However, voids are ignored, which may cause a shorted board.

8. Specify how you want to convert the pad definitions. You can either convert them from the **Embedded Aperture Table** or from the design's **Pad Graphics**.

   The polygon aperture shapes and the Aperture macros are not supported.

   Select **Embedded Aperture Table** to take full advantage of the aperture shapes and sizes. You should select **Pad Graphics** only if you don't have an aperture table embedded in your design.

9. Click **OK**. PCB loads the selected .PCB file.

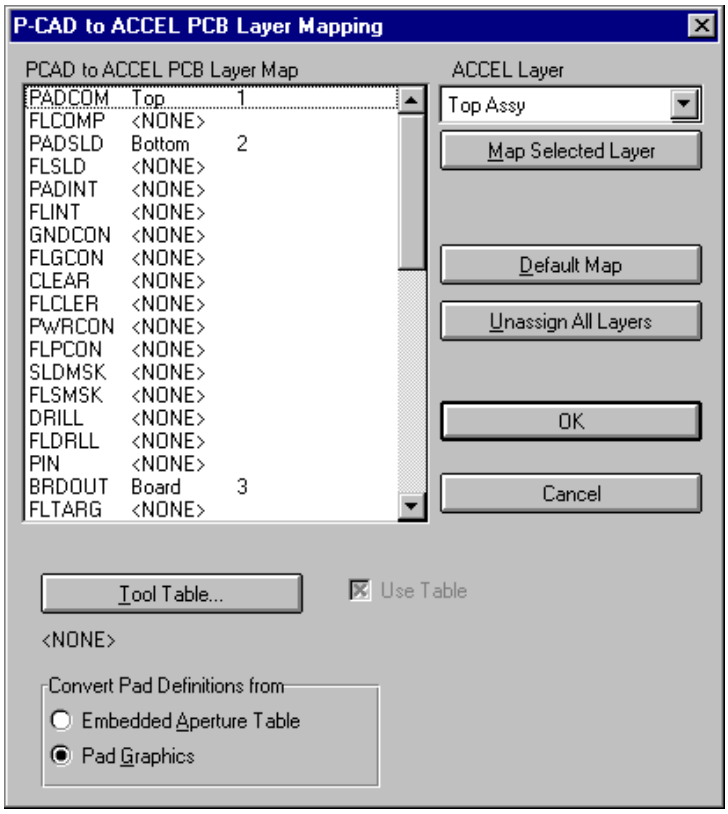
While loading, PCB displays several messages, indicating the system's progress. After PCB loads the file, a message box appears indicating if there were any errors or warnings. If there are none, you can click OK.

If there are errors or warnings while loading the file, PCB creates a log file *design-name*.log, where *design-name* is the name of the P-CAD binary file you loaded. In this case, a dialog box appears, prompting you to view the log file. PCB displays the log file using the viewer selected with the Options Configure command. The default viewer is Notepad.

It is a good idea to examine the log and correct any errors that show up. For details about any problems that could occur, see Appendix B, P-CAD System Messages.

Mapping Layers from P-CAD Binary and PDIF Files to PCB

The P-CAD to ACCEL PCB Layer Mapping dialog box lets you decide which Master Designer layers map to which PCB layers and which layers will not be loaded.



P-CAD to ACCEL PCB Layer Map: Displays the P-CAD layer mapping assignments. A <NONE> next to the P-CAD layer name indicates that PCB will ignore data on that layer. A typical layer assignment looks like this:

PADCOM Top SA 1

where:

- PADCOM is the P-CAD layer.

- Top is the PCB layer assigned to the P-CAD layer PADCOM.
- S indicates the layer's status (S=signal, N=nonsignal, P=plane).
- A indicates the autorouter bias (A=auto, H=horizontal, V=vertical).
- 1 indicates the layer number.

ACCEL Layer: Lists the PCB layers available for mapping.

Map Selected Layer: Assigns the selected P-CAD layer to the selected PCB layer.

Create New Layer: Displays the Options Layers dialog box so you can create a new layer or modify an existing one.

Default Map: Maps the PCB design signal to signal, plane to plane, non-signal to non-signal. This option saves you having to create layers by hand. The default layer map set varies, depending on whether you select embedded aperture tables or pad graphics to convert your pad definitions.

Auto Map All Layers: Automatically maps all unassigned P-CAD layers to PCB layers of the same name. If a layer does not have <NONE> next to it, PCB leaves the current assignment.

Unassign All Layers: Assigns <NONE> to all the P-CAD layers in the list.

Tool Table: Lets you select which tool table to use. Tool tables specify the hole size to use for each pad type in the converted design.

Use Table: Indicates whether or not to use the Tool Table. PCB needs the tool table to apply the correct hole sizes. If you don't specify a tool table, PCB uses a default hole size for the pad types.

Polygons: Indicates to convert polygons to polygons. You should select this option if you never ran the Environment→Merge Voids by Poly command in Master Designer 8.5.

Copper Pours: Instructs PCB to convert polygons to copper pours. Selecting this option automatically creates thermal ties to pads and vias in the same net. You should select this option if you want to preserve the voids in your design.

Embedded Aperture Table: Instructs PCB to convert pad definitions from the design's embedded aperture table.

Pad Graphics: Instructs PCB to convert pad definitions from the design's pad graphics.

Layer mapping goes from specific to general. That is, many P-CAD layers are typically mapped to a single PCB layer. For example, component-side information in P-CAD is frequently contained on the COMP, PADCOM, and PINTOP layers, whereas PCB stores all this information on the Top layer. PCB does not distinguish among Top layer tracks, Top layer padstacks and Top layer SMD pads; they are all on the Top layer.

To map a layer, follow these steps:

1. At the P-CAD to ACCEL Layer Mapping dialog box, select one or more source layers from the **P-CAD to ACCEL PCB Layer Map** list.

2. Select the desired PCB layer from the **ACCEL Layer** list.

3. Click the **Map Selected Layer** button. Notice the **P-CAD to ACCEL PCB Layer Map** list now displays, from left to right:

   - the P-CAD layer name.
   - the PCB layer name, or <NONE> if not assigned.
   - the layer type.
   - the autorouting bias.
   - the layer number.

   You can also click the **Default Map** button to assign all the predefined P-CAD layers to the appropriate PCB layers and all others to <NONE>. Or you can click **Auto Map All Layers** to automatically map all unassigned

layers to <NONE>. Note that clicking **Auto Map All Layers** can create several layers.

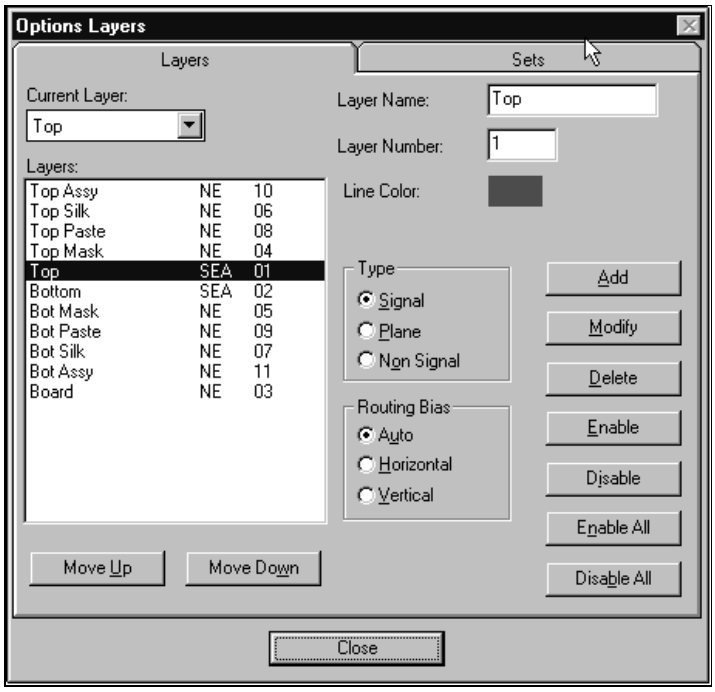
4. Repeat steps 1 through 3 until all layers are mapped.

5. Click **OK**.

When mapping layers, you should group the layers into three categories: signal, nonsignal and plane. For **signal** layers, the layer map often looks like this:

Signal Layer Mapping	
P-CAD Layer	**PCB Layer**
COMP	Top
PADCOM	Top
PINTOP	Top
SOLDER	Bottom
PADSLD	Bottom
PINBOT	Bottom
INT1	Mid-1
INT2	Mid-2

You may need to create layers that are not predefined, such as Mid-1 and Mid-2. To do this, click the **Create New Layer** button. The Options Layers dialog appears, as shown below.



For **non signal** silk layers, the layer mapping is to Top Silk or Bottom Silk. The board outline should map to the Board layer:

Non Signal Layer Mapping	
P-CAD Layer	**PCB Layer**
BRDOUT	Board
SLKSCR	Top Silk
DEVICE	Top Assy
ATTR	Top Silk
ATTR2	<NONE>
REFDES	Top Silk
SLKTOP	Top Silk
SLKBOT	Bottom Silk
DVCTOP	Top Silk
DVCBOT	Bottom Silk
REFDTP	Top Silk
REFDBT	Bottom Silk

The other **Non Signal Layer**s are mask, paste, assembly and documentation layers. We recommend that you do not map mask and paste layers. This is because PCB has built-in manufacturing intelligence and automates creating mask and paste data. *If you choose to map mask and paste layers*, use the following map:

Mask and Paste Layer Mapping	
P-CAD Layer	**PCB Layer**
SLDMSK	Bot Mask
MSKGTP	Top Mask
MSKGBT	Bot Mask
PSTGPT	Top Paste
PSTGBT	Bot Paste

Assembly and documentation layers are typically mapped to layers of the same name.

Plane layer mapping also requires close scrutiny. You must know ahead of time which layers are plane layers and what net each plane is assigned to.

To map a plane layer, click the **Create New Layer** button at the P-CAD to ACCEL PCB Layer Mapping dialog box. The Options Layers dialog box appears. Now create the plane layers that you require, and enter a net name for each plane. The layer map might look something like this:

Plane Layer Mapping		
P-CAD Layer	**PCB Layer**	**Net Name**
GNDCON	GND	GND
PWRCON	VCC	VCC

If, when mapping layers, you do not use an embedded aperture table, you can ignore all other layers, such as flash, $$, and PIN. To specify that a layer is not mapped, map it to <NONE>. If you are using an embedded aperture table, you may not need the graphic data in the flash because the aperture table contains this data.

Saving a P-CAD Design as an ACCEL Binary File

When you save an updated P-CAD binary file, PCB displays a message box asking you if you want to overwrite the original P-CAD binary file.

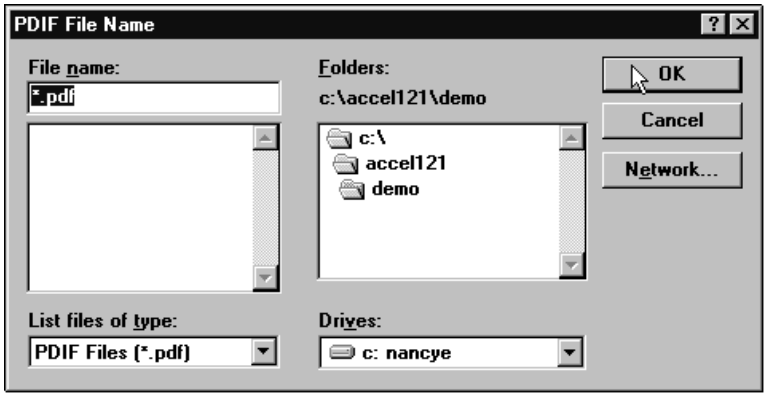
If you select **Yes**, PCB overwrites the existing P-CAD binary file in ACCEL PCB format. Once you overwrite this file, you can't use it in Master Designer again. If you select **No**, PCB displays the Save As dialog box and prompts you for a new filename. If you select **Cancel**, PCB aborts the save process.

Importing PDIF Files

Importing PDIF files to PCB is similar to loading P-CAD binary files.

To import a PDIF file, follow these steps:

1. Select File PDIF In. The PDIF File Name dialog box appears:



2. In the **File Name** box, enter the name of the desired .pdf file.

3. If the file you want is not in the current directory, then either type the directory name in front of the document name, or select the directory from the **Directories** box.

4. Click **OK**. PCB displays the P-CAD to ACCEL PCB Layer Mapping dialog box.

5. At the P-CAD to ACCEL PCB Layer Mapping dialog box, select the appropriate layer mapping assignments. For details about mapping layers, see the section "Mapping Layers from P-CAD to PCB" earlier in this chapter.

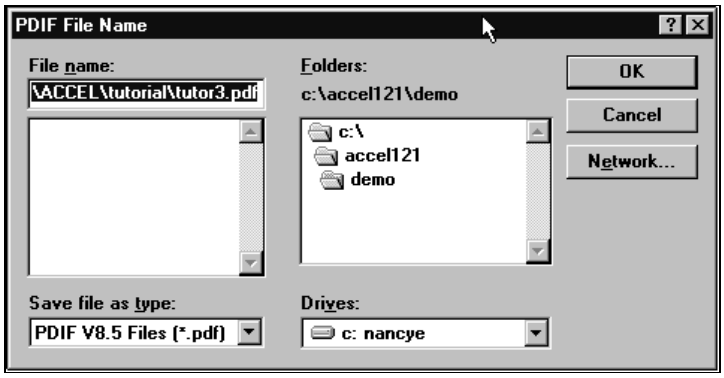
6. Click **OK**. PCB loads the selected PDIF file.

Generating PDIF Files

PCB lets you save your design to PDIF format so you can use it with the latest version of Master Designer.

To generate a PDIF file, follow these steps:

1. Choose File PDIF Out. The PDIF File Name dialog box appears, as shown below:



2. Select a directory in which to save the file. To save the file in a different directory, then either type the directory name in front of the document name, or select the directory from the **Directories** box.

3. Click **OK**. PCB generates the PDIF file and saves it to the selected directory.

While generating the PDIF file, PCB displays several messages on screen, indicating the system's progress. When PCB finishes generating the file, a message box appears indicating if there were any errors or warnings. If there are none, you can click **OK**.

If there are errors or warnings, PCB creates a log file *design-name*.err, where *design-name* is the name of the PDIF file you converted. In this case, a dialog box appears, prompting you to view the log file. PCB displays the log file using the viewer selected with the Options Configure command. The default viewer is Notepad.

Design Considerations

When using either a P-CAD binary file or a PDIF file in PCB, you need to be aware of certain design differences between P-CAD and ACCEL PCB designs. Not all data maps to the ACCEL PCB or Schematic data. This section addresses the design differences you may encounter.

P-CAD Binary Files and PDIF Files

The considerations below apply to both P-CAD binary files and PDIF files:

- **Power pin net assignments:** These can be specified either through a cross reference file or the component's PWGD attribute. If you choose the cross reference file, the file must reside in the same directory as the PDIF file and have the same base name, but with a .fil extension.

  For example, if the PDIF design you wish to load is called C:\PCAD\LAYOUT1.PDF, then the cross reference file must be C:\PCAD\LAYOUT1.FIL. On the other hand, if you are using the PWGD attribute to define the power pins, a cross reference file is not required. The PWGD attribute will be used for assignment before searching the cross reference file.

- **Attached padstacks:** The PDIF file you load into PCB must have an attached padstack section. You can attach the padstack in Master Designer. "No-connect" padstacks are honored, but PCB does not change the style once a connection is made to that the pad. "No-connect" padstacks are padstacks that are used for pads that are not part of any net.

- **SMD pads:** Many surface mount device components in Master Designer are created by placing filled rectangles or rectangular polygons in the component instead of using a padstack as is done for through hole components.

  If PCB detects that the filled rectangle or rectangular polygon is actually an SMD pad, the program creates a pad style for the SMD pad and removes the rectangle from the component. The PCB SMD pads may have been shifted slightly during the translation if the P-CAD pin was not at the center of the rectangle. The end result, however, is the same as the original P-CAD component.

- **Copper Pours:** When Master Designer polygons are loaded and converted to PCB copper pours, the pours are created with the correct net, but are unpoured. You can pour them by selecting the copper pours and running the Edit Properties command. To be compatible with polygons in Master Designer, the copper pours have a 0-mil backoff, solid fill and no thermal spokes. This can lead to weak connections if there are pads under the pour that have no net assignment, such as mounting holes.

  It is recommended that free pads under a copper pour that were intended to connect to the pour be made part of the pour's net. You can do this in Master Designer with the Enter→Ratsnest command before generating the PDIF file or in PCB by placing a connection from the pad to some other node in the net.

- **Keepouts:** Keepouts are created from arcs, circles, filled rectangles, lines, rectangles, and polygons that reside on layers whose name begins with the letters "BAR". If the P-CAD layer name is BARALL and the layer is unmapped (mapped to <NONE>), the keepout will become an *all layer keepout*. Otherwise, the

object on the "BAR" layer becomes a *single layer keepout* on whatever layer it is mapped to.

For example, a polygonal void on the BARTOP layer that is mapped to Top becomes a top layer polygonal keepout. Keepouts in components work the same way.

PDIF Files

The considerations below apply only to PDIF files:

- **Internal components:** All component information must reside in the PDIF file. External component references are not supported.
- **Net data:** In Master Designer, the only objects that are considered part of the net and able to maintain connectivity information are wires, arcs and polygons. Lines, such as those that are used to show DRC violations, are not treated as part of the net and are ignored. After a design is loaded, PCB examines all the copper on the board and updates its internal net connectivity database. A message informs you that the process is occurring.

  You cannot cancel this operation. Partially routed designs, such as those that require connections to discontiguous copper, take more computing time than designs where the nets are either unrouted or fully routed.

Import and Export Considerations

This section discusses the known considerations for importing and exporting with PCB.

Importing

- Since Master Designer uses a non-proportionally spaced font, text appears slightly different when viewed in PCB.
- PCB does not allow certain characters in names, such as

"-" and "[". They are converted to "_". This affects reference designators, net names and component names.

- Tildes (~) in input files are not treated specially.
- Dotted and dashed lines translate to solid lines, but their line width is preserved.
- Designs greater than 60 inches by 60 inches are not loaded into PCB.
- Text can be a maximum of 5000 mils high in Master Designer. In PCB the limit is 1000 mils, or 1 inch.
- Lines and text in padstacks are ignored.
- Copper Pours in components are converted to polygons.
- Cutouts in components are ignored.
- Master Designer allows 100 layers; PCB allows 99.
- When converting P-CAD pad definitions with an embedded aperture table, PCB does not support the POLYGON and SPECIAL apertures.

Exporting

- Component names are truncated to 8 letters. Unique names are maintained by adding letters or numbers to the end of the name. Also, some Master Designer components are represented as DOS files.
- Text stroke thickness is lost.
- Substring barring is not supported. A~B~C (A B-bar C) outputs as "A~B~C" verbatim.
- Text height cannot be smaller than 2 mils.
- Any text with a single quote (') as the last character in the string will be barred in Master Designer.
- Copper Pour thermals are converted to direct connects in Master Designer.
- Non-uniform grids are lost.

Cleanup Tips

This section lists some helpful tips for cleaning up your PDIF file after importing it into PCB.

Pad and Via Styles

When loading PDIF files, you may sometimes encounter unused pad styles and via styles in your design. You can remove these by selecting the **Options Pad Style** command, then clicking the **Purge Unused Styles** button. Repeat this process with the **Options Via Style** command.