

MITSUBISHI LSTTL_s M74LS641P

OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT(NONINVERTED)

DESCRIPTION

The M74LS641P is a semiconductor integrated circuit containing 8 bus transmitter/receiver circuits with non-inverted open collector outputs.

FEATURES

- Bi-directional transmission or separation of two 8 bit data is possible.
- Open collector outputs
- Hysteresis provided (width = 400mV typical) for input/output A and output/input B
- High fan-out ($I_{OL} = 24mA$)
- Wide operating temperature range. ($T_a = -20 \sim +75^\circ C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

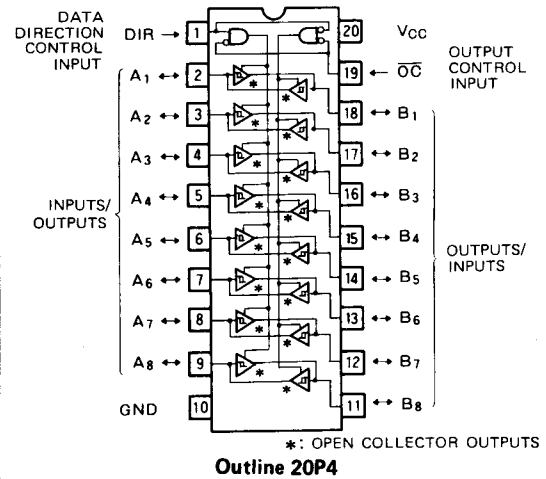
The inputs and outputs of the two buffer circuits with 3-state non-inverted outputs are connected together to form bi-directional buffers. The input sections of input/output A and output/input B have been designed with hysteresis characteristics giving increased noise margin. The input/output direction is controlled by DIR.

When DIR is high, A is the input pin and B is the output pin. When DIR is low then B is input terminal and A is the output terminal. When output control input OC is high, A and B become high so the buffers are isolated.

Open collector outputs are provided, so the high-level output impedance can be freely selected with external load resistors.

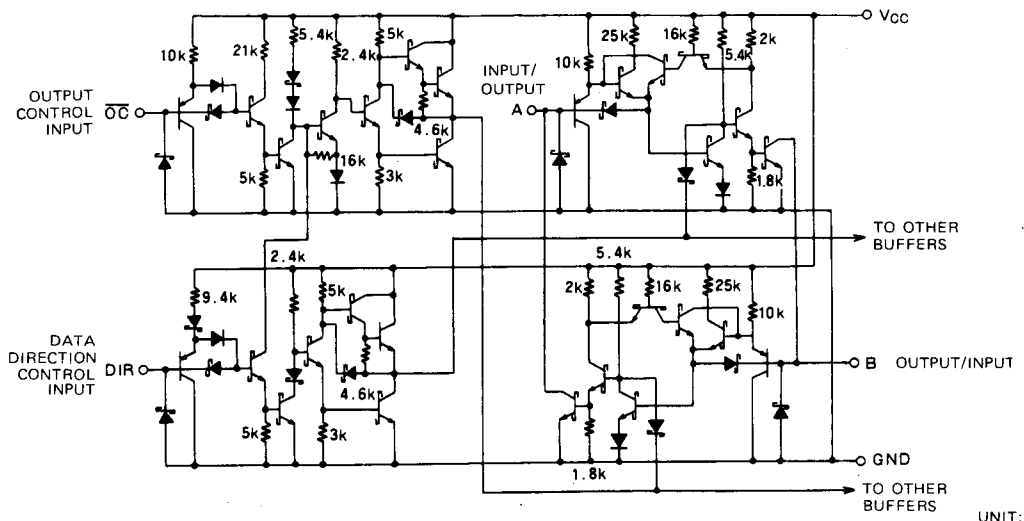
The functions and pin connections of this IC are identical to those of M74LS645P.

PIN CONFIGURATION (TOP VIEW)



A device, M74LS641-1P, having the same pin connections and functions except the value of I_{OL} (= 48mA) has been provided.

CIRCUIT DIAGRAM (Each buffer)



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FUNCTION TABLE (Note 1)

\overline{OC}	DIR	A	B
L	L	O	I
L	H	I	O
H	X	H	H

Note 1: I: Input pin
O: Output (non-inverted output) pin
X: Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7$	V
V_I	Input voltage	A, B	$-0.5 \sim +7$	V
		DIR, \overline{OC}	$-0.5 \sim +15$	V
V_O	Output voltage	High-level state	$-0.5 \sim +7$	V
T_{opr}	Operating free-air ambient temperature range		$-20 \sim +75$	$^\circ\text{C}$
T_{stg}	Storage temperature range		$-65 \sim +150$	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
I_{OH}	High-level output current	$V_O = 5.5\text{V}$	0	100	μA
I_{OL}	Low-level output current	$V_{OL} \leq 0.4\text{V}$	0	12	mA
		$V_{OL} \leq 0.5\text{V}$	0	24	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.6	V
$V_T + - V_T -$	Hysteresis width	$V_{CC} = 4.75\text{V}$	0.2	0.4		V
V_{IC}	Input clamp voltage	$V_{CC} = 4.75\text{V}$, $I_{IC} = -18\text{mA}$			-1.5	V
I_{OH}	High-level output current	$V_{CC} = 4.75\text{V}$, $V_I = 0.6\text{V}$, $V_I = 2\text{V}$, $V_O = 5.5\text{V}$			100	μA
V_{OL}	Low-level output voltage	$V_{CC} = 4.75\text{V}$		0.25	0.4	V
		$V_I = 0.6\text{V}$, $V_I = 2\text{V}$	$I_{OL} = 12\text{mA}$	0.35	0.5	V
I_{IH}	High-level input current	A, B	$V_{CC} = 5.25\text{V}$, $V_I = 2.7\text{V}$		20	μA
		DIR, \overline{OC}			20	μA
		A, B	$V_{CC} = 5.25\text{V}$, $V_I = 5.5\text{V}$		0.1	mA
		DIR, \overline{OC}	$V_{CC} = 5.25\text{V}$, $V_I = 10\text{V}$		0.1	mA
I_{IL}	Low-level input current	$V_{CC} = 5.25\text{V}$, $V_I = 0.4\text{V}$			-0.4	mA
I_{CCH}	Supply current, all outputs high	$V_{CC} = 5.25\text{V}$, $V_I = 0\text{V}$, $V_I = 4.5\text{V}$		48	70	mA
I_{CCL}	Supply current, all outputs low	$V_{CC} = 5.25\text{V}$, $V_I = 0\text{V}$, $V_I = 4.5\text{V}$		62	90	mA
I_{CCZ}	Supply current, all outputs off	$V_{CC} = 5.25\text{V}$, $V_I = 0\text{V}$, $V_I = 4.5\text{V}$		64	95	mA

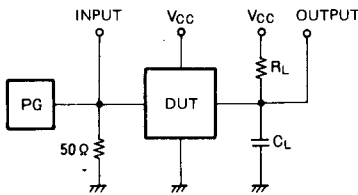
* : All typical values are at $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$.

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SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high level output propagation time	$C_L=45pF, R_L=667\Omega$ (Note 2)		20	25	ns
				20	25	
t_{PHL}	High-to-low level output propagation time			15	25	ns
				15	25	
t_{PLH}	Low-to-high level output propagation time			25	40	ns
				25	40	
t_{PHL}	High-to-low level output propagation time		30	50	ns	
			30	50		

Note 2: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, $t_r = 6ns$, $t_f = 6ns$, $t_w = 500ns$, $V_p = 3V_{p-p}$, $Z_o = 50\Omega$
- (2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)

