

FAST 74F412, 74F432

Multi-Mode Buffered Latches

'F412 Multi-Mode Buffered Latch, Non-Inverting (3-State)
'F432 Multi-Mode Buffered Latch, Inverting (3-State)
Product Specification

FAST Products

FEATURES

- Status flip-flop for interrupt commands
- Asynchronous or latched Receiver modes
- 'F412 Non-inverting
'F432 Inverting
- 3-State outputs
- 300mil-wide Slim DIP package
- Functional equivalent to Intel 8212 except that 'F432 has inverting outputs

DESCRIPTION

The 'F412/'F432 are 8-bit latch with 3-State output buffers. Also included is a status flip-flop for providing device-busy or request-interrupt commands.

Separate Mode (M) and Select (\bar{S}_0 , S_1) inputs allow data to be stored with the outputs enabled or disabled. The devices can be also operated in a fully transparent mode.

Both 'F412 and 'F432 are functional equivalent to the Intel 8212 except that 'F432 has the inverting outputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F412	8.0ns	45mA
74F432	9.0ns	50mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0^\circ C$ to $+70^\circ C$
24-Pin Plastic Slim DIP (300mil)	N74F412N, N74F432N
24-Pin Plastic SOL	N74F412D, N74F432D

NOTE:

1. For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

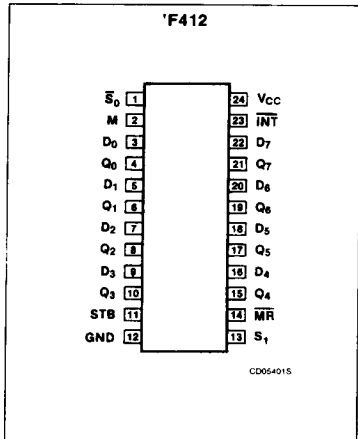
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_7$	Data Inputs	1.0/1.0	20 μ A/0.6mA
\bar{S}_0 , S_1	Select Inputs	1.0/1.0	20 μ A/0.6mA
STB	Strobe Input	1.0/1.0	20 μ A/0.6mA
M	Mode Control Input	1.0/1.0	20 μ A/0.6mA
$\bar{M}\bar{R}$	Master Reset Input	1.0/1.0	20 μ A/0.6mA
$\bar{I}\bar{N}\bar{T}$	Interrupt Output	50/40	1mA/24mA
$Q_0 - Q_7$	Data Latched Outputs	50/40	1mA/24mA

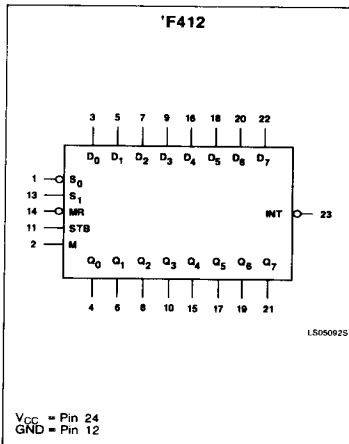
NOTE:

1. One (1.0) FAST Unit Load is defined as: 20 μ A in the High state and 0.6mA in the Low state.

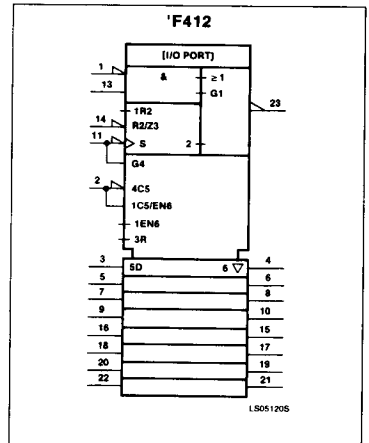
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



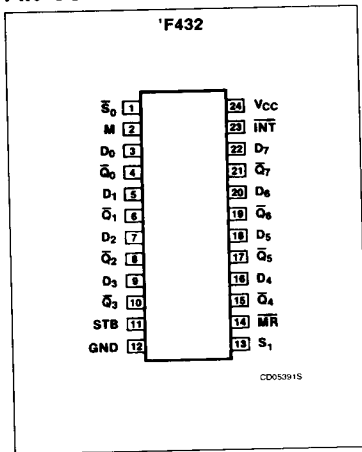
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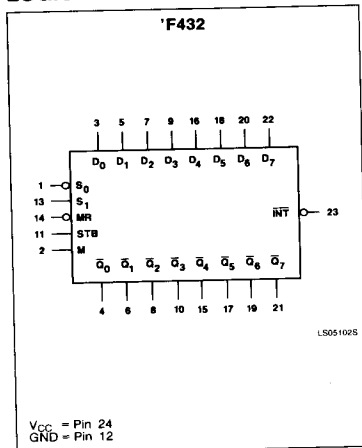
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PIN CONFIGURATION

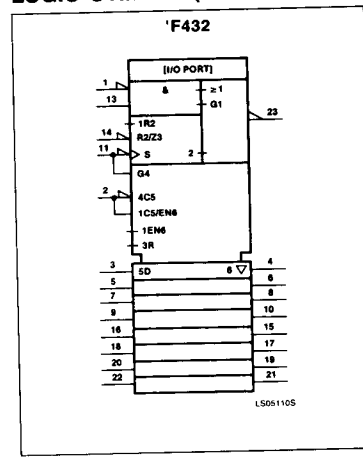


LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DESCRIPTION

This high-performance eight-bit parallel expandable buffer register incorporates package and mode selection inputs and an edge-triggered status flip-flop designed specifically for implementing bus-organized input/output ports. The 3-State data outputs can be connected to a common data bus and controlled from the appropriate select inputs to receive or transmit data. An integral status flip-flop provides busy or request interrupt commands.

The eight data latches are fully transparent when the internal gate enable, G, input is High and the outputs are enabled. Latch transparency is selected by the mode control (M), select (\bar{S}_0 and S_1), and the strobe (STB) inputs and during transparency each data output (Q_n) follows its respective data input (D_n). This mode of operation can be terminated by clearing, de-selecting, or holding the data latches.

An input mode or an output mode is selectable from the M input. In the input mode,

M = L, the eight data latch inputs are enabled when the strobe is High regardless of device selection. If selected during an input mode, the outputs will follow the data inputs. When the strobe input is taken Low, the latches will store the most-recently setup data.

In the output mode, M = H, the output buffers are enabled regardless of any other control input. During the output mode the content of the register is under control of the select (\bar{S}_0 and S_1) inputs.

FUNCTION TABLE

(for Data Latches)

INPUTS					DATA IN	DATA OUT		OPERATING MODE
\bar{MR}	M	\bar{S}_0	S_1	STB		'F412	'F432	
L	H	H	X	X	X	L	H	Clear
L	L	L	H	L	X	L	H	
X	L	X	L	X	X	Z	Z	De-select
X	L	H	X	X	X	Z	Z	
H	H	H	L	X	X	Q_0	\bar{Q}_0	Hold
H	L	L	H	L	X	Q_0	\bar{Q}_0	
H	H	L	H	X	L	L	H	Data Bus
H	H	L	H	X	H	H	L	
H	L	L	H	H	L	L	H	Data Bus
H	L	L	H	H	H	H	L	

FUNCTION TABLE

(for Status Flip-flop)

INPUTS				INT
\bar{MR}	\bar{S}_0	S_1	STB	
L	H	X	X	H
L	X	L	X	H
H	X	X	↑	L
H	L	H	X	L

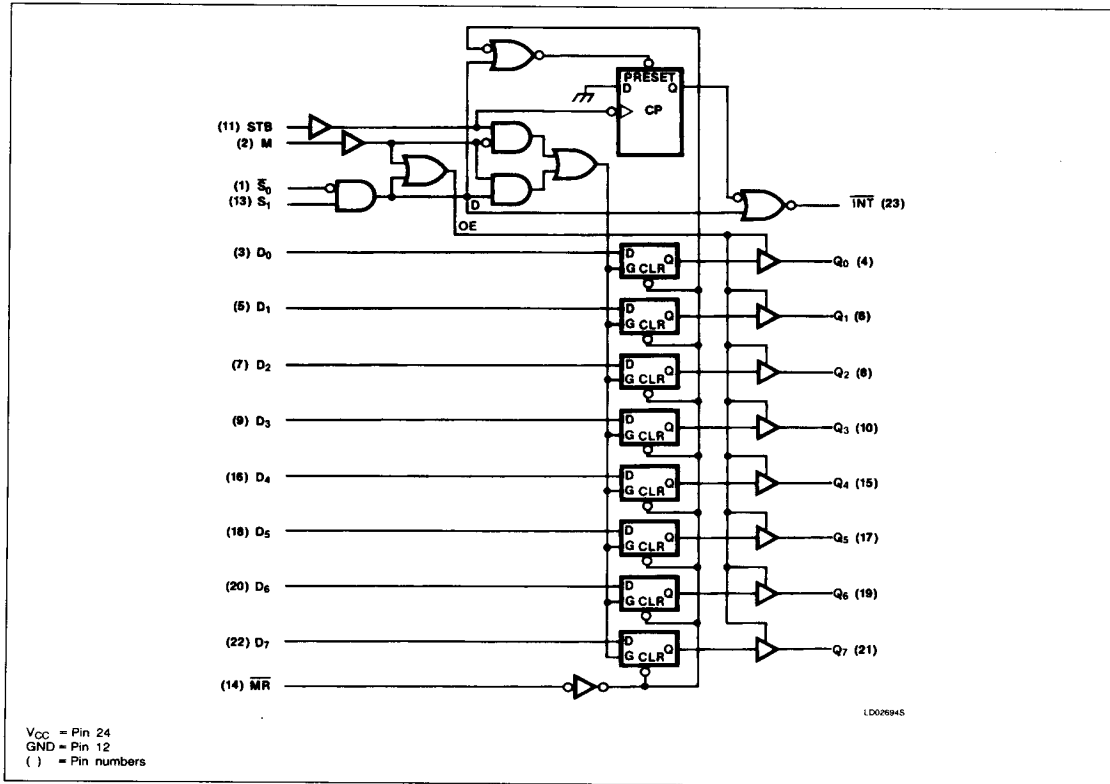
NOTES:

- H = High voltage level
- L = Low voltage level
- X = Don't care
- ↑ = Low-to-High clock transition

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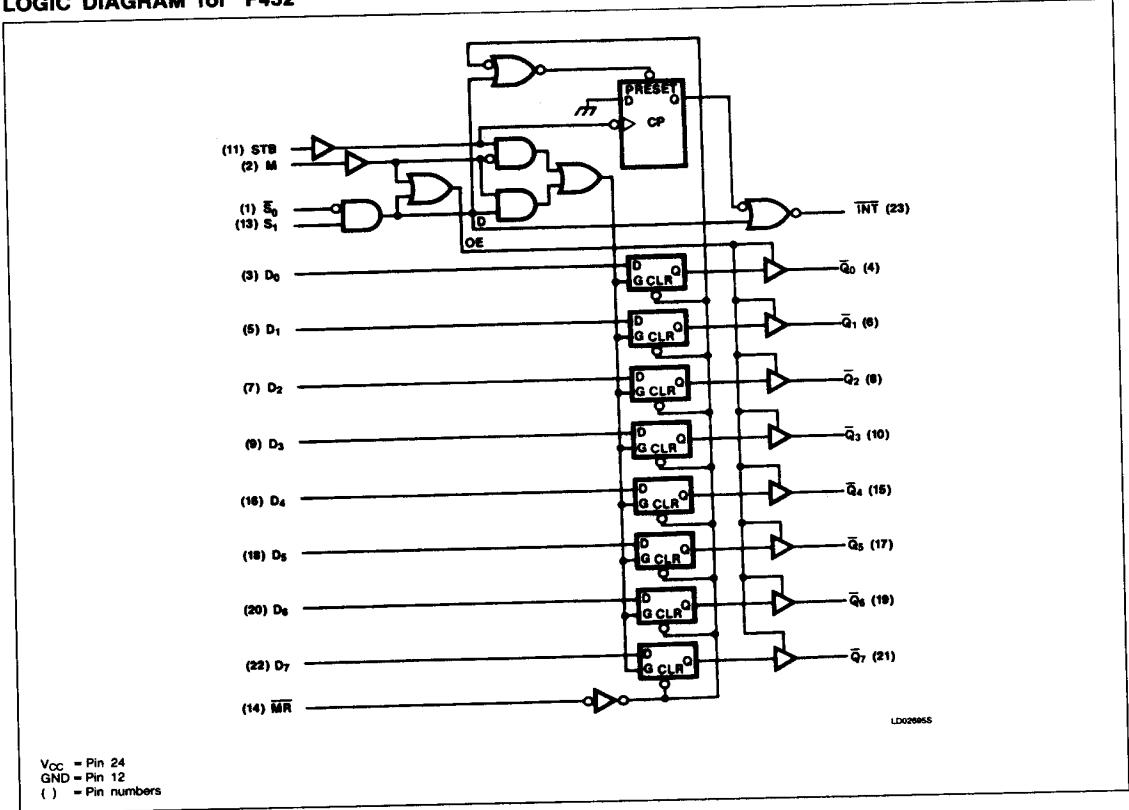
LOGIC DIAGRAM for 'F412



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LOGIC DIAGRAM for 'F432



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DATA LATCHES FUNCTION TABLE

INPUTS					DATA IN	DATA OUT		OPERATING MODE
MR	M	\bar{S}_0	S ₁	STB		'F412	'F432	
L	H	H	X	X	X	L	H	Clear
L	L	L	H	L	X	L	H	
X	L	X	L	X	X	Z	Z	De-select
X	L	H	X	X	X	Z	Z	
H	H	H	X	X	X	Q ₀	\bar{Q}_0	Hold
H	L	L	H	L	X	Q ₀	\bar{Q}_0	
H	H	L	H	X	L	L	H	Data Bus
H	H	L	H	X	H	H	L	
H	L	L	H	H	L	L	H	Data Bus
H	L	L	H	H	H	H	L	

H = High voltage level

L = Low voltage level

X = Don't care

Z = High-impedance

STATUS FLIP-FLOP
FUNCTION TABLE

INPUTS				OUTPUT
MR	\bar{S}_0	S ₁	STB	INT
L	H	X	X	H
L	X	L	X	H
H	X	X	↓	L
H	H	H	X	L

H = High voltage level

L = Low voltage level

X = Don't care

↓ = High-to-Low clock transition

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ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V _{CC}	Supply voltage		-0.5 to +7.0	V
V _{IN}	Input voltage		-0.5 to +7.0	V
I _{IN}	Input current		-30 to +5.0	mA
V _{OUT}	Voltage applied to output in High output state		-0.5 to +V _{CC}	V
I _{OUT}	Current applied to output in Low output state	INT	40	mA
		Q ₀ - Q ₇	48	mA
T _A	Operating free-air temperature range		0 to +70	°C
T _{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{IH}	High-level input voltage	2.0			V
V _{IL}	Low-level input voltage			0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	High-level output current	INT		-1.0	mA
		Q ₀ - Q ₇		-3.0	mA
I _{OL}	Low-level output current	INT		20	mA
		Q ₀ - Q ₇		24	mA
T _A	Operating free-air temperature	0		70	°C

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ¹			74F412, 74F532			UNIT
						Min	Typ ²	Max	
V _{OH}	High-level output voltage		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OH} = -1mA	± 10%V _{CC}	2.5			V
					± 5%V _{CC}	2.7	3.4		V
				I _{OH} = -3mA	± 10%V _{CC}	2.4			V
					± 5%V _{CC}	2.7	3.4		V
V _{OL}	Low-level output voltage		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OL} = MAX	± 10%V _{CC}		0.35	0.50	V
					± 5%V _{CC}		0.35	0.50	V
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = I _{IK}				-0.73	-1.2	V
I _I	Input current at maximum input voltage		V _{CC} = MAX, V _I = 7.0V					100	μA
I _{IH}	High-level input current		V _{CC} = MAX, V _I = 2.7V					20	μA
I _{IL}	Low-level input current		V _{CC} = MAX, V _I = 0.5V					-0.6	mA
I _{OZH}	OFF-state output current, High-level voltage applied		V _{CC} = MAX, V _O = 2.7V					50	μA
I _{OZL}	OFF-state output current, Low-level voltage applied		V _{CC} = MAX, V _O = 0.5V					-50	μA
I _{OS}	Short-circuit output current ³		V _{CC} = MAX, V _O = 0.0V			-60		-150	mA
I _{CC}	Supply current (total)		'F412	I _{CCH}	V _{CC} = MAX		35	50	mA
				I _{CCL}			45	60	mA
				I _{CCZ}			45	60	mA
			'F432	I _{CCH}			40	55	mA
				I _{CCL}			50	70	mA
				I _{CCZ}			50	65	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

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AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F412					UNIT
			T _A = +25°C V _{CC} = +5.0V C _L = 50pF R _L = 500Ω			T _A = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF R _L = 500Ω		
			Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay D _n to Q _n	Waveform 1	3.5 2.0	6.0 3.5	8.5 6.5	3.0 2.0	9.5 7.5	ns
t _{PLH} t _{PHL}	Propagation delay S ₀ , S ₁ or STB to Q _n	Waveform 1, 2	7.5 7.0	13.0 9.0	17.0 14.0	7.0 6.5	18.5 15.0	ns
t _{PLH} t _{PHL}	Propagation delay S ₀ or S ₁ to INT	Waveform 1, 2	3.0 3.0	6.0 6.5	9.5 10.5	3.0 3.0	10.5 11.5	ns
t _{PHL}	Propagation delay MR to Q _n	Waveform 1	6.0	8.0	12.0	5.5	13.0	ns
t _{PHL}	Propagation delay STB to INT	Waveform 2	6.5	10.0	13.0	5.5	15.0	ns
t _{PZH} t _{PZL}	Output Enable time to High or Low level S ₀ to Q _n	Waveform 5 Waveform 6	7.0 7.0	9.0 10.0	12.5 13.5	6.0 6.0	14.0 15.0	ns
t _{PHZ} t _{PLZ}	Output Disable time from High or Low level S ₀ to Q _n	Waveform 5 Waveform 6	4.5 6.5	7.5 12.0	10.5 15.0	4.0 6.0	12.0 16.5	ns
t _{PZH} t _{PZL}	Output enable time to High or Low level S ₁ to Q _n	Waveform 5 Waveform 6	6.0 6.0	10.0 9.0	13.0 12.0	5.0 5.5	14.0 13.0	ns
t _{PHZ} t _{PLZ}	Output disable time from High or Low level S ₁ to Q _n	Waveform 5 Waveform 6	4.0 6.5	6.0 10.0	9.5 13.5	3.5 6.0	10.5 15.0	ns
t _{PZH} t _{PZL}	Output enable time to High or Low level M to Q _n	Waveform 5 Waveform 6	5.0 5.0	8.5 8.5	11.0 11.0	4.5 4.5	12.0 12.0	ns
t _{PHZ} t _{PLZ}	Output disable time from High or Low level M to Q _n	Waveform 5 Waveform 6	4.0 6.0	6.5 9.5	9.0 12.5	3.5 5.5	10.0 14.0	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F412					UNIT
			T _A = +25°C V _{CC} = +5.0V C _L = 50pF R _L = 500Ω			T _A = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF R _L = 500Ω		
			Min	Typ	Max	Min	Max	
t _s (H) t _s (L)	Setup time, High or Low D _n to S ₀ , S ₁ or STB	Waveform 3	0 0			1.0 1.0		ns
t _h (H) t _h (L)	Hold time, High or Low D _n to S ₀ , S ₁ , STB, or M	Waveform 3	8.0 8.0			9.0 9.0		ns
t _w (H) t _w (L)	S ₀ , S ₁ , M, or STB pulse Pulse width, High or Low	Waveform 3	8.0 8.0			9.0 9.0		ns
t _w (L)	MR pulse width	Waveform 4	8.0			9.0		ns
t _{rec}	Recovery time MR to STB	Waveform 4	0			0		ns

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AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F432					UNIT
			T _A = +25°C V _{CC} = +5.0V C _L = 50pF R _L = 500Ω			T _A = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF R _L = 500Ω		
			Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay D _n to Q _n	Waveform 2	4.5 2.5	7.5 4.5	10.5 7.0	4.0 2.5	12.0 8.0	ns
t _{PLH} t _{PHL}	Propagation delay S ₀ , S ₁ or STB to Q _n	Waveform 1, 2	8.5 6.0	14.0 9.5	17.0 13.0	8.0 5.5	19.0 14.0	ns
t _{PLH} t _{PHL}	Propagation delay S ₀ or S ₁ to INT	Waveform 1, 2	3.0 3.5	6.0 6.5	9.5 10.0	2.5 3.0	10.5 10.5	ns
t _{PLH}	Propagation delay M _R to Q _n	Waveform 2	8.0	12.0	16.0	7.5	17.0	ns
t _{PHL}	Propagation delay STB to INT	Waveform 2	7.0	10.0	13.5	6.5	14.5	ns
t _{PZH} t _{PZL}	Output Enable time to High or Low level S ₀ or S ₁ to Q _n	Waveform 5 Waveform 6	6.0 6.0	9.0 11.0	12.5 14.0	5.5 5.5	14.0 15.0	ns
t _{PHZ} t _{PLZ}	Output Disable time from High or Low level S ₀ or S ₁ to Q _n	Waveform 5 Waveform 6	4.0 6.0	7.5 11.5	11.5 15.0	3.5 5.5	12.5 16.5	ns
t _{PZH} t _{PZL}	Output enable time to High or Low level M to Q _n	Waveform 5 Waveform 6	5.0 6.0	7.5 8.0	11.0 11.5	4.5 5.5	12.0 13.0	ns
t _{PHZ} t _{PLZ}	Output disable time from High or Low level M to Q _n	Waveform 5 Waveform 6	3.5 6.0	6.0 10.0	9.5 13.0	3.0 5.5	10.5 13.5	ns

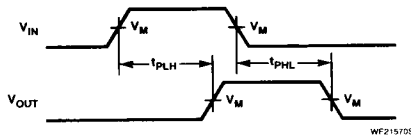
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F432					UNIT
			T _A = +25°C V _{CC} = +5.0V C _L = 50pF R _L = 500Ω			T _A = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF R _L = 500Ω		
			Min	Typ	Max	Min	Max	
t _s (H) t _s (L)	Setup time, High or Low D _n to S ₀ , S ₁ or STB or M	Waveform 3	0 0			1.0 1.0		ns
t _h (H) t _h (L)	Hold time, High or Low D _n to S ₀ , S ₁ or STB or M	Waveform 3	9.0 8.0			9.5 8.5		ns
t _w (H) t _w (L)	S ₀ , S ₁ , M or STB Pulse width, High or Low	Waveform 3	8.0 8.0			9.0 9.0		ns
t _w (L)	M _R pulse width Low	Waveform 4	8.0			9.0		ns
t _{rec}	Recovery Time M _R to STB	Waveform 4	0			0		ns

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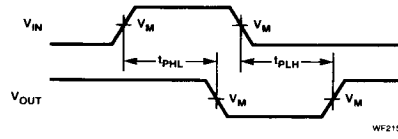
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AC WAVEFORMS



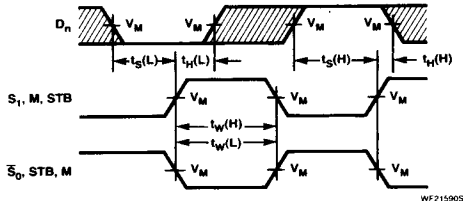
WF215705

Waveform 1. Propagation Delay for Non-Inverting Outputs



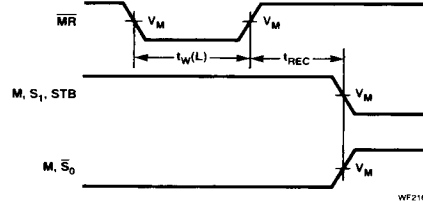
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Waveform 2. Propagation Delay for Inverting Outputs



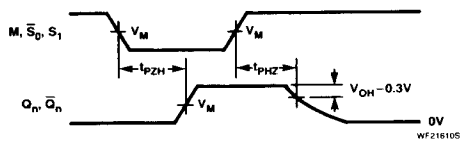
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Waveform 3. Setup and Hold Times



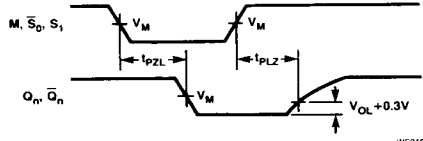
WF216905

Waveform 4. Recovery Times



WF216105

Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time From High Level



WF216205

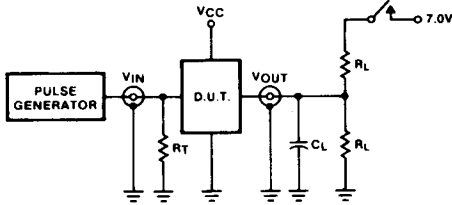
Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

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TEST CIRCUIT AND WAVEFORMS



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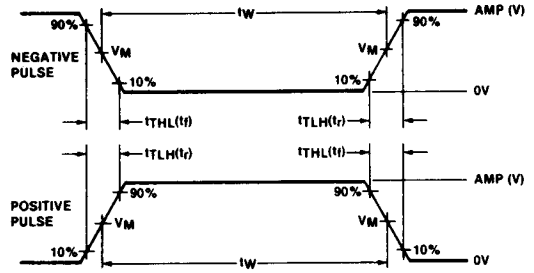
Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance;
 see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT}
 of pulse generators.



WF004505

$V_M = 1.5V$
 Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns