Features

- High Performance, Low Power 32-bit AVR® Microcontroller
  - Compact Single-Cycle RISC Instruction Set Including DSP Instruction Set
  - Read-Modify-Write Instructions and Atomic Bit Manipulation
  - Performing up to 1.51 DMIPS/MHz
    - Up to 92 DMIPS Running at 66 MHz from Flash (1 Wait-State)
    - Up to 54 DMIPS Running at 36 MHz from Flash (0 Wait-State)
  - Memory Protection Unit
- Multi-Layer Bus System
  - High-Performance Data Transfers on Separate Buses for Increased Performance
  - 8 Peripheral DMA Channels (PDCA) Improves Speed for Peripheral Communication
  - 4 generic DMA Channels for High Bandwidth Data Paths
- Internal High-Speed Flash
  - 256 KBytes, 128 KBytes, 64 KBytes versions
  - Single-Cycle Flash Access up to 36 MHz
  - Prefetch Buffer Optimizing Instruction Execution at Maximum Speed
  - 4 ms Page Programming Time and 8 ms Full-Chip Erase Time
  - 100,000 Write Cycles, 15-year Data Retention Capability
  - Flash Security Locks and User Defined Configuration Area
- Internal High-Speed SRAM
  - 64 KBytes Single-Cycle Access at Full Speed, Connected to CPU Local Bus
  - 64 KBytes (2x32KBytes with independent access) on the Multi-Layer Bus System
- Interrupt Controller
  - Autovectored Low Latency Interrupt Service with Programmable Priority
- System Functions
  - Power and Clock Manager Including Internal RC Clock and One 32 KHz Oscillator
  - Two Multipurpose Oscillators and Two Phase-Lock-Loop (PLL),
  - Watchdog Timer, Real-Time Clock Timer
- External Memories
  - Support SDRAM, SRAM, NandFlash (1-bit and 4-bit ECC), Compact Flash
  - Up to 66 MHz
- External Storage device support
  - MultiMediaCard (MMC V4.3), Secure-Digital (SD V2.0), SDIO V1.1
  - CE-ATA V1.1, FastSD, SmartMedia, Compact Flash
  - Memory Stick: Standard Format V1.40, PRO Format V1.00, Micro
  - IDE Interface
- One Advanced Encryption System (AES) for AT32UC3A3256S, AT32UC3A3128S, AT32UC3A364S, AT32UC3A4256S, AT32UC3A4128S and AT32UC3A364S
  - 256-, 192-, 128-bit Key Algorithm, Compliant with FIPS PUB 197 Specifications
  - Buffer Encryption/Decryption Capabilities
- Universal Serial Bus (USB)
  - High-Speed USB (480 Mbit/s) Device/MiniHost with On-The-Go (OTG)
  - Flexible End-Point Configuration and Management with Dedicated DMA Channels
  - On-Chip Transceivers Including Pull-Ups
- One 8-channel 10-bit Analog-To-Digital Converter, multiplexed with Digital IOs.
- Two Three-Channel 16-bit Timer/Counter (TC)
- Four Universal Synchronous/Asynchronous Receiver/Transmitters (USART)
  - Fractionnal Baudrate Generator

32-bit AVR® Microcontroller

AT32UC3A3256S
AT32UC3A3256
AT32UC3A3128S
AT32UC3A3128
AT32UC3A364S
AT32UC3A364
AT32UC3A4256S
AT32UC3A4256
AT32UC3A4128S
AT32UC3A4128
AT32UC3A464S
AT32UC3A464

Preliminary

32072C–03/2010

  - Support for SPI and LIN
  - Optionnal support for IrDA, ISO7816, Hardware Handshaking, RS485 interfaces and Modem Line
- Two Master/Slave Serial Peripheral Interfaces (SPI) with Chip Select Signals
- One Synchronous Serial Protocol Controller
  - Supports I2S and Generic Frame-Based Protocols
- Two Master/Slave Two-Wire Interface (TWI), 400kbit/s I2C-compatible
- 16-bit Stereo Audio Bitstream
  - Sample Rate Up to 50 KHz
- On-Chip Debug System (JTAG interface)
  - Nexus Class 2+, Runtime Control, Non-Intrusive Data and Program Trace
- 110 General Purpose Input/Output (GPIOs)
  - Standard or High Speed mode
  - Toggle capability: up to 66MHz
- Packages
  - 144-ball TFBGA, 11x11 mm, pitch 0.8 mm
  - 144-pin LQFP, 22x22 mm, pitch 0.5 mm
  - 100-ball VFBGA, 7x7 mm, pitch 0.65 mm
- Single 3.3V Power Supply

1. Description

The AT32UC3A3/A4 is a complete System-On-Chip microcontroller based on the AVR32 UC RISC processor running at frequencies up to 66MHz. AVR32 UC is a high-performance 32-bit RISC microprocessor core, designed for cost-sensitive embedded applications, with particular emphasis on low power consumption, high code density and high performance.

The processor implements a Memory Protection Unit (MPU) and a fast and flexible interrupt controller for supporting modern operating systems and real-time operating systems. Higher computation capabilities are achievable using a rich set of DSP instructions.

The AT32UC3A3/A4 incorporates on-chip Flash and SRAM memories for secure and fast access. 64 KBytes of SRAM are directly coupled to the AVR32 UC for performances optimization. Two blocks of 32 Kbytes SRAM are independently attached to the High Speed Bus Matrix, allowing real ping-pong management.

The Peripheral Direct Memory Access Controller (PDCA) enables data transfers between peripherals and memories without processor involvement. The PDCA drastically reduces processing overhead when transferring continuous and large data streams.

The Power Manager improves design flexibility and security: the on-chip Brown-Out Detector monitors the power supply, the CPU runs from the on-chip RC oscillator or from one of external oscillator sources, a Real-Time Clock and its associated timer keeps track of the time.

The device includes two sets of three identical 16-bit Timer/Counter (TC) channels. Each channel can be independently programmed to perform frequency measurement, event counting, interval measurement, pulse generation, delay timing and pulse width modulation. 16-bit channels are combined to operate as 32-bit channels.

The AT32UC3A3/A4 also features many communication interfaces for communication intensive applications like UART, SPI or TWI. Additionally, a flexible Synchronous Serial Controller (SSC) is available. The SSC provides easy access to serial communication protocols and audio standards like I2S.

The AT32UC3A3/A4 includes a powerfull External Bus Interface to interface all standard memory device like SRAM, SDRAM, NAND Flash or parallel interfaces like LCD Module.

The peripheral set includes a High Speed MCI for SDIO/SD/MMC and a hardware encryption module based on AES algorithm.

The device embeds a 10-bit ADC and a Digital Audio bistream DAC.

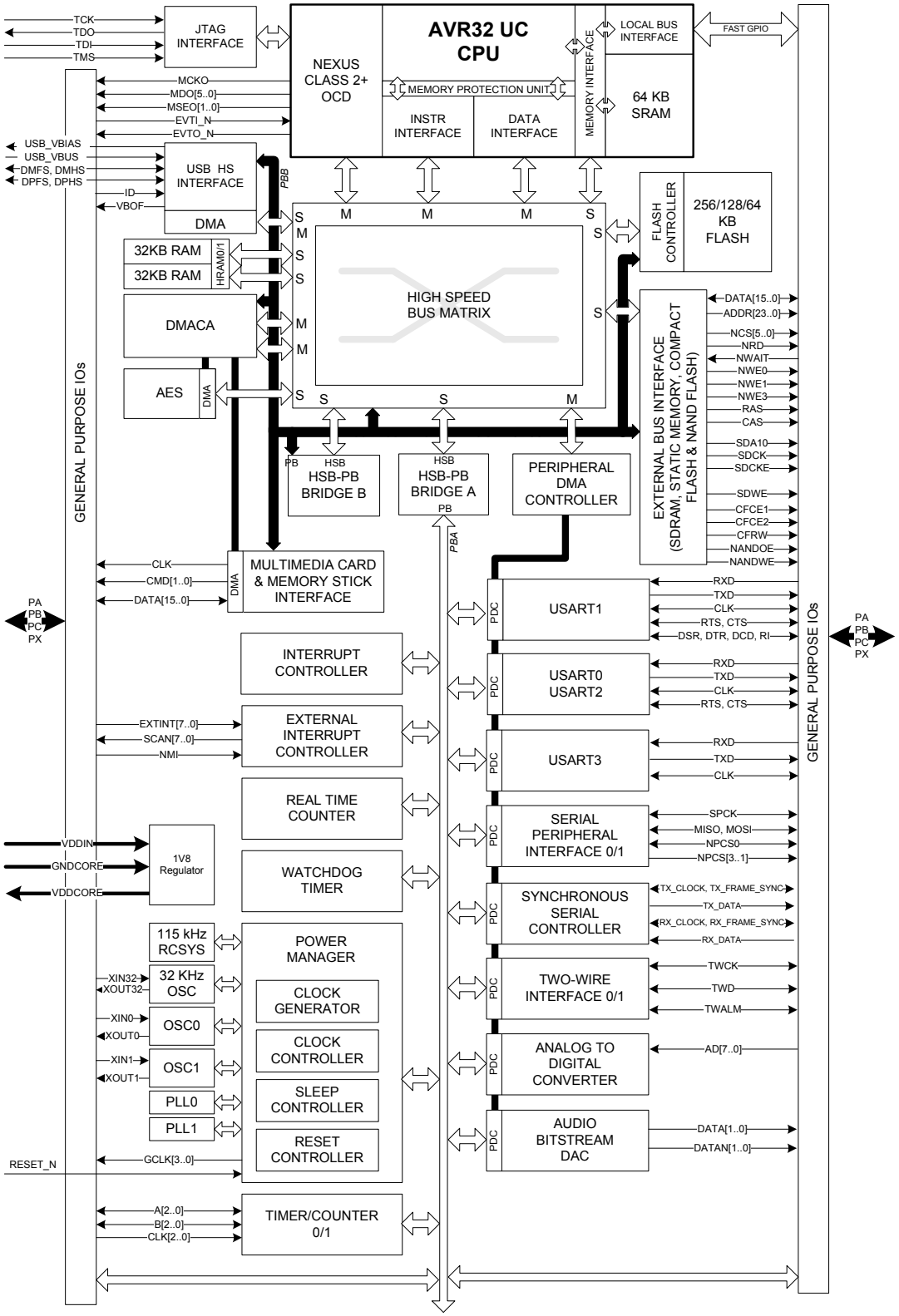
The Direct Memory Access controller (DMACA) allows high bandwidth data flows between high speed peripherals (USB, External Memories, MMC, SDIO, ...) and through high speed internal features (AES, internal memories).

The High-Speed (480MBit/s) USB 2.0 Device and Host interface supports several USB Classes at the same time thanks to the rich Endpoint configuration. The On-The-Go (OTG) Host interface allows device like a USB Flash disk or a USB printer to be directly connected to the processor. This periphal has its own dedicated DMA and is perfect for Mass Storage application.

AT32UC3A3/A4 integrates a class 2+ Nexus 2.0 On-Chip Debug (OCD) System, with non-intrusive real-time trace, full-speed read/write memory access in addition to basic runtime control.

2. Blockdiagram

Figure 2-1. Blockdiagram



2.1 Processor and Architecture

2.1.1 AVR32 UC CPU

- 32-bit load/store AVR32A RISC architecture
  - 15 general-purpose 32-bit registers
  - 32-bit Stack Pointer, Program Counter and Link Register reside in register file
  - Fully orthogonal instruction set
  - Privileged and unprivileged modes enabling efficient and secure Operating Systems
  - Innovative instruction set together with variable instruction length ensuring industry leading code density
  - DSP extension with saturating arithmetic, and a wide variety of multiply instructions
- Three stage pipeline allows one instruction per clock cycle for most instructions
  - Byte, halfword, word and double word memory access
  - Multiple interrupt priority levels
- MPU allows for operating systems with memory protection

2.1.2 Debug and Test System

- IEEE1149.1 compliant JTAG and boundary scan
- Direct memory access and programming capabilities through JTAG interface
- Extensive On-Chip Debug features in compliance with IEEE-ISTO 5001-2003 (Nexus 2.0) Class 2+
  - Low-cost NanoTrace supported
- Auxiliary port for high-speed trace information
- Hardware support for six Program and two data breakpoints
- Unlimited number of software breakpoints supported
- Advanced Program, Data, Ownership and Watchpoint trace supported

2.1.3 Peripheral DMA Controller

- Transfers from/to peripheral to/from any memory space without intervention of the processor
- Next Pointer Support, forbids strong real-time constraints on buffer management
- Eight channels and 24 Handshake interfaces
  - Two for each USART
  - Two for each Serial Synchronous Controller (SSC)
  - Two for each Serial Peripheral Interface (SPI)
  - One for ADC
  - Four for each TWI Interface
  - Two for each Audio Bit Stream DAC

2.1.4 Bus System

- High Speed Bus (HSB) matrix with 7 Masters and 10 Slaves handled
  - Handles Requests from
    - Masters: the CPU (Instruction and Data Fetch), PDCA, CPU SAB, USBB, DMACA
    - Slaves: the internal Flash, internal SRAM, Peripheral Bus A, Peripheral Bus B, External Bus Interface (EBI), Advanced Encrytion Standard (AES)
  - Round-Robin Arbitration (three modes supported: no default master, last accessed default master, fixed default master)
  - Burst breaking with Slot Cycle Limit
  - One address decoder provided per master
- Peripheral Bus A able to run on at divided bus speeds compared to the High Speed Bus

3. Signals Description

The following table gives details on the signal name classified by peripheral

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
Power				
VDDIO	I/O Power Supply	Power		3.0 to 3.6 V
VDDANA	Analog Power Supply	Power		3.0 to 3.6 V
VDDIN	Voltage Regulator Input Supply	Power		2.7 to 3.6 V
ONREG	Voltage Regulator ON/OFF	Power Control	1	2.7 to 3.6 V
VDDCORE	Voltage Regulator Output for Digital Supply	Power Output		1.65 to 1.95V
GNDANA	Analog Ground	Ground		
GNDIO	I/O Ground	Ground		
GNDCORE	DIgital Ground	Ground		
GNDPLL	PLL Ground	Ground		
Clocks, Oscillators, and PLL's				
XIN0, XIN1, XIN32	Crystal 0, 1, 32 Input	Analog		
XOUT0, XOUT1, XOUT32	Crystal 0, 1, 32 Output	Analog		
JTAG				
TCK	Test Clock	Input		
TDI	Test Data In	Input		
TDO	Test Data Out	Output		
TMS	Test Mode Select	Input		
Auxiliary Port - AUX				
MCKO	Trace Data Output Clock	Output		
MDO[5:0]	Trace Data Output	Output		
MSEO[1:0]	Trace Frame Control	Output		
EVTI_N	Event In	Output	Low	
EVTO_N	Event Out	Output	Low	
Power Manager - PM				

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
GCLK[2:0]	Generic Clock Pins	Output		
RESET_N	Reset Pin	Input	Low	
DMA Controller - DMACA (optional)				
DMAACK[1:0]	DMA Acknowledge	Output		
DMARQ[1:0]	DMA Requests	Input		
External Interrupt Module - EIM				
EXTINT[7:0]	External Interrupt Pins	Input		
KPS0 - KPS7	Keypad Scan Pins	Output		
NMI_N	Non-Maskable Interrupt Pin	Input	Low	
General Purpose Input/Output pin - GPIOA, GPIOB, GPIOC, GPIOX				
PA[31:0]	Parallel I/O Controller GPIOA	I/O		
PB[11:0]	Parallel I/O Controller GPIOB	I/O		
PC[5:0]	Parallel I/O Controller GPIOC	I/O		
PX[59:0]	Parallel I/O Controller GPIO X	I/O		
External Bus Interface - EBI				
ADDR[23:0]	Address Bus	Output		
CAS	Column Signal	Output	Low	
CFCE1	Compact Flash 1 Chip Enable	Output	Low	
CFCE2	Compact Flash 2 Chip Enable	Output	Low	
CFRNW	Compact Flash Read Not Write	Output		
DATA[15:0]	Data Bus	I/O		
NANDOE	NAND Flash Output Enable	Output	Low	
NANDWE	NAND Flash Write Enable	Output	Low	
NCS[5:0]	Chip Select	Output	Low	
NRD	Read Signal	Output	Low	
NWAIT	External Wait Signal	Input	Low	
NWE0	Write Enable 0	Output	Low	
NWE1	Write Enable 1	Output	Low	

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
RAS	Row Signal	Output	Low	
SDA10	SDRAM Address 10 Line	Output		
SDCK	SDRAM Clock	Output		
SDCKE	SDRAM Clock Enable	Output		
SDCS	SDRAM Chip Select	Output	Low	
SDWE	SDRAM Write Enable	Output	Low	
MultiMedia Card Interface - MCI				
CLK	Multimedia Card Clock	Output		
CMD[1:0]	Multimedia Card Command	I/O		
DATA[15:0]	Multimedia Card Data	I/O		
Serial Peripheral Interface - SPI0				
MISO	Master In Slave Out	I/O		
MOSI	Master Out Slave In	I/O		
NPCS[3:0]	SPI Peripheral Chip Select	I/O	Low	
SCK	Clock	Output		
Synchronous Serial Controller - SSC				
RX_CLOCK	SSC Receive Clock	I/O		
RX_DATA	SSC Receive Data	Input		
RX_FRAME_SYNC	SSC Receive Frame Sync	I/O		
TX_CLOCK	SSC Transmit Clock	I/O		
TX_DATA	SSC Transmit Data	Output		
TX_FRAME_SYNC	SSC Transmit Frame Sync	I/O		
Timer/Counter - TC0, TC1				
A0	Channel 0 Line A	I/O		
A1	Channel 1 Line A	I/O		
A2	Channel 2 Line A	I/O		
B0	Channel 0 Line B	I/O		
B1	Channel 1 Line B	I/O		

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
B2	Channel 2 Line B	I/O		
CLK0	Channel 0 External Clock Input	Input		
CLK1	Channel 1 External Clock Input	Input		
CLK2	Channel 2 External Clock Input	Input		
Two-wire Interface - TWI0, TWI1				
SCL	Serial Clock	I/O		
SDA	Serial Data	I/O		
Universal Synchronous Asynchronous Receiver Transmitter - USART0, USART1, USART2, USART3				
CLK	Clock	I/O		
CTS	Clear To Send	Input		
DCD	Data Carrier Detect			Only USART1
DSR	Data Set Ready			Only USART1
DTR	Data Terminal Ready			Only USART1
RI	Ring Indicator			Only USART1
RTS	Request To Send	Output		
RXD	Receive Data	Input		
RXDN	Inverted Receive Data	Input	Low	
TXD	Transmit Data	Output		
TXDN	Inverted Transmit Data	Output	Low	
Analog to Digital Converter - ADC				
AD0 - AD7	Analog input pins	Analog input		
Audio Bitstream DAC (ABDAC)				
DATA0-DATA1	D/A Data out	Output		
DATAN0-DATAN1	D/A Data inverted out	Output		
Universal Serial Bus Device - USB				
FSDM	USB Full Speed Data -	Analog		
FSDP	USB Full Speed Data +	Analog		
HSDM	USB High Speed Data -	Analog		

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
HSDP	USB High Speed Data +	Analog		
USB_VBIAS	USB VBIAS reference	Analog		Connect to the ground through a 6810ohms (+/- 0.5%) resistor
USB_VBUS	USB VBUS for OTG feature	Output		

4. Package and Pinout

4.1 Package

The device pins are multiplexed with peripheral functions as described in the Peripheral Multiplexing on I/O Line section.

Figure 4-1. TFBGA144 Pinout (top view)

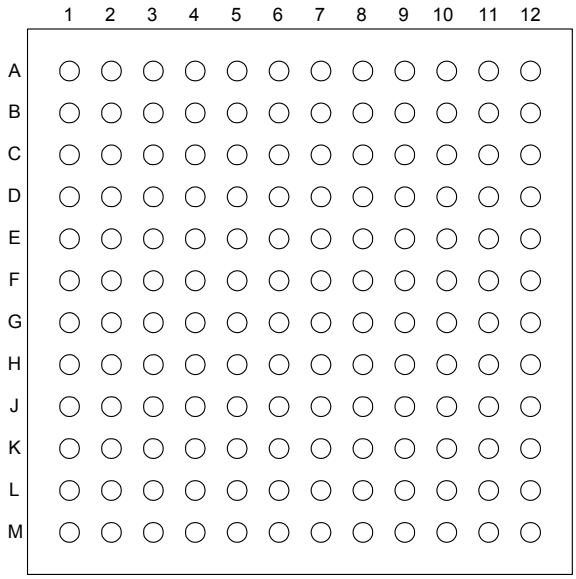


Table 4-1. TFBGA144 Package Pinout

	1	2	3	4	5	6	7	8	9	10	11	12
A	PX40	PB00	PA28	PA27	PB03	PA29	PC02	PC04	PC05	DPHS	DMHS	USB_VBUS
B	PX10	PB11	PA31	PB02	VDDIO	PB04	PC03	VDDIO	USB_VBIAS	DMFS	GNDPLL	PA09
C	PX09	PX35	GNDIO	PB01	PX16	PX13	PA30	PB08	DPFS	GNDCORE	PA08	PA10
D	PX08	PX37	PX36	PX47	PX19	PX12	PB10	PA02	PA26	PA11	PB07	PB06
E	PX38	VDDIO	PX54	PX53	VDDIO	PX15	PB09	VDDIN	PA25	PA07	VDDCORE	PA12
F	PX39	PX07	PX06	PX49	PX48	GNDIO	GNDIO	PA06	PA04	PA05	PA13	PA16
G	PX00	PX05	PX59	PX50	PX51	GNDIO	GNDIO	PA23	PA24	PA03	PA00	PA01
H	PX01	VDDIO	PX58	PX57	VDDIO	PC01	PA17	VDDIO	PA21	PA22	VDDANA	PB05
J	PX04	PX02	PX34	PX56	PX55	PA14	PA15	PA19	PA20	TMS	TDO	RESET_N
K	PX03	PX44	GNDIO	PX46	PC00	PX17	PX52	PA18	PX27	GNDIO	PX29	TCK
L	PX11	GNDIO	PX45	PX20	VDDIO	PX18	PX43	VDDIN	PX26	PX28	GNDANA	TDI
M	PX22	PX41	PX42	PX14	PX21	PX23	PX24	PX25	PX32	PX31	PX30	PX33

Figure 4-2. LQFP144 Pinout

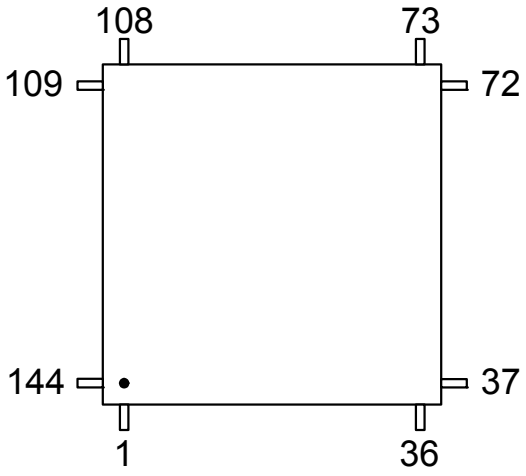


Table 4-2. LQFP144 Package Pinout

1	USB_VBUS	**25**	PB02	**49**	PX09	**73**	PX20	**97**	PX31	**121**	PB05
2	VDDIO	**26**	PA27	**50**	PX08	**74**	PX46	**98**	PC00	**122**	PA00
3	USB_VBIAS	**27**	PB01	**51**	PX38	**75**	PX50	**99**	PC01	**123**	PA01
4	GNDIO	**28**	PA28	**52**	PX39	**76**	PX57	**100**	PA14	**124**	PA05
5	DMHS	**29**	PA31	**53**	PX06	**77**	PX51	**101**	PA15	**125**	PA03
6	DPHS	**30**	PB00	**54**	PX07	**78**	PX56	**102**	GNDIO	**126**	PA04
7	GNDIO	**31**	PB11	**55**	PX00	**79**	PX55	**103**	VDDIO	**127**	PA06
8	DMFS	**32**	PX16	**56**	PX59	**80**	PX21	**104**	TMS	**128**	PA16
9	DPFS	**33**	PX13	**57**	PX58	**81**	VDDIO	**105**	TDO	**129**	PA13
10	VDDIO	**34**	PX12	**58**	PX05	**82**	GNDIO	**106**	RESET_N	**130**	VDDIO
11	PB08	**35**	PX19	**59**	PX01	**83**	PX17	**107**	TCK	**131**	GNDIO
12	PC05	**36**	PX40	**60**	PX04	**84**	PX18	**108**	TDI	**132**	PA12
13	PC04	**37**	PX10	**61**	PX34	**85**	PX23	**109**	PA21	**133**	PA07
14	PA30	**38**	PX35	**62**	PX02	**86**	PX24	**110**	PA22	**134**	PB06
15	PA02	**39**	PX47	**63**	PX03	**87**	PX52	**111**	PA23	**135**	PB07
16	PB10	**40**	PX15	**64**	VDDIO	**88**	PX43	**112**	PA24	**136**	PA11
17	PB09	**41**	PX48	**65**	GNDIO	**89**	PX27	**113**	PA20	**137**	PA08
18	PC02	**42**	PX53	**66**	PX44	**90**	PX26	**114**	PA19	**138**	PA10
19	PC03	**43**	PX49	**67**	PX11	**91**	PX28	**115**	PA18	**139**	PA09
20	GNDIO	**44**	PX36	**68**	PX14	**92**	PX25	**116**	PA17	**140**	GNDCORE
21	VDDIO	**45**	PX37	**69**	PX42	**93**	PX32	**117**	GNDANA	**141**	VDDCORE
22	PB04	**46**	PX54	**70**	PX45	**94**	PX29	**118**	VDDANA	**142**	VDDIN
23	PA29	**47**	GNDIO	**71**	PX41	**95**	PX33	**119**	PA25	**143**	VDDIN
24	PB03	**48**	VDDIO	**72**	PX22	**96**	PX30	**120**	PA26	**144**	GNDPLL

Figure 4-3. VFBGA100 Pinout (top view)

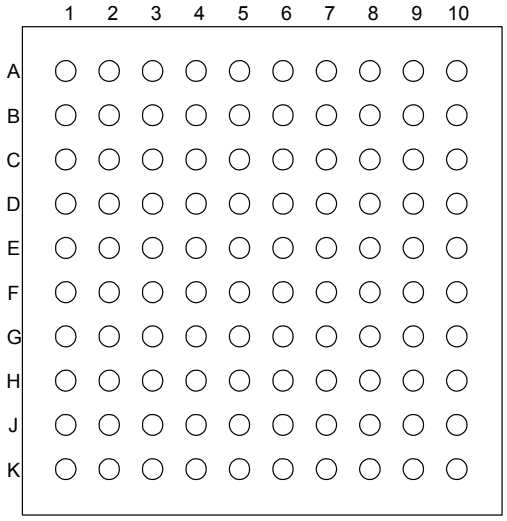


Table 4-3. VFBGA100 Package Pinout

	1	2	3	4	5	6	7	8	9	10
A	PA28	PA27	PB04	PA30	PC02	PC03	PC05	DPHS	DMHS	USB_VBUS
B	PB00	PB01	PB02	PA29	VDDIO	VDDIO	PC04	DPFS	DMFS	GNDPLL
C	PB11	PA31	GNDIO	PB03	PB09	PB08	USB_VBIAS	GNDIO	PA11	PA10
D	PX12	PX10	PX13	PX16/PX53[1]	PB10	PB07	PB06	PA09	VDDIN	VDDIN
E	PA02/PX47[1]	GNDIO	PX08	PX09	VDDIO	GNDIO	PA16	PA06/PA13[1]	PA04	VDDCORE
F	PX19/PX59[1]	VDDIO	PX06	PX07	GNDIO	VDDIO	PA26/PB05[1]	PA08	PA03	GNDCORE
G	PX05	PX01	PX02	PX00	PX30	PA23/PX46[1]	PA12/PA25[1]	PA00/PA18[1]	PA05	PA01/PA17[1]
H	PX04	PX21	GNDIO	PX25	PX31	PA22/PX20[1]	TMS	GNDANA	PA20/PX18[1]	PA07/PA19[1]
J	PX03	PX24	PX26	PX29	VDDIO	VDDANA	PA15/PX45[1]	TDO	RESET_N	PA24/PX17[1]
K	PX23	PX27	PX28	PX15/PX32[1]	PC00/PX14[1]	PC01	PA14/PX11[1]	TDI	TCK	PA21/PX22[1]

Note: 1. Those balls are physically connected to 2 GPIOs. Software must managed carrefully the GPIO configuration to avoid electrical conflict

4.2 Peripheral Multiplexing on I/O lines

Each GPIO line can be assigned to one of 4 peripheral functions; A, B, C, or D. The following table defines how the I/O lines on the peripherals A, B, C, or D are multiplexed by the GPIO.

Table 4-4. GPIO Controller Function Multiplexing

TFBGA 144	QFP 144	VFBGA 100	Pin	GPIO Pin	Function A	Function B	Function C	Function D
G11	122	G8[1]	PA00	GPIO 0	USART0 - RTS	TC0 - CLK1	SPI1 - NPCS[3]	
G12	123	G10[1]	PA01	GPIO 1	USART0 - CTS	TC0 - A1	USART2 - RTS	
D8	15	E1[1]	PA02	GPIO 2	USART0 - CLK	TC0 - B1	SPI0 - NPCS[0]	
G10	125	F9	PA03	GPIO 3	USART0 - RXD	EIC - EXTINT[4]	ABDAC - DATA[0]	
F9	126	E9	PA04	GPIO 4	USART0 - TXD	EIC - EXTINT[5]	ABDAC - DATAN[0]	
F10	124	G9	PA05	GPIO 5	USART1 - RXD	TC1 - CLK0	USB - ID	
F8	127	E8[1]	PA06	GPIO 6	USART1 - TXD	TC1 - CLK1	USB - VBOF	
E10	133	H10[1]	PA07	GPIO 7	SPI0 - NPCS[3]	ABDAC - DATAN[0]	USART1 - CLK	
C11	137	F8	PA08	GPIO 8	SPI0 - SPCK	ABDAC - DATA[0]	TC1 - B1	
B12	139	D8	PA09	GPIO 9	SPI0 - NPCS[0]	EIC - EXTINT[6]	TC1 - A1	
C12	138	C10	PA10	GPIO 10	SPI0 - MOSI	USB - VBOF	TC1 - B0	
D10	136	C9	PA11	GPIO 11	SPI0 - MISO	USB - ID	TC1 - A2	
E12	132	G7[1]	PA12	GPIO 12	USART1 - CTS	SPI0 - NPCS[2]	TC1 - A0	
F11	129	E8[1]	PA13	GPIO 13	USART1 - RTS	SPI0 - NPCS[1]	EIC - EXTINT[7]	
J6	100	K7[1]	PA14	GPIO 14	SPI0 - NPCS[1]	TWIMS0 - TWALM	TWIMS1 - TWCK	
J7	101	J7[1]	PA15	GPIO 15	MCI - CMD[1]	SPI1 - SPCK	TWIMS1 - TWD	
F12	128	E7	PA16	GPIO 16	MCI - DATA[11]	SPI1 - MOSI	TC1 - CLK2	
H7	116	G10[1]	PA17	GPIO 17	MCI - DATA[10]	SPI1 - NPCS[1]	ADC - AD[7]	
K8	115	G8[1]	PA18	GPIO 18	MCI - DATA[9]	SPI1 - NPCS[2]	ADC - AD[6]	
J8	114	H10[1]	PA19	GPIO 19	MCI - DATA[8]	SPI1 - MISO	ADC - AD[5]	
J9	113	H9[1]	PA20	GPIO 20	EIC - NMI	SSC - RX_FRAME_SYNC	ADC - AD[4]	
H9	109	K10[1]	PA21	GPIO 21	ADC - AD[0]	EIC - EXTINT[0]	USB - ID	
H10	110	H6[1]	PA22	GPIO 22	ADC - AD[1]	EIC - EXTINT[1]	USB - VBOF	
G8	111	G6[1]	PA23	GPIO 23	ADC - AD[2]	EIC - EXTINT[2]	ABDAC - DATA[1]	
G9	112	J10[1]	PA24	GPIO 24	ADC - AD[3]	EIC - EXTINT[3]	ABDAC - DATAN[1]	
E9	119	G7[1]	PA25	GPIO 25	TWIMS0 - TWD	TWIMS1 - TWALM	USART1 - DCD	
D9	120	F7[1])	PA26	GPIO 26	TWIMS0 - TWCK	USART2 - CTS	USART1 - DSR	
A4	26	A2	PA27	GPIO 27	MCI - CLK	SSC - RX_DATA	USART3 - RTS	MSI - SCLK
A3	28	A1	PA28	GPIO 28	MCI - CMD[0]	SSC - RX_CLOCK	USART3 - CTS	MSI - BS
A6	23	B4	PA29	GPIO 29	MCI - DATA[0]	USART3 - TXD	TC0 - CLK0	MSI - DATA[0]
C7	14	A4	PA30	GPIO 30	MCI - DATA[1]	USART3 - CLK	DMACA - DMAACK[0]	MSI - DATA[1]
B3	29	C2	PA31	GPIO 31	MCI - DATA[2]	USART2 - RXD	DMACA - DMARQ[0]	MSI - DATA[2]
A2	30	B1	PB00	GPIO 32	MCI - DATA[3]	USART2 - TXD	ADC - TRIGGER	MSI - DATA[3]
C4	27	B2	PB01	GPIO 33	MCI - DATA[4]	ABDAC - DATA[1]	EIC - SCAN[0]	MSI - INS

Table 4-4. GPIO Controller Function Multiplexing

B4	25	B3	PB02	GPIO 34	MCI - DATA[5]	ABDAC - DATAN[1]	EIC - SCAN[1]	
A5	24	C4	PB03	GPIO 35	MCI - DATA[6]	USART2 - CLK	EIC - SCAN[2]	
B6	22	A3	PB04	GPIO 36	MCI - DATA[7]	USART3 - RXD	EIC - SCAN[3]	
H12	121	F7(1)	PB05	GPIO 37	USB - ID	TC0 - A0	EIC - SCAN[4]	
D12	134	D7	PB06	GPIO 38	USB - VBOF	TC0 - B0	EIC - SCAN[5]	
D11	135	D6	PB07	GPIO 39	SPI1 - SPCK	SSC - TX_CLOCK	EIC - SCAN[6]	
C8	11	C6	PB08	GPIO 40	SPI1 - MISO	SSC - TX_DATA	EIC - SCAN[7]	
E7	17	C5	PB09	GPIO 41	SPI1 - NPCS[0]	SSC - RX_DATA	EBI - NCS[4]	
D7	16	D5	PB10	GPIO 42	SPI1 - MOSI	SSC - RX_FRAME_SYNC	EBI - NCS[5]	
B2	31	C1	PB11	GPIO 43	USART1 - RXD	SSC - TX_FRAME_SYNC	PM - GCLK[1]	
K5	98	K5(1)	PC00	GPIO 45				
H6	99	K6	PC01	GPIO 46				
A7	18	A5	PC02	GPIO 47				
B7	19	A6	PC03	GPIO 48				
A8	13	B7	PC04	GPIO 49				
A9	12	A7	PC05	GPIO 50				
G1	55	G4	PX00	GPIO 51	EBI - DATA[10]	USART0 - RXD	USART1 - RI	
H1	59	G2	PX01	GPIO 52	EBI - DATA[9]	USART0 - TXD	USART1 - DTR	
J2	62	G3	PX02	GPIO 53	EBI - DATA[8]	USART0 - CTS	PM - GCLK[0]	
K1	63	J1	PX03	GPIO 54	EBI - DATA[7]	USART0 - RTS		
J1	60	H1	PX04	GPIO 55	EBI - DATA[6]	USART1 - RXD		
G2	58	G1	PX05	GPIO 56	EBI - DATA[5]	USART1 - TXD		
F3	53	F3	PX06	GPIO 57	EBI - DATA[4]	USART1 - CTS		
F2	54	F4	PX07	GPIO 58	EBI - DATA[3]	USART1 - RTS		
D1	50	E3	PX08	GPIO 59	EBI - DATA[2]	USART3 - RXD		
C1	49	E4	PX09	GPIO 60	EBI - DATA[1]	USART3 - TXD		
B1	37	D2	PX10	GPIO 61	EBI - DATA[0]	USART2 - RXD		
L1	67	K7(1)	PX11	GPIO 62	EBI - NWE1	USART2 - TXD		
D6	34	D1	PX12	GPIO 63	EBI - NWE0	USART2 - CTS	MCI - CLK	
C6	33	D3	PX13	GPIO 64	EBI - NRD	USART2 - RTS	MCI - CLK	
M4	68	K5(1)	PX14	GPIO 65	EBI - NCS[1]		TC0 - A0	
E6	40	K4(1)	PX15	GPIO 66	EBI - ADDR[19]	USART3 - RTS	TC0 - B0	
C5	32	D4(1)	PX16	GPIO 67	EBI - ADDR[18]	USART3 - CTS	TC0 - A1	
K6	83	J10(1)	PX17	GPIO 68	EBI - ADDR[17]	DMACA - DMARQ[1]	TC0 - B1	
L6	84	H9(1)	PX18	GPIO 69	EBI - ADDR[16]	DMACA - DMAACK[1]	TC0 - A2	
D5	35	F1(1)	PX19	GPIO 70	EBI - ADDR[15]	EIC - SCAN[0]	TC0 - B2	
L4	73	H6(1)	PX20	GPIO 71	EBI - ADDR[14]	EIC - SCAN[1]	TC0 - CLK0	
M5	80	H2	PX21	GPIO 72	EBI - ADDR[13]	EIC - SCAN[2]	TC0 - CLK1	
M1	72	K10(1)	PX22	GPIO 73	EBI - ADDR[12]	EIC - SCAN[3]	TC0 - CLK2	

Table 4-4. GPIO Controller Function Multiplexing

M6	85	K1	PX23	GPIO 74	EBI - ADDR[11]	EIC - SCAN[4]	SSC - TX_CLOCK	
M7	86	J2	PX24	GPIO 75	EBI - ADDR[10]	EIC - SCAN[5]	SSC - TX_DATA	
M8	92	H4	PX25	GPIO 76	EBI - ADDR[9]	EIC - SCAN[6]	SSC - RX_DATA	
L9	90	J3	PX26	GPIO 77	EBI - ADDR[8]	EIC - SCAN[7]	SSC - RX_FRAME_SYNC	
K9	89	K2	PX27	GPIO 78	EBI - ADDR[7]	SPI0 - MISO	SSC - TX_FRAME_SYNC	
L10	91	K3	PX28	GPIO 79	EBI - ADDR[6]	SPI0 - MOSI	SSC - RX_CLOCK	
K11	94	J4	PX29	GPIO 80	EBI - ADDR[5]	SPI0 - SPCK		
M11	96	G5	PX30	GPIO 81	EBI - ADDR[4]	SPI0 - NPCS[0]		
M10	97	H5	PX31	GPIO 82	EBI - ADDR[3]	SPI0 - NPCS[1]		
M9	93	K4(1)	PX32	GPIO 83	EBI - ADDR[2]	SPI0 - NPCS[2]		
M12	95		PX33	GPIO 84	EBI - ADDR[1]	SPI0 - NPCS[3]		
J3	61		PX34	GPIO 85	EBI - ADDR[0]	SPI1 - MISO	PM - GCLK[0]	
C2	38		PX35	GPIO 86	EBI - DATA[15]	SPI1 - MOSI	PM - GCLK[1]	
D3	44		PX36	GPIO 87	EBI - DATA[14]	SPI1 - SPCK	PM - GCLK[2]	
D2	45		PX37	GPIO 88	EBI - DATA[13]	SPI1 - NPCS[0]	PM - GCLK[3]	
E1	51		PX38	GPIO 89	EBI - DATA[12]	SPI1 - NPCS[1]	USART1 - DCD	
F1	52		PX39	GPIO 90	EBI - DATA[11]	SPI1 - NPCS[2]	USART1 - DSR	
A1	36		PX40	GPIO 91		MCI - CLK		
M2	71		PX41	GPIO 92	EBI - CAS			
M3	69		PX42	GPIO 93	EBI - RAS			
L7	88		PX43	GPIO 94	EBI - SDA10	USART1 - RI		
K2	66		PX44	GPIO 95	EBI - SDWE	USART1 - DTR		
L3	70	J7(1)	PX45	GPIO 96	EBI - SDCK			
K4	74	G6(1)	PX46	GPIO 97	EBI - SDCKE			
D4	39	E1(1)	PX47	GPIO 98	EBI - NANDOE	ADC - TRIGGER	MCI - DATA[11]	
F5	41		PX48	GPIO 99	EBI - ADDR[23]	USB - VBOF	MCI - DATA[10]	
F4	43		PX49	GPIO 100	EBI - CFRNW	USB - ID	MCI - DATA[9]	
G4	75		PX50	GPIO 101	EBI - CFCE2	TC1 - B2	MCI - DATA[8]	
G5	77		PX51	GPIO 102	EBI - CFCE1	DMACA - DMAACK[0]	MCI - DATA[15]	
K7	87		PX52	GPIO 103	EBI - NCS[3]	DMACA - DMARQ[0]	MCI - DATA[14]	
E4	42	D4(1)	PX53	GPIO 104	EBI - NCS[2]		MCI - DATA[13]	
E3	46		PX54	GPIO 105	EBI - NWAIT	USART3 - TXD	MCI - DATA[12]	
J5	79		PX55	GPIO 106	EBI - ADDR[22]	EIC - SCAN[3]	USART2 - RXD	
J4	78		PX56	GPIO 107	EBI - ADDR[21]	EIC - SCAN[2]	USART2 - TXD	
H4	76		PX57	GPIO 108	EBI - ADDR[20]	EIC - SCAN[1]	USART3 - RXD	
H3	57		PX58	GPIO 109	EBI - NCS[0]	EIC - SCAN[0]	USART3 - TXD	
G3	56	F1(1)	PX59	GPIO 110	EBI - NANDWE		MCI - CMD[1]	

Note: 1. Those balls are physically connected to 2 GPIOs. Software must managed carrefully the GPIO configuration to avoid electrical conflict

4.2.1 Oscillator Pinout

Table 4-5. Oscillator Pinout

TFBGA144	QFP144	VFBGA100	Pin name	Oscillator pin
A7	18	A5	PC02	XIN0
B7	19	A6	PC03	XOUT0
A8	13	B7	PC04	XIN1
A9	12	A7	PC05	XIN1
K5	98	K5(1)	PC00	XIN32
H6	99	K6	PC01	XOUT32

Note: 1. This ball is physically connected to 2 GPIOs. Software must managed carrefully the GPIO configuration to avoid electrical conflict

4.2.2 JTAG port connections

Table 4-6. JTAG Pinout

TFBGA144	QFP144	VFBGA100	Pin name	JTAG pin
K12	107	K9	TCK	TCK
L12	108	K8	TDI	TDI
J11	105	J8	TDO	TDO
J10	104	H7	TMS	TMS

4.2.3 Nexus OCD AUX port connections

If the OCD trace system is enabled, the trace system will take control over a number of pins, irrespective of the GPIO configuration. Three differents OCD trace pin mappings are possible, depending on the configuration of the OCD AXS register. For details, see the AVR32 UC Technical Reference Manual.

Table 4-7. Nexus OCD AUX port connections

Pin	AXS=0	AXS=1	AXS=2
EVTI_N	PB05	PA08	PX00
MDO[5]	PA00	PX56	PX06
MDO[4]	PA01	PX57	PX05
MDO[3]	PA03	PX58	PX04
MDO[2]	PA16	PA24	PX03
MDO[1]	PA13	PA23	PX02
MDO[0]	PA12	PA22	PX01
MSEO[1]	PA10	PA07	PX08
MSEO[0]	PA11	PX55	PX07
MCKO	PB07	PX00	PB09
EVTO_N	PB06	PB06	PB06

4.3 Signal Descriptions

The following table gives details on signal name classified by peripheral.

Table 4-8. Signal Description List

Signal Name	Function	Type	Active Level	Comments
Power				
VDDIO	I/O Power Supply	Power		3.0 to 3.6V
VDDANA	Analog Power Supply	Power		3.0 to 3.6V
VDDIN	Voltage Regulator Input Supply	Power		3.0 to 3.6V
VDDCORE	Voltage Regulator Output for Digital Supply	Power Output		1.65 to 1.95 V
GNDANA	Analog Ground	Ground		
GNDIO	I/O Ground	Ground		
GNDCORE	Digital Ground	Ground		
GNDPLL	PLL Ground	Ground		
Clocks, Oscillators, and PLL's				
XIN0, XIN1, XIN32	Crystal 0, 1, 32 Input	Analog		
XOUT0, XOUT1, XOUT32	Crystal 0, 1, 32 Output	Analog		
JTAG				
TCK	Test Clock	Input		
TDI	Test Data In	Input		
TDO	Test Data Out	Output		
TMS	Test Mode Select	Input		
Auxiliary Port - AUX				
MCKO	Trace Data Output Clock	Output		
MDO[5:0]	Trace Data Output	Output		
MSEO[1:0]	Trace Frame Control	Output		
EVTI_N	Event In	Output	Low	
EVTO_N	Event Out	Output	Low	
Power Manager - PM				
GCLK[3:0]	Generic Clock Pins	Output		

Table 4-8. Signal Description List

Signal Name	Function	Type	Active Level	Comments
RESET_N	Reset Pin	Input	Low	
DMA Controller - DMACA (optional)				
DMAACK[1:0]	DMA Acknowledge	Output		
DMARQ[1:0]	DMA Requests	Input		
External Interrupt Controller - EIC				
EXTINT[7:0]	External Interrupt Pins	Input		
SCAN[7:0]	Keypad Scan Pins	Output		
NMI	Non-Maskable Interrupt Pin	Input	Low	
General Purpose Input/Output pin - GPIOA, GPIOB, GPIOC, GPIOX				
PA[31:0]	Parallel I/O Controller GPIO port A	I/O		
PB[11:0]	Parallel I/O Controller GPIO port B	I/O		
PC[5:0]	Parallel I/O Controller GPIO port C	I/O		
PX[59:0]	Parallel I/O Controller GPIO port X	I/O		
External Bus Interface - EBI				
ADDR[23:0]	Address Bus	Output		
CAS	Column Signal	Output	Low	
CFCE1	Compact Flash 1 Chip Enable	Output	Low	
CFCE2	Compact Flash 2 Chip Enable	Output	Low	
CFRNW	Compact Flash Read Not Write	Output		
DATA[15:0]	Data Bus	I/O		
NANDOE	NAND Flash Output Enable	Output	Low	
NANDWE	NAND Flash Write Enable	Output	Low	
NCS[5:0]	Chip Select	Output	Low	
NRD	Read Signal	Output	Low	
NWAIT	External Wait Signal	Input	Low	
NWE0	Write Enable 0	Output	Low	
NWE1	Write Enable 1	Output	Low	
RAS	Row Signal	Output	Low	

Table 4-8. Signal Description List

Signal Name	Function	Type	Active Level	Comments
SDA10	SDRAM Address 10 Line	Output		
SDCK	SDRAM Clock	Output		
SDCKE	SDRAM Clock Enable	Output		
SDWE	SDRAM Write Enable	Output	Low	
MultiMedia Card Interface - MCI				
CLK	Multimedia Card Clock	Output		
CMD[1:0]	Multimedia Card Command	I/O		
DATA[15:0]	Multimedia Card Data	I/O		
Memory Stick Interface - MSI				
SCLK	Memory Stick Clock	Output		
BS	Memory Stick Command	I/O		
DATA[3:0]	Multimedia Card Data	I/O		
Serial Peripheral Interface - SPI0, SPI1				
MISO	Master In Slave Out	I/O		
MOSI	Master Out Slave In	I/O		
NPCS[3:0]	SPI Peripheral Chip Select	I/O	Low	
SPCK	Clock	Output		
Synchronous Serial Controller - SSC				
RX_CLOCK	SSC Receive Clock	I/O		
RX_DATA	SSC Receive Data	Input		
RX_FRAME_SYNC	SSC Receive Frame Sync	I/O		
TX_CLOCK	SSC Transmit Clock	I/O		
TX_DATA	SSC Transmit Data	Output		
TX_FRAME_SYNC	SSC Transmit Frame Sync	I/O		
Timer/Counter - TC0, TC1				
A0	Channel 0 Line A	I/O		
A1	Channel 1 Line A	I/O		
A2	Channel 2 Line A	I/O		

Table 4-8. Signal Description List

Signal Name	Function	Type	Active Level	Comments
B0	Channel 0 Line B	I/O		
B1	Channel 1 Line B	I/O		
B2	Channel 2 Line B	I/O		
CLK0	Channel 0 External Clock Input	Input		
CLK1	Channel 1 External Clock Input	Input		
CLK2	Channel 2 External Clock Input	Input		
Two-wire Interface - TWI0, TWI1				
TWCK	Serial Clock	I/O		
TWD	Serial Data	I/O		
TWALM	SMBALERT signal	I/O		
Universal Synchronous Asynchronous Receiver Transmitter - USART0, USART1, USART2, USART3				
CLK	Clock	I/O		
CTS	Clear To Send	Input		
DCD	Data Carrier Detect			Only USART1
DSR	Data Set Ready			Only USART1
DTR	Data Terminal Ready			Only USART1
RI	Ring Indicator			Only USART1
RTS	Request To Send	Output		
RXD	Receive Data	Input		
TXD	Transmit Data	Output		
Analog to Digital Converter - ADC				
AD0 - AD7	Analog input pins	Analog input		
Audio Bitstream DAC (ABDAC)				
DATA0-DATA1	D/A Data out	Output		
DATAN0-DATAN1	D/A Data inverted out	Output		
Universal Serial Bus Device - USB				
DMFS	USB Full Speed Data -	Analog		
DPFS	USB Full Speed Data +	Analog		

Table 4-8. Signal Description List

Signal Name	Function	Type	Active Level	Comments
DMHS	USB High Speed Data -	Analog		
DPHS	USB High Speed Data +	Analog		
USB_VBIAS	USB VBIAS reference	Analog		Connect to the ground through a 6810 ohms (+/- 1%) resistor in parallel with a 10pf capacitor. If USB hi-speed feature is not required, leave this pin unconnected to save power
USB_VBUS	USB VBUS for OTG feature	Output		
VBOF	USB VBUS on/off bus power control port	Output		
ID	ID Pin fo the USB bus	Input		

4.4 I/O Line Considerations

4.4.1 JTAG Pins

TMS and TDI pins have pull-up resistors. TDO pin is an output, driven at up to VDDIO, and has no pull-up resistor.

4.4.2 RESET_N Pin

The RESET_N pin is a schmitt input and integrates a permanent pull-up resistor to VDDIO. As the product integrates a power-on reset cell, the RESET_N pin can be left unconnected in case no reset from the system needs to be applied to the product.

4.4.3 TWI Pins

When these pins are used for TWI, the pins are open-drain outputs with slew-rate limitation and inputs with inputs with spike filtering. When used as GPIO pins or used for other peripherals, the pins have the same characteristics as other GPIO pins.

4.4.4 GPIO Pins

All the I/O lines integrate a programmable pull-up resistor. Programming of this pull-up resistor is performed independently for each I/O line through the I/O Controller. After reset, I/O lines default as inputs with pull-up resistors disabled, except when indicated otherwise in the column “Reset State” of the I/O Controller multiplexing tables.

4.5 Power Considerations

4.5.1 Power Supplies

The AT32UC3A3 has several types of power supply pins:

- **VDDIO: Powers I/O lines. Voltage is 3.3V nominal**
- **VDDANA: Powers the ADC. Voltage is 3.3V nominal**
- **VDDIN: Input voltage for the voltage regulator. Voltage is 3.3V nominal**
- **VDDCORE: Output voltage from regulator for filtering purpose and provides the supply to the core, memories, and peripherals. Voltage is 1.8V nominal**

The ground pin GNDCORE is common to VDDCORE and VDDIN. The ground pin for VDDANA is GNDANA. The ground pins for VDDIO are GNDIO.

Refer to Electrical Characteristics chapter for power consumption on the various supply pins.

4.5.2 Voltage Regulator

The AT32UC3A3 embeds a voltage regulator that converts from 3.3V to 1.8V with a load of up to 100 mA. The regulator takes its input voltage from VDDIN, and supplies the output voltage on VDDCORE and powers the core, memories and peripherals.

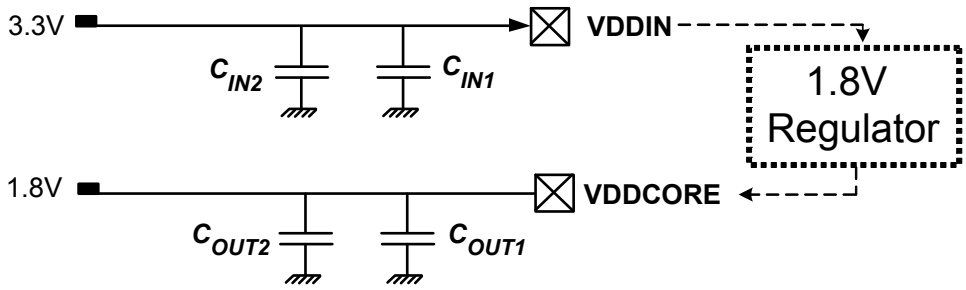
Adequate output supply decoupling is mandatory for VDDCORE to reduce ripple and avoid oscillations.

The best way to achieve this is to use two capacitors in parallel between VDDCORE and GNDCORE:

- One external 470 pF (or 1 nF) NPO capacitor (C_{OUT1}) should be connected as close to the chip as possible.
- One external 2.2 µF (or 3.3 µF) X7R capacitor (C_{OUT2}).

Adequate input supply decoupling is mandatory for VDDIN in order to improve startup stability and reduce source voltage drop.

The input decoupling capacitor should be placed close to the chip, e.g., two capacitors can be used in parallel (1 nF NPO and 4.7 µF X7R).



5. Power Considerations

5.1 Power Supplies

The AT32UC3A3/A4 has several types of power supply pins:

- **VDDIO: Powers I/O lines. Voltage is 3.3V nominal**
- **VDDANA: Powers the ADC Voltage and provides the ADVREF voltage is 3.3V nominal**
- **VDDIN: Input voltage for the voltage regulator. Voltage is 3.3V nominal**
- **VDDCORE: Output voltage from regulator for filtering purpose and provides the supply to the core, memories, and peripherals. Voltage is 1.8V nominal**

The ground pins GNDCORE are common to VDDCORE and VDDIN. The ground pin for VDDANA is GNDANA. The ground pin for VDDIO is GNDIO

Refer to Electrical Characteristics chapter for power consumption on the various supply pins.

5.2 Voltage Regulator

The AT32UC3A3 embeds a voltage regulator that converts from 3.3V to 1.8V with a load of up to 100 mA. The regulator takes its input voltage from VDDIN, and supplies the output voltage on VDDCORE and powers the core, memories and peripherals.

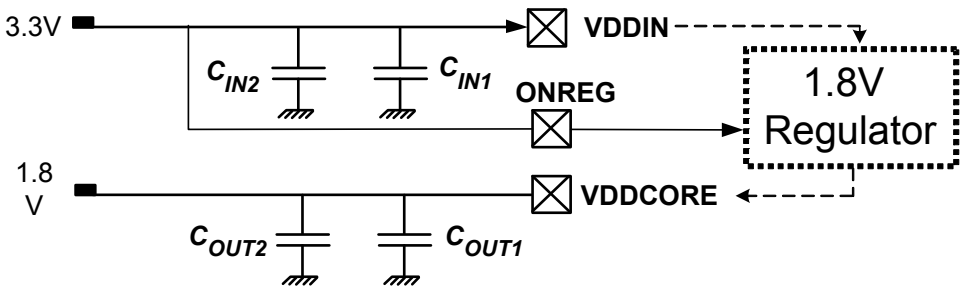
Adequate output supply decoupling is mandatory for VDDCORE to reduce ripple and avoid oscillations.

The best way to achieve this is to use two capacitors in parallel between VDDCORE and GNDCORE:

- One external 470 pF (or 1 nF) NPO capacitor (C_{OUT1}) should be connected as close to the chip as possible.
- One external 2.2 µF (or 3.3 µF) X7R capacitor (C_{OUT2}).

Adequate input supply decoupling is mandatory for VDDIN in order to improve startup stability and reduce source voltage drop.

The input decoupling capacitor should be placed close to the chip, e.g., two capacitors can be used in parallel (100 nF NPO and 4.7 µF X7R).



ONREG input must be tied to VDDIN.

6. I/O Line Considerations

6.1 JTAG Pins

TMS and TDI pins have pull-up resistors. TDO pin is an output, driven at up to VDDIO, and has no pull-up resistor.

6.2 RESET_N Pin

The RESET_N pin is a schmitt input and integrates a permanent pull-up resistor to VDDIO. As the product integrates a power-on reset cell, the RESET_N pin can be left unconnected in case no reset from the system needs to be applied to the product.

6.3 TWI Pins

When these pins are used for TWI, the pins are open-drain outputs with slew-rate limitation and inputs with inputs with spike filtering. When used as GPIO pins or used for other peripherals, the pins have the same characteristics as other GPIO pins.

6.4 GPIO Pins

All the I/O lines integrate a programmable pull-up resistor. Programming of this pull-up resistor is performed independently for each I/O line through the I/O Controller. After reset, I/O lines default as inputs with pull-up resistors disabled, except when indicated otherwise in the column “Reset State” of the I/O Controller multiplexing tables.

7. Memories

7.1 Embedded Memories

- **Internal High-Speed Flash**
  - **256KBytes (AT32UC3A3256/S)**
  - **128Kbytes (AT32UC3A3128/S)**
  - **64Kbytes (AT32UC3A364/S)**
    - **0 wait state access at up to 36MHz in worst case conditions**
    - **1 wait state access at up to 66MHz in worst case conditions**
    - **Pipelined Flash architecture, allowing burst reads from sequential Flash locations, hiding penalty of 1 wait state access**
    - **Pipelined Flash architecture typically reduces the cycle penalty of 1 wait state operation to only 15% compared to 0 wait state operation**
    - **100 000 write cycles, 15-year data retention capability**
    - **Sector lock capabilities, Bootloader protection, Security Bit**
    - **32 fuses, preserved during Chip Erase**
    - **User page for data to be preserved during Chip Erase**
- **Internal High-Speed SRAM**
  - **64KBytes, Single-cycle access at full speed on CPU Local Bus and accessible through the High Speed Bud (HSB) matrix**
  - **2x32KBytes, accessible independently through the High Speed Bud (HSB) matrix**

7.2 Physical Memory Map

The System Bus is implemented as a bus matrix. All system bus addresses are fixed, and they are never remapped in any way, not even in boot.

Note that AVR32 UC CPU uses unsegmented translation, as described in the AVR32UC Technical Architecture Manual.

The 32-bit physical address space is mapped as follows:

Table 7-1. AT32UC3A3A4 Physical Memory Map

Device	Start Address	Size AT32UC3A3256S AT32UC3A3256 AT32UC3A4256S AT32UC3A4256	Size AT32UC3A3128S AT32UC3A3128 AT32UC3A4128S AT32UC3A4128	Size AT32UC3A364S AT32UC3A364 AT32UC3A464S AT32UC3A464
Embedded CPU SRAM	0x00000000	64KByte	64KByte	64KByte
Embedded Flash	0x80000000	256KByte	128KByte	64KByte
EBI SRAM CS0	0xC0000000	16MByte	16MByte	16MByte
EBI SRAM CS2	0xC8000000	16MByte	16MByte	16MByte
EBI SRAM CS3	0xCC000000	16MByte	16MByte	16MByte
EBI SRAM CS4	0xD8000000	16MByte	16MByte	16MByte
EBI SRAM CS5	0xDC000000	16MByte	16MByte	16MByte
EBI SRAM CS1 /SDRAM CS0	0xD0000000	128MByte	128MByte	128MByte
USB Data	0xE0000000	64KByte	64KByte	64KByte

Table 7-1. AT32UC3A3A4 Physical Memory Map

Device	Start Address	Size AT32UC3A3256S AT32UC3A3256 AT32UC3A4256S AT32UC3A4256	Size AT32UC3A3128S AT32UC3A3128 AT32UC3A4128S AT32UC3A4128	Size AT32UC3A364S AT32UC3A364 AT32UC3A464S AT32UC3A464
HRAMC0	0xFF000000	32KByte	32KByte	32KByte
HRAMC1	0xFF008000	32KByte	32KByte	32KByte
HSB-PB Bridge A	0xFFFF0000	64KByte	64KByte	64KByte
HSB-PB Bridge B	0xFFFE0000	64KByte	64KByte	64KByte

7.3 Peripheral Address Map

Table 7-2. Peripheral Address Mapping

Address		Peripheral Name
0xFF100000	DMACA	DMA Controller - DMACA
0xFFFD0000	AES	Advanced Encryption Standard - AES
0xFFFE0000	USB	USB 2.0 OTG Interface - USB
0xFFFE1000	HMATRIX	HSB Matrix - HMATRIX
0xFFFE1400	FLASHC	Flash Controller - FLASHC
0xFFFE1C00	SMC	Static Memory Controller - SMC
0xFFFE2000	SDRAMC	SDRAM Controller - SDRAMC
0xFFFE2400	ECCHRS	Error code corrector Hamming and Reed Solomon - ECCHRS
0xFFFE2800	BUSMON	Bus Monitor module - BUSMON
0xFFFE4000	MCI	Mulitmedia Card Interface - MCI
0xFFFE8000	MSI	Memory Stick Interface - MSI
0xFFFF0000	PDCA	Peripheral DMA Controller - PDCA
0xFFFF0800	INTC	Interrupt controller - INTC

Table 7-2. Peripheral Address Mapping

0xFFFF0C00	PM	Power Manager - PM
0xFFFF0D00	RTC	Real Time Counter - RTC
0xFFFF0D30	WDT	Watchdog Timer - WDT
0xFFFF0D80	EIC	External Interrupt Controller - EIC
0xFFFF1000	GPIO	General Purpose Input/Output Controller - GPIO
0xFFFF1400	USART0	Universal Synchronous/Asynchronous Receiver/Transmitter - USART0
0xFFFF1800	USART1	Universal Synchronous/Asynchronous Receiver/Transmitter - USART1
0xFFFF1C00	USART2	Universal Synchronous/Asynchronous Receiver/Transmitter - USART2
0xFFFF2000	USART3	Universal Synchronous/Asynchronous Receiver/Transmitter - USART3
0xFFFF2400	SPI0	Serial Peripheral Interface - SPI0
0xFFFF2800	SPI1	Serial Peripheral Interface - SPI1
0xFFFF2C00	TWIM0	Two-wire Master Interface - TWIM0
0xFFFF3000	TWIM1	Two-wire Master Interface - TWIM1
0xFFFF3400	SSC	Synchronous Serial Controller - SSC
0xFFFF3800	TC0	Timer/Counter - TC0
0xFFFF3C00	ADC	Analog to Digital Converter - ADC
0xFFFF4000	ABDAC	Audio Bitstream DAC - ABDAC
0xFFFF4400	TC1	Timer/Counter - TC1

Table 7-2. Peripheral Address Mapping

0xFFFF5000	TWIS0	Two-wire Slave Interface - TWIS0
0xFFFF5400	TWIS1	Two-wire Slave Interface - TWIS1

7.4 CPU Local Bus Mapping

Some of the registers in the GPIO module are mapped onto the CPU local bus, in addition to being mapped on the Peripheral Bus. These registers can therefore be reached both by accesses on the Peripheral Bus, and by accesses on the local bus.

Mapping these registers on the local bus allows cycle-deterministic toggling of GPIO pins since the CPU and GPIO are the only modules connected to this bus. Also, since the local bus runs at CPU speed, one write or read operation can be performed per clock cycle to the local bus-mapped GPIO registers.

The following GPIO registers are mapped on the local bus:

Table 7-3. Local Bus Mapped GPIO Registers

Port	Register	Mode	Local Bus Address	Access
0	Output Driver Enable Register (ODER)	WRITE	0x40000040	Write-only
		SET	0x40000044	Write-only
		CLEAR	0x40000048	Write-only
		TOGGLE	0x4000004C	Write-only
	Output Value Register (OVR)	WRITE	0x40000050	Write-only
		SET	0x40000054	Write-only
		CLEAR	0x40000058	Write-only
		TOGGLE	0x4000005C	Write-only
	Pin Value Register (PVR)	-	0x40000060	Read-only
1	Output Driver Enable Register (ODER)	WRITE	0x40000140	Write-only
		SET	0x40000144	Write-only
		CLEAR	0x40000148	Write-only
		TOGGLE	0x4000014C	Write-only
	Output Value Register (OVR)	WRITE	0x40000150	Write-only
		SET	0x40000154	Write-only
		CLEAR	0x40000158	Write-only
		TOGGLE	0x4000015C	Write-only
	Pin Value Register (PVR)	-	0x40000160	Read-only

Table 7-3. Local Bus Mapped GPIO Registers

Port	Register	Mode	Local Bus Address	Access
2	Output Driver Enable Register (ODER)	WRITE	0x40000240	Write-only
		SET	0x40000244	Write-only
		CLEAR	0x40000248	Write-only
		TOGGLE	0x4000024C	Write-only
	Output Value Register (OVR)	WRITE	0x40000250	Write-only
		SET	0x40000254	Write-only
		CLEAR	0x40000258	Write-only
		TOGGLE	0x4000025C	Write-only
	Pin Value Register (PVR)	-	0x40000260	Read-only
3	Output Driver Enable Register (ODER)	WRITE	0x40000340	Write-only
		SET	0x40000344	Write-only
		CLEAR	0x40000348	Write-only
		TOGGLE	0x4000034C	Write-only
	Output Value Register (OVR)	WRITE	0x40000350	Write-only
		SET	0x40000354	Write-only
		CLEAR	0x40000358	Write-only
		TOGGLE	0x4000035C	Write-only
	Pin Value Register (PVR)	-	0x40000360	Read-only

8. Peripherals

8.1 Clock Connections

8.1.1 Timer/Counters

Each Timer/Counter channel can independently select an internal or external clock source for its counter:

Table 8-1. Timer/Counter clock connections

Source	Name	Connection
Internal	TIMER_CLOCK1	32 KHz clock
	TIMER_CLOCK2	PBA Clock / 2
	TIMER_CLOCK3	PBA Clock / 8
	TIMER_CLOCK4	PBA Clock / 32
	TIMER_CLOCK5	PBA Clock / 128
External	XC0	See Table 8.2 on page 32
	XC1	
	XC2	

8.2 Peripheral Multiplexing on I/O lines

Each GPIO line can be assigned to one of 4 peripheral functions; A, B, C or D. The following table define how the I/O lines on the peripherals A, B, C or D are multiplexed by the GPIO.

Table 8-2. GPIO Controller Function Multiplexing

BGA144	QFP144	PIN	GPIO Pin	Function A	Function B	Function C	Function D
G11	122	PA00	GPIO 0	USART0 - RTS	TC0 - CLK1	SPI1 - NPCS[3]	
G12	123	PA01	GPIO 1	USART0 - CTS	TC0 - A1	USART2 - RTS	
D8	15	PA02	GPIO 2	USART0 - CLK	TC0 - B1	SPI0 - NPCS[0]	
G10	125	PA03	GPIO 3	USART0 - RXD	EIC - EXTINT[4]	DAC - DATA[0]	
F9	126	PA04	GPIO 4	USART0 - TXD	EIC - EXTINT[5]	DAC - DATAN[0]	
F10	124	PA05	GPIO 5	USART1 - RXD	TC1 - CLK0	USB - USB_ID	
F8	127	PA06	GPIO 6	USART1 - TXD	TC1 - CLK1	USB - USB_VBOF	
E10	133	PA07	GPIO 7	SPI0 - NPCS[3]	DAC - DATAN[0]	USART1 - CLK	
C11	137	PA08	GPIO 8	SPI0 - SCK	DAC - DATA[0]	TC1 - B1	
B12	139	PA09	GPIO 9	SPI0 - NPCS[0]	EIC - EXTINT[6]	TC1 - A1	
C12	138	PA10	GPIO 10	SPI0 - MOSI	USB - USB_VBOF	TC1 - B0	
D10	136	PA11	GPIO 11	SPI0 - MISO	USB - USB_ID	TC1 - A2	
E12	132	PA12	GPIO 12	USART1 - CTS	SPI0 - NPCS[2]	TC1 - A0	
F11	129	PA13	GPIO 13	USART1 - RTS	SPI0 - NPCS[1]	EIC - EXTINT[7]	

Table 8-2. GPIO Controller Function Multiplexing

J6	100	PA14	GPIO 14	SPI0 - NPCS[1]	TWIMS0 - TWALM	TWIMS1 - TWCK	
J7	101	PA15	GPIO 15	MCI - CMD[1]	SPI1 - SCK	TWIMS1 - TWD	
F12	128	PA16	GPIO 16	MCI - DATA[11]	SPI1 - MOSI	TC1 - CLK2	
H7	116	PA17	GPIO 17	MCI - DATA[10]	SPI1 - NPCS[1]	ADC - AD[7]	
K8	115	PA18	GPIO 18	MCI - DATA[9]	SPI1 - NPCS[2]	ADC - AD[6]	
J8	114	PA19	GPIO 19	MCI - DATA[8]	SPI1 - MISO	ADC - AD[5]	
J9	113	PA20	GPIO 20	NMI	SSC - RX_FRAME_SYNC	ADC - AD[4]	
H9	109	PA21	GPIO 21	ADC - AD[0]	EIC - EXTINT[0]	USB - USB_ID	
H10	110	PA22	GPIO 22	ADC - AD[1]	EIC - EXTINT[1]	USB - USB_VBOF	
G8	111	PA23	GPIO 23	ADC - AD[2]	EIC - EXTINT[2]	DAC - DATA[1]	
G9	112	PA24	GPIO 24	ADC - AD[3]	EIC - EXTINT[3]	DAC - DATAN[1]	
E9	119	PA25	GPIO 25	TWIMS0 - TWD	TWIMS1 - TWALM	USART1 - DCD	
D9	120	PA26	GPIO 26	TWIMS0 - TWCK	USART2 - CTS	USART1 - DSR	
A4	26	PA27	GPIO 27	MCI - CLK	SSC - RX_DATA	USART3 - RTS	MSI - SCLK
A3	28	PA28	GPIO 28	MCI - CMD[0]	SSC - RX_CLOCK	USART3 - CTS	MSI - BS
A6	23	PA29	GPIO 29	MCI - DATA[0]	USART3 - TXD	TC0 - CLK0	MSI - DATA[0]
C7	14	PA30	GPIO 30	MCI - DATA[1]	USART3 - CLK	DMACA - DMAACK[0]	MSI - DATA[1]
B3	29	PA31	GPIO 31	MCI - DATA[2]	USART2 - RXD	DMACA - DMARQ[0]	MSI - DATA[2]
A2	30	PB00	GPIO 32	MCI - DATA[3]	USART2 - TXD	ADC - TRIGGER	MSI - DATA[3]
C4	27	PB01	GPIO 33	MCI - DATA[4]	DAC - DATA[1]	EIC - SCAN[0]	MSI - INS
B4	25	PB02	GPIO 34	MCI - DATA[5]	DAC - DATAN[1]	EIC - SCAN[1]	
A5	24	PB03	GPIO 35	MCI - DATA[6]	USART2 - CLK	EIC - SCAN[2]	
B6	22	PB04	GPIO 36	MCI - DATA[7]	USART3 - RXD	EIC - SCAN[3]	
H12	121	PB05	GPIO 37	USB - USB_ID	TC0 - A0	EIC - SCAN[4]	
D12	134	PB06	GPIO 38	USB - USB_VBOF	TC0 - B0	EIC - SCAN[5]	
D11	135	PB07	GPIO 39	SPI1 - SCK	SSC - TX_CLOCK	EIC - SCAN[6]	
C8	11	PB08	GPIO 40	SPI1 - MISO	SSC - TX_DATA	EIC - SCAN[7]	
E7	17	PB09	GPIO 41	SPI1 - NPCS[0]	SSC - RX_DATA	EBI - NCS[4]	
D7	16	PB10	GPIO 42	SPI1 - MOSI	SSC - RX_FRAME_SYNC	EBI - NCS[5]	
B2	31	PB11	GPIO 43	USART1 - RXD	SSC - TX_FRAME_SYNC	PM - GCLK[1]	
K5	98	PC00	GPIO 45				

Table 8-2. GPIO Controller Function Multiplexing

H6	99	PC01	GPIO 46				
A7	18	PC02	GPIO 47				
B7	19	PC03	GPIO 48				
A8	13	PC04	GPIO 49				
A9	12	PC05	GPIO 50				
G1	55	PX00	GPIO 51	EBI - DATA[10]	USART0 - RXD	USART1 - RI	
H1	59	PX01	GPIO 52	EBI - DATA[9]	USART0 - TXD	USART1 - DTR	
J2	62	PX02	GPIO 53	EBI - DATA[8]	USART0 - CTS	PM - GCLK[0]	
K1	63	PX03	GPIO 54	EBI - DATA[7]	USART0 - RTS		
J1	60	PX04	GPIO 55	EBI - DATA[6]	USART1 - RXD		
G2	58	PX05	GPIO 56	EBI - DATA[5]	USART1 - TXD		
F3	53	PX06	GPIO 57	EBI - DATA[4]	USART1 - CTS		
F2	54	PX07	GPIO 58	EBI - DATA[3]	USART1 - RTS		
D1	50	PX08	GPIO 59	EBI - DATA[2]	USART3 - RXD		
C1	49	PX09	GPIO 60	EBI - DATA[1]	USART3 - TXD		
B1	37	PX10	GPIO 61	EBI - DATA[0]	USART2 - RXD		
L1	67	PX11	GPIO 62	EBI - NWE1	USART2 - TXD		
D6	34	PX12	GPIO 63	EBI - NWE0	USART2 - CTS		
C6	33	PX13	GPIO 64	EBI - NRD	USART2 - RTS		
M4	68	PX14	GPIO 65	EBI - NCS[1]		TC0 - A0	
E6	40	PX15	GPIO 66	EBI - ADDR[19]	USART3 - RTS	TC0 - B0	
C5	32	PX16	GPIO 67	EBI - ADDR[18]	USART3 - CTS	TC0 - A1	
K6	83	PX17	GPIO 68	EBI - ADDR[17]	DMACA - DMARQ[1]	TC0 - B1	
L6	84	PX18	GPIO 69	EBI - ADDR[16]	DMACA - DMAACK[1]	TC0 - A2	
D5	35	PX19	GPIO 70	EBI - ADDR[15]	EIC - SCAN[0]	TC0 - B2	
L4	73	PX20	GPIO 71	EBI - ADDR[14]	EIC - SCAN[1]	TC0 - CLK0	
M5	80	PX21	GPIO 72	EBI - ADDR[13]	EIC - SCAN[2]	TC0 - CLK1	
M1	72	PX22	GPIO 73	EBI - ADDR[12]	EIC - SCAN[3]	TC0 - CLK2	
M6	85	PX23	GPIO 74	EBI - ADDR[11]	EIC - SCAN[4]	SSC - TX_CLOCK	
M7	86	PX24	GPIO 75	EBI - ADDR[10]	EIC - SCAN[5]	SSC - TX_DATA	
M8	92	PX25	GPIO 76	EBI - ADDR[9]	EIC - SCAN[6]	SSC - RX_DATA	
L9	90	PX26	GPIO 77	EBI - ADDR[8]	EIC - SCAN[7]	SSC - RX_FRAME_SYNC	
K9	89	PX27	GPIO 78	EBI - ADDR[7]	SPI0 - MISO	SSC - TX_FRAME_SYNC	
L10	91	PX28	GPIO 79	EBI - ADDR[6]	SPI0 - MOSI	SSC - RX_CLOCK	

Table 8-2. GPIO Controller Function Multiplexing

K11	94	PX29	GPIO 80	EBI - ADDR[5]	SPI0 - SCK		
M11	96	PX30	GPIO 81	EBI - ADDR[4]	SPI0 - NPCS[0]		
M10	97	PX31	GPIO 82	EBI - ADDR[3]	SPI0 - NPCS[1]		
M9	93	PX32	GPIO 83	EBI - ADDR[2]	SPI0 - NPCS[2]		
M12	95	PX33	GPIO 84	EBI - ADDR[1]	SPI0 - NPCS[3]		
J3	61	PX34	GPIO 85	EBI - ADDR[0]	SPI1 - MISO	PM - GCLK[0]	
C2	38	PX35	GPIO 86	EBI - DATA[15]	SPI1 - MOSI	PM - GCLK[1]	
D3	44	PX36	GPIO 87	EBI - DATA[14]	SPI1 - SCK	PM - GCLK[2]	
D2	45	PX37	GPIO 88	EBI - DATA[13]	SPI1 - NPCS[0]	PM - GCLK[3]	
E1	51	PX38	GPIO 89	EBI - DATA[12]	SPI1 - NPCS[1]	USART1 - DCD	
F1	52	PX39	GPIO 90	EBI - DATA[11]	SPI1 - NPCS[2]	USART1 - DSR	
A1	36	PX40	GPIO 91	EBI - SDCS			
M2	71	PX41	GPIO 92	EBI - CAS			
M3	69	PX42	GPIO 93	EBI - RAS			
L7	88	PX43	GPIO 94	EBI - SDA10	USART1 - RI		
K2	66	PX44	GPIO 95	EBI - SDWE	USART1 - DTR		
L3	70	PX45	GPIO 96	EBI - SDCK			
K4	74	PX46	GPIO 97	EBI - SDCKE			
D4	39	PX47	GPIO 98	EBI - NANDOE	ADC - TRIGGER	MCI - DATA[11]	
F5	41	PX48	GPIO 99	EBI - ADDR[23]	USB - USB_VBOF	MCI - DATA[10]	
F4	43	PX49	GPIO 100	EBI - CFRNW	USB - USB_ID	MCI - DATA[9]	
G4	75	PX50	GPIO 101	EBI - CFCE2	TC1 - B2	MCI - DATA[8]	
G5	77	PX51	GPIO 102	EBI - CFCE1	DMACA - DMAACK[0]	MCI - DATA[15]	
K7	87	PX52	GPIO 103	EBI - NCS[3]	DMACA - DMARQ[0]	MCI - DATA[14]	
E4	42	PX53	GPIO 104	EBI - NCS[2]		MCI - DATA[13]	
E3	46	PX54	GPIO 105	EBI - NWAIT	USART3 - TXD	MCI - DATA[12]	
J5	79	PX55	GPIO 106	EBI - ADDR[22]	EIC - SCAN[3]	USART2 - RXD	
J4	78	PX56	GPIO 107	EBI - ADDR[21]	EIC - SCAN[2]	USART2 - TXD	
H4	76	PX57	GPIO 108	EBI - ADDR[20]	EIC - SCAN[1]	USART3 - RXD	
H3	57	PX58	GPIO 109	EBI - NCS[0]	EIC - SCAN[0]	USART3 - TXD	
G3	56	PX59	GPIO 110	EBI - NANDWE		MCI - CMD[1]	

8.3 Oscillator Pinout

Table 8-3. Oscillator Pinout

pin	pin	Pad	Oscillator pin
A7	18	PC02	xin0
A8	13	PC04	xin1

Table 8-3. Oscillator Pinout

K5	98	PC00	xin32
B7	19	PC03	xout0
A9	12	PC05	xout1
H6	99	PC01	xout32

8.4 Peripheral overview

8.4.1 Power Manager

- Controls integrated oscillators and PLLs
- Generates clocks and resets for digital logic
- Supports 2 crystal oscillators 0.4-20 MHz
- Supports 2 PLLs 40-240 MHz
- Supports 32 KHz ultra-low power oscillator
- Integrated low-power RC oscillator
- On-the fly frequency change of CPU, HSB, PBA, and PBB clocks
- Sleep modes allow simple disabling of logic clocks, PLLs, and oscillators
- Module-level clock gating through maskable peripheral clocks
- Wake-up from internal or external interrupts
- Generic clocks with wide frequency range provided
- Automatic identification of reset sources
- Controls brownout detector (BOD and BOD33), RC oscillator, and bandgap voltage reference through control and calibration registers

8.4.2 Real Time Counter

- 32-bit real-time counter with 16-bit prescaler
- Clocked from RC oscillator or 32 KHz oscillator
- Long delays
  - Max timeout 272 years
- High resolution: Max count frequency 16 KHz
- Extremely low power consumption
- Available in all sleep modes except Static
- Interrupt on wrap

8.4.3 Watchdog Timer

- Watchdog timer counter with 32-bit prescaler
- Clocked from the system RC oscillator (RCSYS)

8.4.4 Interrupt Controller

- Autovectored low latency interrupt service with programmable priority
  - 4 priority levels for regular, maskable interrupts
  - One Non-Maskable Interrupt

- Up to 64 groups of interrupts with up to 32 interrupt requests in each group

8.4.5 External Interrupts Controller

- Dedicated interrupt request for each interrupt
- Individually maskable interrupts
- Interrupt on rising or falling edge
- Interrupt on high or low level
- Asynchronous interrupts for sleep modes without clock
- Filtering of interrupt lines
- Maskable NMI interrupt
- Keypad scan support
-

8.4.6 Flash Controller

- Controls flash block with dual read ports allowing staggered reads.
- Supports 0 and 1 wait state bus access.
- Allows interleaved burst reads for systems with one wait state, outputting one 32-bit word per clock cycle.
- 32-bit HSB interface for reads from flash array and writes to page buffer.
- 32-bit PB interface for issuing commands to and configuration of the controller.
- 16 lock bits, each protecting a region consisting of (total number of pages in the flash block / 16) pages.
- Regions can be individually protected or unprotected.
- Additional protection of the Boot Loader pages.
- Supports reads and writes of general-purpose NVM bits.
- Supports reads and writes of additional NVM pages.
- Supports device protection through a security bit.
- Dedicated command for chip-erase, first erasing all on-chip volatile memories before erasing flash and clearing security bit.
- Interface to Power Manager for power-down of flash-blocks in sleep mode.

8.4.7 HSB Bus Matrix

- User Interface on peripheral bus
- Configurable Number of Masters (Up to sixteen)
- Configurable Number of Slaves (Up to sixteen)
- One Decoder for Each Master
- Three Different Memory Mappings for Each Master (Internal and External boot, Remap)
- One Remap Function for Each Master
- Programmable Arbitration for Each Slave
  - Round-Robin
  - Fixed Priority
- Programmable Default Master for Each Slave
  - No Default Master
  - Last Accessed Default Master
  - Fixed Default Master

- One Cycle Latency for the First Access of a Burst
- Zero Cycle Latency for Default Master
- One Special Function Register for Each Slave (Not dedicated)

8.4.8 External Bus Interface

- Optimized for application memory space support
- Integrates three external memory controllers:
  - Static Memory Controller (SMC)
  - SDRAM Controller (SDRAMC)
  - Error Corrected Code (ECCHRS) controller
- Additional logic for NAND Flash/SmartMedia™ and CompactFlash™ support
  - NAND Flash support: 8-bit as well as 16-bit devices are supported
  - CompactFlash support: all modes (Attribute Memory, Common Memory, I/O, True IDE) are supported but the signals _IOIS16 (I/O and True IDE modes) and _ATA SEL (True IDE mode) are not handled.
- Optimized external bus:16-bit data bus
  - Up to 24-bit Address Bus, Up to 8-Mbytes Addressable
  - Optimized pin multiplexing to reduce latencies on external memories
- Up to 6 Chip Selects, Configurable Assignment:
  - Static Memory Controller on Chip Select 0
  - SDRAM Controller or Static Memory Controller on Chip Select 1
  - Static Memory Controller on Chip Select 2, Optional NAND Flash support
  - Static Memory Controller on Chip Select 3, Optional NAND Flash support
  - Static Memory Controller on Chip Select 4, Optional CompactFlash™ support
  - Static Memory Controller on Chip Select 5, Optional CompactFlash™ support

8.4.9 Static Memory Controller

- 6 chip selects available
- 16-Mbytes address space per chip select
- 8- or 16-bit data bus
- Word, halfword, byte transfers
- Byte write or byte select lines
- Programmable setup, pulse and hold time for read signals per chip select
- Programmable setup, pulse and hold time for write signals per chip select
- Programmable data float time per chip select
- Compliant with LCD module
- External wait request
- Automatic switch to slow clock mode
- Asynchronous read in page mode supported: page size ranges from 4 to 32 bytes

8.4.10 SDRAM Controller

- 128-Mbytes address space
- Numerous configurations supported
  - 2K, 4K, 8K row address memory parts
  - SDRAM with two or four internal banks
  - SDRAM with 16-bit data path
- Programming facilities
  - Word, halfword, byte access
  - Automatic page break when memory boundary has been reached
  - Multibank ping-pong access

  - Timing parameters specified by software
  - Automatic refresh operation, refresh rate is programmable
  - Automatic update of DS, TCR and PASR parameters (mobile SDRAM devices)
- Energy-saving capabilities
  - Self-refresh, power-down, and deep power-down modes supported
  - Supports mobile SDRAM devices
- Error detection
  - Refresh error interrupt
- SDRAM power-up initialization by software
- CAS latency of one, two, and three supported
- Auto Precharge command not used

8.4.11 Peripheral DMA Controller

- Multiple channels
- Generates transfers to/from peripherals such as USART and SPI
- Two address pointers/counters per channel allowing double buffering
- Performance monitors to measure average and maximum transfer latency

8.4.12 DMA Controller

- 2 HSB Master Interfaces
- Channels
- Software and Hardware Handshaking Interfaces
  - 9 Hardware Handshaking Interfaces
- Memory/Non-Memory Peripherals to Memory/Non-Memory Peripherals Transfer
- Single-block DMA Transfer
- Multi-block DMA Transfer
  - Linked Lists
  - Auto-Reloading
  - Contiguous Blocks
- DMA Controller is Always the Flow Controller
- Additional Features
  - Scatter and Gather Operations
  - Channel Locking
  - Bus Locking
  - FIFO Mode
  - Pseudo Fly-by Operation

8.4.13 General-Purpose Input/Output Controller

Each I/O line of the GPIO features:

- Configurable pin-change, rising-edge or falling-edge interrupt on any I/O line
- A glitch filter providing rejection of pulses shorter than one clock cycle
- Input visibility and output control
- Multiplexing of up to four peripheral functions per I/O line
- Programmable internal pull-up resistor

Serial Peripheral Interface

- Compatible with an embedded 32-bit microcontroller
- Supports communication with serial external devices
  - Four chip selects with external decoder support allow communication with up to 15 peripherals

  - Serial memories, such as DataFlash and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD controllers, CAN controllers and Sensors
  - External co-processors
- Master or Slave Serial Peripheral Bus Interface
  - 4 - to 16-bit programmable data length per chip select
  - Programmable phase and polarity per chip select
  - Programmable transfer delays between consecutive transfers and between clock and data per chip select
  - Programmable delay between consecutive transfers
  - Selectable mode fault detection
- Connection to Peripheral DMA Controller channel capabilities optimizes data transfers
  - One channel for the receiver, one channel for the transmitter
  - Next buffer support
  - Four character FIFO in reception

8.4.14 Two-Wire Slave Interface

- Compatible with I^2C standard
  - 100 and 400 kbit/s transfer speeds
  - 7 and 10-bit and General Call addressing
- Compatible with SMBus standard
  - Hardware Packet Error Checking (CRC) generation and verification with ACK response
  - SMBALERT interface
  - 25 ms clock low timeout delay
  - 25 ms slave cumulative clock low extend time
- Compatible with PMBus
- DMA interface for reducing CPU load
- Arbitrary transfer lengths, including 0 data bytes
- Optional clock stretching if transmit or receive buffers not ready for data transfer
- 32-bit Peripheral Bus interface for configuration of the interface

8.4.15 Two-Wire Master Interface

- Compatible with I^2C standard
  - Multi-master support
  - 100 and 400 kbit/s transfer speeds
  - 7- and 10-bit and General Call addressing
- Compatible with SMBus standard
  - Hardware Packet Error Checking (CRC) generation and verification with ACK control
  - SMBus ALERT interface
  - 25 ms clock low timeout delay
  - 10 ms master cumulative clock low extend time
  - 25 ms slave cumulative clock low extend time

- Compatible with PMBus
- Compatible with Atmel Two-Wire Interface Serial Memories
- DMA interface for reducing CPU load
- Arbitrary transfer lengths, including 0 data bytes
- Optional clock stretching if transmit or receive buffers not ready for data transfer

8.4.16 Synchronous Serial Controller

- Provides serial synchronous communication links used in audio and telecom applications
- Independent receiver and transmitter, common clock divider
- Interfaced with two Peripheral DMA Controller channels to reduce processor overhead
- Configurable frame sync and data length
- Receiver and transmitter can be configured to start automatically or on detection of different events on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

8.4.17 Universal Synchronous Asynchronous Receiver Transmitter

- Programmable Baud Rate Generator
- 5- to 9-bit Full-duplex Synchronous or Asynchronous Serial Communications
  - 1, 1.5 or 2 Stop Bits in Asynchronous Mode or 1 or 2 Stop Bits in Synchronous Mode
  - Parity Generation and Error Detection
  - Framing Error Detection, Overrun Error Detection
  - MSB- or LSB-first
  - Optional Break Generation and Detection
  - By 8 or by 16 Over-sampling Receiver Frequency
  - Optional Hardware Handshaking RTS-CTS
  - Optional Modem Signal Management DTR-DSR-DCD-RI
  - Receiver Time-out and Transmitter Timeguard
  - Optional Multidrop Mode with Address Generation and Detection
- RS485 with Driver Control Signal
- ISO7816, T = 0 or T = 1 Protocols for Interfacing with Smart Cards
  - NACK Handling, Error Counter with Repetition and Iteration Limit
- IrDA Modulation and Demodulation
  - Communication at up to 115.2 Kbps
- SPI Mode
  - Master or Slave
  - Serial Clock Programmable Phase and Polarity
  - SPI Serial Clock (CLK) Frequency up to Internal Clock Frequency CLK_USART/4
- LIN Mode
  - Compliant with LIN 1.3 and LIN 2.0 specifications
  - Master or Slave
  - Processing of frames with up to 256 data bytes
  - Response Data length can be configurable or defined automatically by the Identifier
  - Self synchronization in Slave node configuration
  - Automatic processing and verification of the “Synch Break” and the “Synch Field”
  - The “Synch Break” is detected even if it is partially superimposed with a data byte
  - Automatic Identifier parity calculation/sending and verification
  - Parity sending and verification can be disabled
  - Automatic Checksum calculation/sending and verification
  - Checksum sending and verification can be disabled
  - Support both “Classic” and “Enhanced” checksum types

  - Full LIN error checking and reporting
  - Frame Slot Mode: the Master allocates slots to the scheduled frames automatically.
  - Generation of the Wakeup signal
- Test Modes
  - Remote Loopback, Local Loopback, Automatic Echo
- Supports Connection of Two Peripheral DMA Controller Channels (PDCA)
  - Offers Buffer Transfer without Processor Intervention

8.4.18 USB On-The-Go Interface

- Compatible with the USB 2.0 specification
- Supports High (480 Mbit/s), Full (12 Mbit/s) and Low (1.5 Mbit/s) speed communication and On-The-Go
- eight pipes/endpoints
- 2368 of Embedded Dual-Port RAM (DPRAM) for Pipes/Endpoints
- Up to 2 memory banks per Pipe/Endpoint (Not for Control Pipe/Endpoint)
- Flexible Pipe/Endpoint configuration and management with dedicated DMA channels
- On-Chip UTMI transceiver including Pull-Ups/Pull-downs
- On-Chip OTG pad including VBUS analog comparator

8.4.19 Timer/Counter

- Three 16-bit Timer Counter channels
- A wide range of functions including:
  - Frequency measurement
  - Event counting
  - Interval measurement
  - Pulse generation
  - Delay timing
  - Pulse width modulation
  - Up/down capabilities
- Each channel is user-configurable and contains:
  - Three external clock inputs
  - Five internal clock inputs
  - Two multi-purpose input/output signals
- Internal interrupt signal
- Two global registers that act on all three TC channels

8.4.20 Analog-to-Digital Converter

- Integrated multiplexer offering up to eight independent analog inputs
- Individual enable and disable of each channel
- Hardware or software trigger
  - External trigger pin
  - Timer counter outputs (corresponding TIOA trigger)
- Peripheral DMA Controller support
- Possibility of ADC timings configuration
- Sleep mode and conversion sequencer
  - Automatic wakeup on trigger and back to sleep mode after conversions of all enabled channels

8.4.21 HSB Bus Performance Monitor

- Allows performance monitoring of High Speed Bus master interfaces
  - Up to 4 masters can be monitored
  - Peripheral Bus access to monitor registers
- The following is monitored
  - Data transfer cycles
  - Bus stall cycles
  - Maximum access latency for a single transfer
- Automatic handling of event overflow

8.4.22 Multimedia Card Interface

- Compatible with Multimedia Card specification version 4.3
- Compatible with SD Memory Card specification version 2.0
- Compatible with SDIO specification version 1.1
- Compatible with CE-ATA specification 1.1
- Cards clock rate up to master clock divided by two
- Boot Operation Mode support
- High Speed mode support
- Embedded power management to slow down clock rate when not used
- Supports 2 Slots
  - Each slot for either a MultiMediaCard bus (up to 30 cards) or an SD Memory Card
- Support for stream, block and multi-block data read and write
- Supports connection to DMA Controller
  - Minimizes processor intervention for large buffer transfers
- Built in FIFO (from 16 to 256 bytes) with large memory aperture supporting incremental access
- Support for CE-ATA completion cignal disable command
- Protection against unexpected modification on-the-Fly of the configuration registers

8.4.23 Error Corrected Code Controller

- Hardware Error Corrected Code Generation with two methods :
  - Hamming code detection and correction by software (ECC-H)
  - Reed-Solomon code detection by hardware, correction by hardware or software (ECC-RS)
- Supports NAND Flash and SmartMedia™ devices with 8- or 16-bit data path for ECC-H, and with 8-bit data path for ECC-RS
- Supports NAND Flash and SmartMedia™ with page sizes of 528, 1056, 2112, and 4224 bytes (specified by software)
- ECC_H supports :
  - One bit correction per page of 512,1024,2048, or 4096 bytes
  - One bit correction per sector of 512 bytes of data for a page size of 512, 1024, 2048, or 4096 bytes
  - One bit correction per sector of 256 bytes of data for a page size of 512, 1024, 2048, or 4096 bytes
- ECC_RS supports :
  - 4 errors correction per sector of 512 bytes of data for a page size of 512, 1024, 2048, and 4096 bytes with 8-bit data path

8.4.24 Advanced Encryption Standart

- Compliant with *FIPS Publication 197, Advanced Encryption Standard (AES)*
- 128-bit/192-bit/256-bit cryptographic key
- 12/14/16 clock cycles encryption/decryption processing time with a 128-bit/192-bit/256-bit cryptographic key
- Support of the five standard modes of operation specified in the *NIST Special Publication 800-38A, Recommendation for Block Cipher Modes of Operation - Methods and Techniques:*
  - Electronic Code Book (ECB)
  - Cipher Block Chaining (CBC)
  - Cipher Feedback (CFB)
  - Output Feedback (OFB)
  - Counter (CTR)
- 8-, 16-, 32-, 64- and 128-bit data size possible in CFB mode
- Last output data mode allows optimized Message Authentication Code (MAC) generation
- Hardware counter measures against differential power analysis attacks
- Connection to DMA Controller capabilities optimizes data transfers for all operating modes

8.4.25 Audio Bitstream DAC

- Digital Stereo DAC
- Oversampled D/A conversion architecture
  - Oversampling ratio fixed 128x
  - FIR equalization filter
  - Digital interpolation filter: Comb4
  - 3rd Order Sigma-Delta D/A converters
- Digital bitstream outputs
- Parallel interface
- Connected to DMA Controller for background transfer without CPU intervention

8.4.26 On-Chip Debug

- Debug interface in compliance with IEEE-ISTO 5001-2003 (Nexus 2.0) Class 2+
- JTAG access to all on-chip debug functions
- Advanced program, data, ownership, and watchpoint trace supported
- NanoTrace JTAG-based trace access
- Auxiliary port for high-speed trace information
- Hardware support for 6 program and 2 data breakpoints
- Unlimited number of software breakpoints supported
- Automatic CRC check of memory regions

8.4.27 JTAG and Boundary Scan

- IEEE1149.1 compliant JTAG Interface
- Boundary-Scan Chain for board-level testing
- Direct memory access and programming capabilities through JTAG Interface
-

9. Boot Sequence

This chapter summarizes the boot sequence of the AT32UC3A3/A4. The behavior after power-up is controlled by the Power Manager. For specific details, refer to Section 9. ”Power Manager (PM)” on page 39.

9.1 Starting of Clocks

After power-up, the device will be held in a reset state by the Power-On Reset circuitry, until the power has stabilized throughout the device. Once the power has stabilized, the device will use the internal RC Oscillator as clock source.

On system start-up, the PLLs are disabled. All clocks to all modules are running. No clocks have a divided frequency, all parts of the system receives a clock with the same frequency as the internal RC Oscillator.

9.2 Fetching of Initial Instructions

After reset has been released, the AVR32 UC CPU starts fetching instructions from the reset address, which is 0x8000_0000. This address points to the first address in the internal Flash.

The code read from the internal Flash is free to configure the system to use for example the PLLs, to divide the frequency of the clock routed to some of the peripherals, and to gate the clocks to unused peripherals.

10. Electrical Characteristics

10.1 Absolute Maximum Ratings*

Operating Temperature	-40°C to +85°C
Storage Temperature	-60°C to +150°C
Voltage on Input Pin with respect to Ground	-0.3V to 3.6V
Maximum Operating Voltage (VDDCORE)	1.95V
Maximum Operating Voltage (VDDIO)	3.6V
Total DC Output Current on all I/O Pin	
for TQFP144 package	370 mA
for TFBGA144 package	370 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

10.2 DC Characteristics

The following characteristics are applicable to the operating temperature range: T_A = -40°C to 85°C, unless otherwise specified and are certified for a junction temperature up toT_J = 100°C.

Table 10-1. DC Characteristics

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
$V_{VDDCORE}$	DC Supply Core			1.65		1.95	V
V_{VDDIO}	DC Supply Peripheral I/Os			3.0		3.6	V
V_{IL}	Input Low-level Voltage			-0.3		+0.8	V
V_{IH}	Input High-level Voltage			2.0		V_{VDDIO} +0.3	V
V_{OL}	Output Low-level Voltage	I_{OL} = -2mA for Pin drive x1 I_{OL} = -4mA for Pin drive x2 I_{OL} = -8mA for Pin drive x3				0.4	V
V_{OH}	Output High-level Voltage	I_{OL} = 2mA for Pin drive x1 I_{OL} = 4mA for Pin drive x2 I_{OL} = 8mA for Pin drive x3		V_{VDDIO} -0.4			V
I_{LEAK}	Input Leakage Current	Pullup resistors disabled				1	µA
C_{IN}	Input Capacitance				7		pF
R_{PULLUP}	Pull-up Resistance			9	15	25	KΩ
I_O	Output Current Pin drive 1x Pin drive 2x Pin drive 3x See Table 10-2					2.0 4.0 8.0	mA
I_{SC}	Static Current	On V_{VDDIN} = 3.3V, CPU in static mode	T_A = 25°C		30		µA
			T_A = 85°C		175		µA

Table 10-2. Pins Drive Capabilities

PIN	Drive	PIN	Drive	PIN	Drive	PIN	Drive	PIN	Drive
PA00	3x	PA22	1x	PC00	1x	P1x6	2x	P3x8	2x
PA01	1x	PA23	1x	PC01	1x	P1x7	2x	P3x9	2x
PA02	1x	PA24	1x	PC02	1x	P1x8	2x	PX40	2x
PA03	1x	PA25	1x	PC03	1x	P1x9	2x	PX41	2x
PA04	1x	PA26	1x	PC04	1x	P2x0	2x	PX42	2x
PA05	1x	PA27	2x	PC05	1x	P21x	2x	PX43	2x
PA06	1x	PA28	1x	PX00	2x	P2x2	2x	PX44	2x
PA07	1x	PA29	1x	PX01	2x	P2x3	2x	PX45	3x
PA08	3x	PA30	1x	PX02	2x	P2x4	2x	PX46	2x
PA09	2x	PA31	1x	PX03	2x	P2x5	2x	PX47	2x
PA10	2x	PB00	1x	PX04	2x	P2x6	2x	PX48	2x
PA11	2x	PB01	1x	PX05	2x	P2x7	2x	PX49	2x
PA12	1x	PB02	1x	PX06	2x	P2x8	2x	PX50	2x
PA13	1x	PB03	1x	PX07	2x	P2x9	2x	PX51	2x
PA14	1x	PB04	1x	PX08	2x	P3x0	2x	PX52	2x
PA15	1x	PB05	3x	PX09	2x	P31x	2x	PX53	2x
PA16	1x	PB06	1x	P1x0	2x	P32x	2x	PX54	2x
PA17	1x	PB07	3x	P1x1	2x	P3x3	2x	PX55	2x
PA18	1x	PB08	2x	P1x2	2x	P3x4	2x	PX56	2x
PA19	1x	PB09	2x	P1x3	2x	P3x5	2x	PX57	2x
PA20	1x	PB10	2x	P1x4	2x	P3x6	2x	PX58	2x
PA21	1x	PB11	1x	P1x5	2x	P3x7	2x	PX59	2x

10.3 Regulator characteristics

Table 10-3. Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{VDDIN}	Supply voltage (input)		2.7	3.3	3.6	V
$V_{VDDCORE}$	Supply voltage (output)		1.81	1.85	1.89	V

Table 10-4. Decoupling Requirements

Symbol	Parameter	Conditions	Typ.	Technology	Unit
C_{IN1}	Input Regulator Capacitor 1		1	NPO	nF
C_{IN2}	Input Regulator Capacitor 2		4.7	X7R	µF
C_{OUT1}	Output Regulator Capacitor 1		470	NPO	pF
C_{OUT2}	Output Regulator Capacitor 2		2.2	X7R	µF

10.4 Analog characteristics

10.4.1 ADC

Table 10-5. Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{VDDANA}	Analog Power Supply		3.0		3.6	V

Table 10-6. Decoupling Requirements

Symbol	Parameter	Conditions	Typ.	Technology	Unit
C_{VDDANA}	Power Supply Capacitor		100	NPO	nF

10.4.2 BOD

Table 10-7. BOD Level Values

Symbol	Parameter Value	Conditions	Min.	Typ.	Max.	Unit
BODLEVEL	00 1111b			1.78		V
	01 0111b			1.69		V
	01 1111b			1.60		V
	10 0111b			1.51		V

Table 10-7 describes the values of the BODLEVEL field in the flash FGPFR register.

Table 10-8. BOD Timing

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{BOD}	Minimum time with VDDCORE < VBOD to detect power failure	Falling VDDCORE from 1.8V to 1.1V		300	800	ns

10.4.3 Reset Sequence

Table 10-9. Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDRR}	VDDCORE rise rate to ensure power-on-reset		0.01			V/ms
V_{DDFR}	VDDCORE fall rate to ensure power-on-reset		0.01		400	V/ms
V_{POR+}	Rising threshold voltage: voltage up to which device is kept under reset by POR on rising VDDCORE	Rising VDDCORE: $V_{RESTART}$ -> V_{POR+}	1.35	1.5	1.6	V
V_{POR-}	Falling threshold voltage: voltage when POR resets device on falling VDDCORE	Falling VDDCORE: 1.8V -> V_{POR+}	1.25	1.3	1.4	V
$V_{RESTART}$	On falling VDDCORE, voltage must go down to this value before supply can rise again to ensure reset signal is released at V_{POR+}	Falling VDDCORE: 1.8V -> $V_{RESTART}$	-0.1		0.5	V
T_{POR}	Minimum time with VDDCORE < V_{POR-}	Falling VDDCORE: 1.8V -> 1.1V		15		µs
T_{RST}	Time for reset signal to be propagated to system			200	400	µs
T_{SSU1}	Time for Cold System Startup: Time for CPU to fetch its first instruction (RCosc not calibrated)		480		960	µs
T_{SSU2}	Time for Hot System Startup: Time for CPU to fetch its first instruction (RCosc calibrated)			420		µs

Figure 10-1. MCU Cold Start-Up RESET_N tied to VDDIN

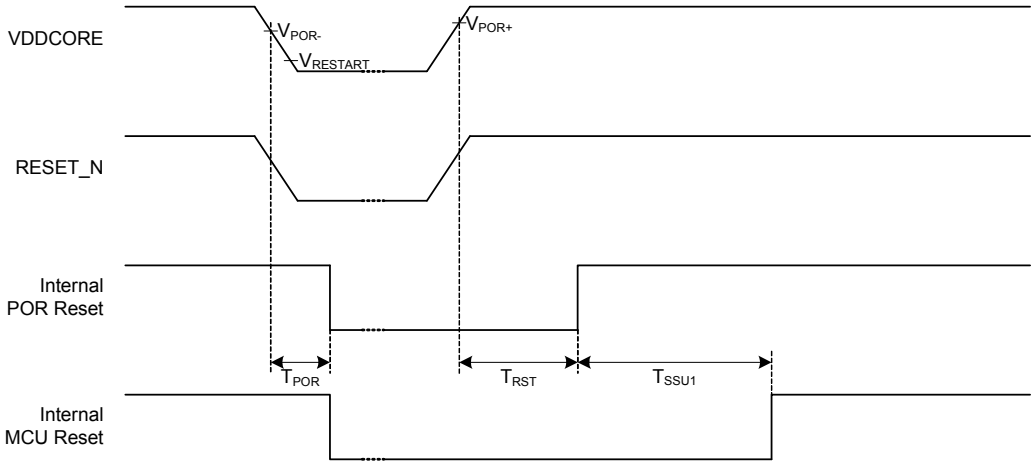


Figure 10-2. MCU Cold Start-Up RESET_N Externally Driven

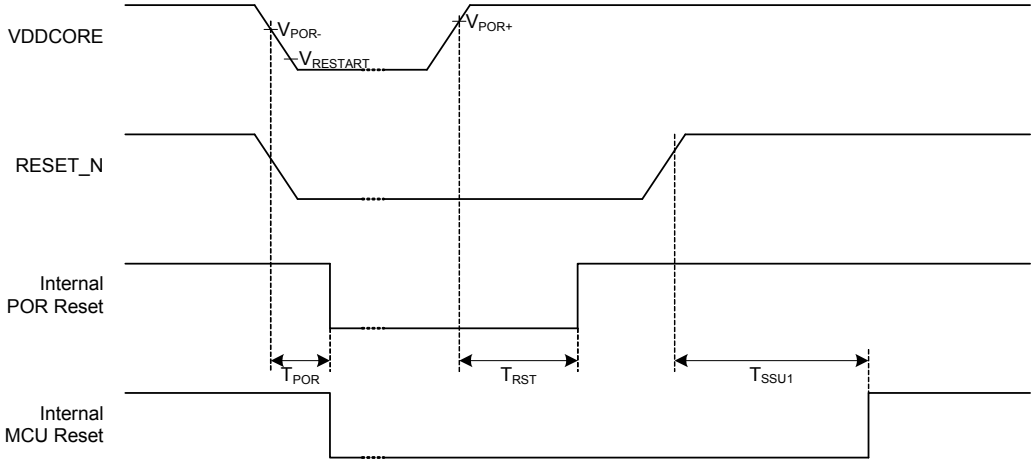
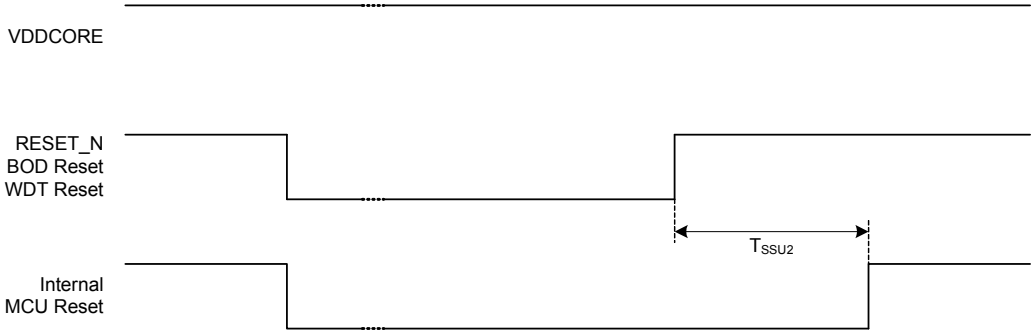


Figure 10-3. MCU Hot Start-Up



10.4.4 RESET_N Characteristics

Table 10-10. RESET_N Waveform Parameters

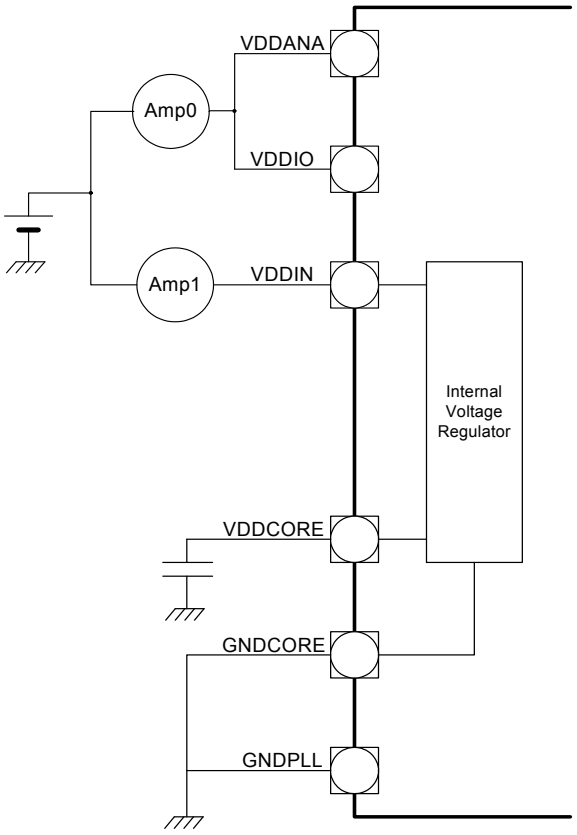
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{RESET}	RESET_N minimum pulse width		10			ns

10.5 Power Consumption

The values in Table 10-11 and Table 10-12 on page 54 are measured values of power consumption with operating conditions as follows:

- V_{DDIO} = 3.3V
- T_A = 25°C
- I/Os are configured in input, pull-up enabled.

Figure 10-4. Measurement Setup



These figures represent the power consumption measured on the power supplies.

Table 10-11. Power Consumption for Different Modes

Mode	Conditions[1]		Typ.	Unit
Active	CPU running from flash CPU clocked from PLL0 at f MHz Voltage regulator is on. XIN0: external clock [1] XIN1 stopped. XIN32 stopped PLL0 running All peripheral clocks activated GPIOs on internal pull-up JTAG unconnected with ext pull-up	f = 12 MHz	10	mA
		f = 24 MHz	18	mA
		f = 36 MHz	27	mA
		f = 50 MHz	34	mA
		f = 60 MHz	42	mA
Static	T_A = 25 °C CPU is in static mode GPIOs on internal pull-up All peripheral clocks de-activated DM and DP pins connected to ground XIN0, Xin1 and XIN32 are stopped	on Amp0	0	µA
		on Amp1	<100	µA

1. Core frequency is generated from XIN0 using the PLL so that 140 MHz < fpll0 < 160 MHz and 10 MHz < fxin0 < 12 MHz

Table 10-12. Power Consumption by Peripheral in Active Mode

Peripheral	Typ.	Unit
GPIO	37	µA/MHz
SMC	10	
SDRAMC	4	
ADC	18	
EBI	31	
INTC	25	
TWI	14	
PDCA	30	
RTC	7	
SPI	13	
SSC	13	
TC	10	
USART	35	

10.6 System Clock Characteristics

These parameters are given in the following conditions:

- V_{DDCORE} = 1.8V
- Ambient Temperature = 25°C

10.6.1 CPU/HSB Clock Characteristics

Table 10-13. Core Clock Waveform Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$1/(t_{CPCPU})$	CPU Clock Frequency				66	MHz
t_{CPCPU}	CPU Clock Period		15,15			ns

10.6.2 PBA Clock Characteristics

Table 10-14. PBA Clock Waveform Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$1/(t_{CPPBA})$	PBA Clock Frequency				66	MHz
t_{CPPBA}	PBA Clock Period		15.15			ns

10.6.3 PBB Clock Characteristics

Table 10-15. PBB Clock Waveform Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$1/(t_{CPPBB})$	PBB Clock Frequency				66	MHz
t_{CPPBB}	PBB Clock Period		15.15			ns

10.7 Oscillator Characteristics

The following characteristics are applicable to the operating temperature range: T_A = -40°C to 85°C and worst case of power supply, unless otherwise specified.

10.7.1 Slow Clock RC Oscillator

Table 10-16. RC Oscillator Frequency

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F_{RC}	RC Oscillator Frequency	Calibration point: T_A = 85°C		115.2	116	KHz
		T_A = 25°C		112		KHz
		T_A = -40°C	105	108		KHz

10.7.2 32 KHz Oscillator

Table 10-17. 32 KHz Oscillator Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$1/(t_{CP32KHz})$	Oscillator Frequency	External clock on XIN32			30	MHz
		Crystal		32 768		Hz
C_L	Equivalent Load Capacitance		6		12.5	pF
ESR	Crystal Equivalent Series Resistance				100	KΩ
t_{ST}	Startup Time	C_L = 6pF(1) C_L = 12.5pF(1)			600 1200	ms
t_{CH}	XIN32 Clock High Half-period		0.4 t_{CP}		0.6 t_{CP}	
t_{CL}	XIN32 Clock Low Half-period		0.4 t_{CP}		0.6 t_{CP}	
C_{IN}	XIN32 Input Capacitance				5	pF
I_{OSC}	Current Consumption	Active mode			1.8	µA
		Standby mode			0.1	µA

Note: 1. C_L is the equivalent load capacitance.

10.7.3 Main Oscillators

Table 10-18. Main Oscillators Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$1/(t_{CPMAIN})$	Oscillator Frequency	External clock on XIN			50	MHz
		Crystal	0.4		20	MHz
C_{L1}, C_{L2}	Internal Load Capacitance ($C_{L1} = C_{L2}$)			7		pF
ESR	Crystal Equivalent Series Resistance				75	Ω
	Duty Cycle		40	50	60	%
t_{ST}	Startup Time	f = 400 KHz f = 8 MHz f = 16 MHz f = 20 MHz				ms
t_{CH}	XIN Clock High Half-period		0.4 t_{CP}		0.6 t_{CP}	
t_{CL}	XIN Clock Low Half-period		0.4 t_{CP}		0.6 t_{CP}	
C_{IN}	XIN Input Capacitance			7		pF
I_{OSC}	Current Consumption	Active mode at 400 KHz. Gain = G0		30		µA
		Active mode at 8 MHz. Gain = G1		45		µA
		Active mode at 16 MHz. Gain = G2		95		µA
		Active mode at 20 MHz. Gain = G3		205		µA

10.7.4 Phase Lock Loop

Table 10-19. PLL Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F_{OUT}	VCO Output Frequency		80		240	MHz
F_{IN}	Input Frequency (after input divider)		4		16	MHz
I_{PLL}	Current Consumption	Active mode (Fout=80 MHz)		250		µA
		Active mode (Fout=240 MHz)		600		µA

10.8 ADC Characteristics

Table 10-20. Channel Conversion Time and ADC Clock

Parameter	Conditions	Min.	Typ.	Max.	Unit
ADC Clock Frequency	10-bit resolution mode			5	MHz
	8-bit resolution mode			8	MHz
Startup Time	Return from Idle Mode			20	µs
Track and Hold Acquisition Time		600			ns
Conversion Time	ADC Clock = 5 MHz			2	µs
	ADC Clock = 8 MHz			1.25	µs
Throughput Rate	ADC Clock = 5 MHz			384 (1)	kSPS
	ADC Clock = 8 MHz			533 (2)	kSPS

1. Corresponds to 13 clock cycles: 3 clock cycles for track and hold acquisition time and 10 clock cycles for conversion.
2. Corresponds to 15 clock cycles: 5 clock cycles for track and hold acquisition time and 10 clock cycles for conversion.

Table 10-21. ADC Power Consumption

Parameter	Conditions	Min.	Typ.	Max.	Unit
Current Consumption on VDDANA (1)	On 13 samples with ADC clock = 5 MHz			1.25	mA

1. Including internal reference input current

Table 10-22. Analog Inputs

Parameter	Conditions	Min.	Typ.	Max.	Unit
Input Voltage Range		0		VDDANA	V
Input Leakage Current				1	µA
Input Capacitance			7		pF

Table 10-23. Transfer Characteristics in 8-bit mode

Parameter	Conditions	Min.	Typ.	Max.	Unit
Resolution			8		Bit
Absolute Accuracy	ADC Clock = 5 MHz			0.8	LSB
	ADC Clock = 8 MHz			1.5	LSB
Integral Non-linearity	ADC Clock = 5 MHz		0.35	0.5	LSB
	ADC Clock = 8 MHz		0.5	1.0	LSB
Differential Non-linearity	ADC Clock = 5 MHz		0.3	0.5	LSB
	ADC Clock = 8 MHz		0.5	1.0	LSB
Offset Error	ADC Clock = 5 MHz	-0.5		0.5	LSB
Gain Error	ADC Clock = 5 MHz	-0.5		0.5	LSB

Table 10-24. Transfer Characteristics in 10-bit mode

Parameter	Conditions	Min.	Typ.	Max.	Unit
Resolution			10		Bit
Absolute Accuracy	ADC Clock = 5 MHz			3	LSB
Integral Non-linearity	ADC Clock = 5 MHz		1.5	2	LSB

Table 10-24. Transfer Characteristics in 10-bit mode

Parameter	Conditions	Min.	Typ.	Max.	Unit
Differential Non-linearity	ADC Clock = 5 MHz		1	2	LSB
	ADC Clock = 2.5 MHz		0.6	1	LSB
Offset Error	ADC Clock = 5 MHz	-2		2	LSB
Gain Error	ADC Clock = 5 MHz	-2		2	LSB

10.9 USB Transceiver Characteristics

10.9.1 Electrical Characteristics

Table 10-25. Electrical Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Input Levels						
V_{IL}	Low Level				TBD	V
V_{IH}	High Level		TBD			V
V_{DI}	Differential Input Sensivity	|(D+) - (D-)|	TBD			V
V_{CM}	Differential Input Common Mode Range		TBD		TBD	V
C_{IN}	Transceiver capacitance	Capacitance to ground on each line			TBD	pF
I	Hi-Z State Data Line Leakage	$0V < V_{IN} < 3.3V$	TBD		TBD	µA
Output Levels						
V_{OL}	Low Level Output	Measured with R_L of 1.425 kΩ tied to 3.6V	TBD		TBD	V
V_{OH}	High Level Output	Measured with R_L of 14.25 kΩ tied to GND	TBD		TBD	V
V_{CRS}	Output Signal Crossover Voltage		TBD		TBD	V
Filtering						
R_{EXT}	Recommended External USB Series Resistor	In series with each USB pin with ±5%		39		Ω
R_{BIAS}	VBIAS External Resistor	±1%		6810		Ω
C_{BIAS}	VBIAS External Capcitor			10		pF

10.9.2 Switching Characteristics

Table 10-26. In Low Speed

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{FR}	Transition Rise Time	C_{LOAD} = 400 pF	TBD		TBD	ns
t_{FE}	Transition Fall Time	C_{LOAD} = 400 pF	TBD		TBD	ns
t_{FRFM}	Rise/Fall time Matching	C_{LOAD} = 400 pF	TBD		TBD	%

Table 10-27. In Full Speed

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{FR}	Transition Rise Time	C_{LOAD} = 50 pF	TBD		TBD	ns
t_{FE}	Transition Fall Time	C_{LOAD} = 50 pF	TBD		TBD	ns
t_{FRFM}	Rise/Fall time Matching		TBD		TBD	%

10.9.3 Static Power Consumption

Table 10-28. Static Power Consumption

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{BIAS}	Bias current consumption on VBG				1	µA
$I_{VDDUTMI}$	HS Transceiver and I/O current consumption				8	µA
	FS/HS Transceiver and I/O current consumption	If cable is connected, add 200µA (typical) due to Pull-up/Pull-down current consumption			3	µA

10.9.4 Dynamic Power Consumption

Table 10-29. Dynamic Power Consumption

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{BIAS}	Bias current consumption on VBG			0.7	0.8	mA
$I_{VDDUTMI}$	HS Transceiver current consumption	HS transmission		47	60	mA
	HS Transceiver current consumption	HS reception		18	27	mA
	FS/HS Transceiver current consumption	FS transmission 0m cable (1)		4	6	mA
	FS/HS Transceiver current consumption	FS transmission 5m cable		26	30	mA
	FS/HS Transceiver current consumption	FS reception		3	4.5	mA

1. Including 1 mA due to Pull-up/Pull-down current consumption.

41.2.1 USB High Speed Design Guidelines

In order to facilitate hardware design, Atmel provides an application note on www.atmel.com.

10.10 EBI Timings

These timings are given for worst case process, T = 85·C, VDDCORE = 1.65V, VDDIO = 3V and 40 pF load capacitance.

10.10.1 SMC Signals

Table 10-30. SMC Clock Signal

Symbol	Parameter	Max.[1]	Unit
$1/(t_{CPSMC})$	SMC Controller Clock Frequency	$1/(t_{cpcpu})$	MHz

Note: 1. The maximum frequency of the SMC interface is the same as the max frequency for the HSB.

Table 10-31. SMC Read Signals with Hold Settings

Symbol	Parameter	Min.	Unit
NRD Controlled (READ_MODE = 1)			
SMC_1	Data Setup before NRD High	12	ns
SMC_2	Data Hold after NRD High	0	ns
SMC_3	NRD High to NBS0/A0 Change[1]	nrd hold length * t_{CPSMC} - 1.3	ns
SMC_4	NRD High to NBS1 Change[1]	nrd hold length * t_{CPSMC} - 1.3	ns
SMC_5	NRD High to NBS2/A1 Change[1]	nrd hold length * t_{CPSMC} - 1.3	ns
SMC_7	NRD High to A2 - A23 Change[1]	nrd hold length * t_{CPSMC} - 1.3	ns
SMC_8	NRD High to NCS Inactive[1]	(nrd hold length - ncs rd hold length) * t_{CPSMC} - 2.3	ns
SMC_9	NRD Pulse Width	nrd pulse length * t_{CPSMC} - 1.4	ns
NRD Controlled (READ_MODE = 0)			
SMC_{10}	Data Setup before NCS High	11.5	ns
SMC_{11}	Data Hold after NCS High	0	ns
SMC_{12}	NCS High to NBS0/A0 Change[1]	ncs rd hold length * t_{CPSMC} - 2.3	ns
SMC_{13}	NCS High to NBS0/A0 Change[1]	ncs rd hold length * t_{CPSMC} - 2.3	ns
SMC_{14}	NCS High to NBS2/A1 Change[1]	ncs rd hold length * t_{CPSMC} - 2.3	ns
SMC_{16}	NCS High to A2 - A23 Change[1]	ncs rd hold length * t_{CPSMC} - 4	ns
SMC_{17}	NCS High to NRD Inactive[1]	ncs rd hold length - nrd hold length)* t_{CPSMC} - 1.3	ns
SMC_{18}	NCS Pulse Width	ncs rd pulse length * t_{CPSMC} - 3.6	ns

Note: 1. hold length = total cycle duration - setup duration - pulse duration. “hold length” is for “ncs rd hold length” or “nrd hold length”.

Table 10-32. SMC Read Signals with no Hold Settings

Symbol	Parameter	Min.	Unit
NRD Controlled (READ_MODE = 1)			
SMC_{19}	Data Setup before NRD High	13.7	ns
SMC_{20}	Data Hold after NRD High	1	ns
NRD Controlled (READ_MODE = 0)			
SMC_{21}	Data Setup before NCS High	13.3	ns
SMC_{22}	Data Hold after NCS High	0	ns

Table 10-33. SMC Write Signals with Hold Settings

Symbol	Parameter	Min.	Unit
NRD Controlled (READ_MODE = 1)			
SMC_{23}	Data Out Valid before NWE High	(nwe pulse length - 1) * t_{CPSMC} - 0.9	ns
SMC_{24}	Data Out Valid after NWE High(1)	nwe hold length * t_{CPSMC} - 6	ns
SMC_{25}	NWE High to NBS0/A0 Change(1)	nwe hold length * t_{CPSMC} - 1.9	ns
SMC_{26}	NWE High to NBS1 Change(1)	nwe hold length * t_{CPSMC} - 1.9	ns
SMC_{29}	NWE High to A1 Change(1)	nwe hold length * t_{CPSMC} - 1.9	ns
SMC_{31}	NWE High to A2 - A23 Change(1)	nwe hold length * t_{CPSMC} - 1.7	ns
SMC_{32}	NWE High to NCS Inactive(1)	(nwe hold length - ncs wr hold length)* t_{CPSMC} - 2.9	ns
SMC_{33}	NWE Pulse Width	nwe pulse length * t_{CPSMC} - 0.9	ns
NRD Controlled (READ_MODE = 0)			
SMC_{34}	Data Out Valid before NCS High	(ncs wr pulse length - 1)* t_{CPSMC} - 4.6	ns
SMC_{35}	Data Out Valid after NCS High(1)	ncs wr hold length * t_{CPSMC} - 5.8	ns
SMC_{36}	NCS High to NWE Inactive(1)	(ncs wr hold length - nwe hold length)* t_{CPSMC} - 0.6	ns

Note: 1. hold length = total cycle duration - setup duration - pulse duration. “hold length” is for “ncs wr hold length” or “nwe hold length"

Table 10-34. SMC Write Signals with No Hold Settings (NWE Controlled only)

Symbol	Parameter	Min.	Unit
SMC_{37}	NWE Rising to A2-A25 Valid	5.4	ns
SMC_{38}	NWE Rising to NBS0/A0 Valid	5	ns
SMC_{39}	NWE Rising to NBS1 Change	5	ns
SMC_{40}	NWE Rising to A1/NBS2 Change	5	ns
SMC_{41}	NWE Rising to NBS3 Change	5	ns
SMC_{42}	NWE Rising to NCS Rising	5.1	ns

Table 10-34. SMC Write Signals with No Hold Settings (NWE Controlled only)

Symbol	Parameter	Min.	Unit
SMC_{43}	Data Out Valid before NWE Rising	(nwe pulse length - 1) * t_{CPSMC} - 1.2	ns
SMC_{44}	Data Out Valid after NWE Rising	5	ns
SMC_{45}	NWE Pulse Width	nwe pulse length * t_{CPSMC} - 0.9	ns

Figure 10-5. SMC Signals for NCS Controlled Accesses.

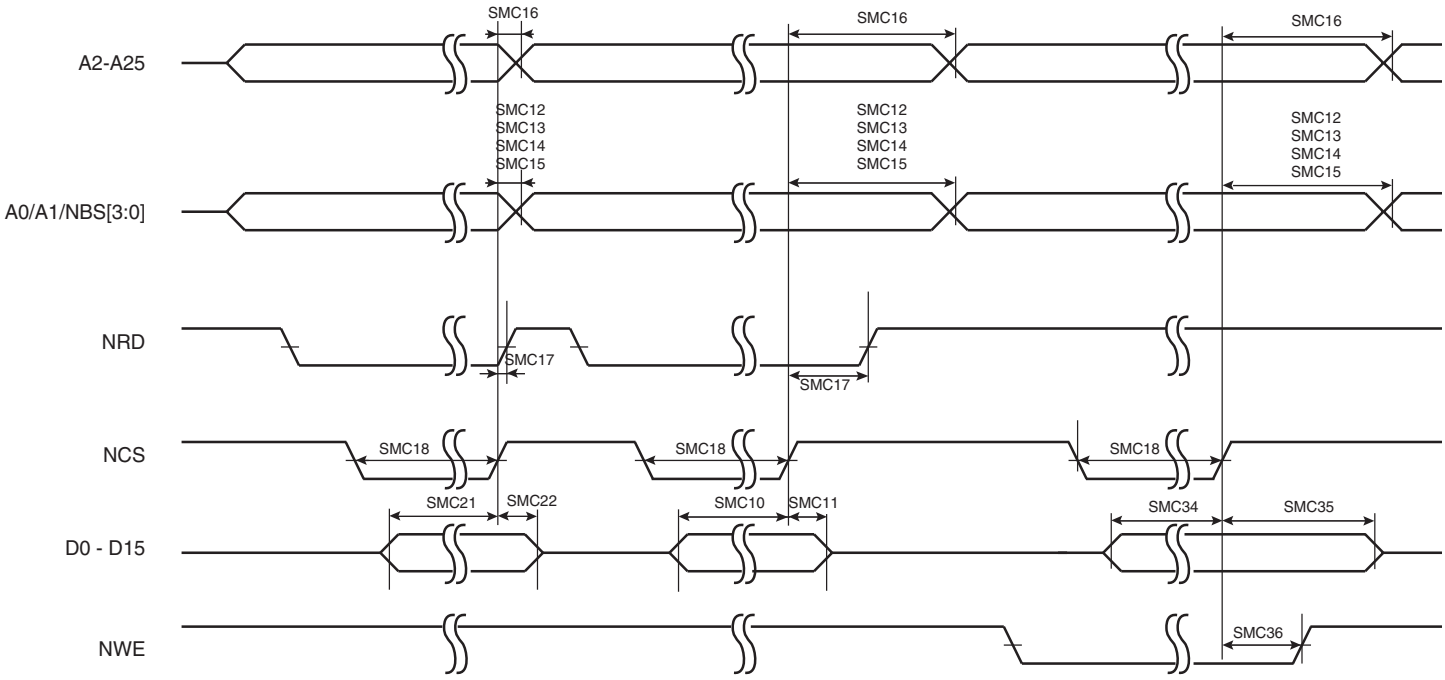
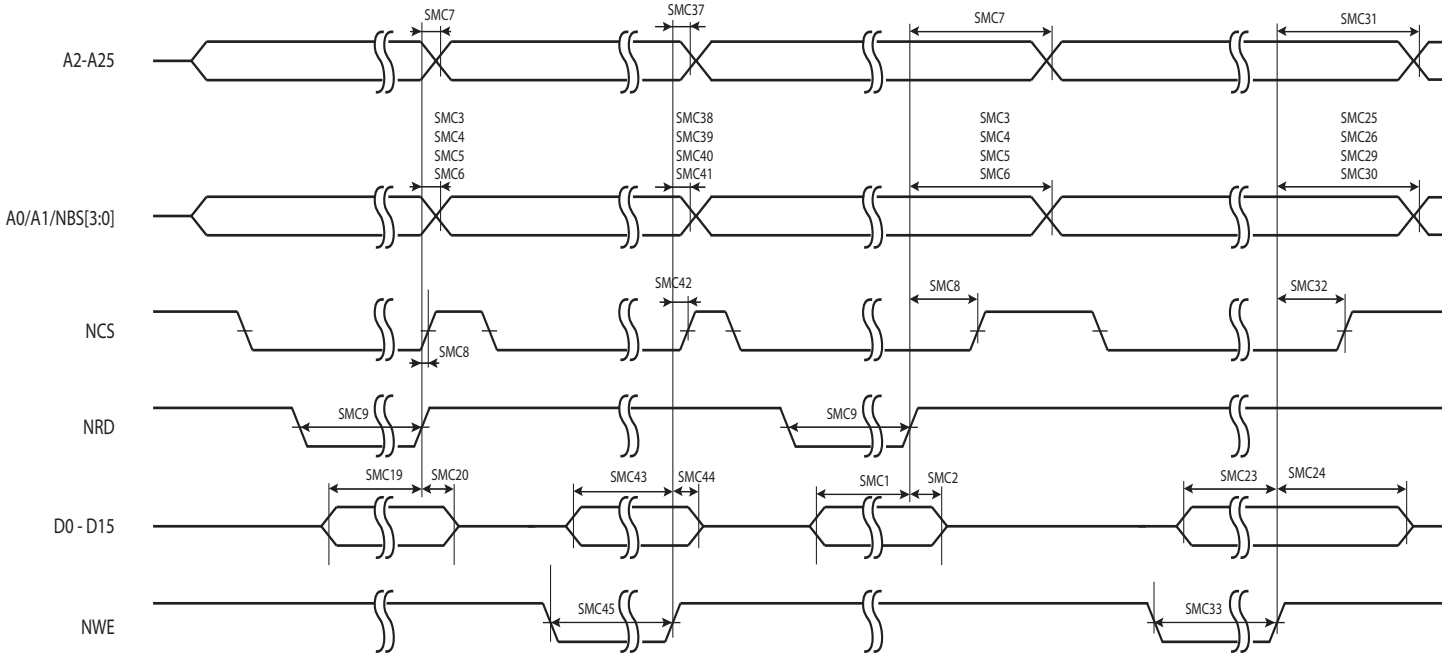


Figure 10-6. SMC Signals for NRD and NRW Controlled Accesses.



10.10.2 SDRAM Signals

These timings are given for 10 pF load on SDCK and 40 pF on other signals.

Table 10-35. SDRAM Clock Signal.

Symbol	Parameter	Conditions	Min.	Max.[1]	Unit
$1/(t_{CPSDCK})$	SDRAM Controller Clock Frequency			$1/(t_{cpcpu})$	MHz

Note: 1. The maximum frequency of the SDRAMC interface is the same as the max frequency for the HSB.

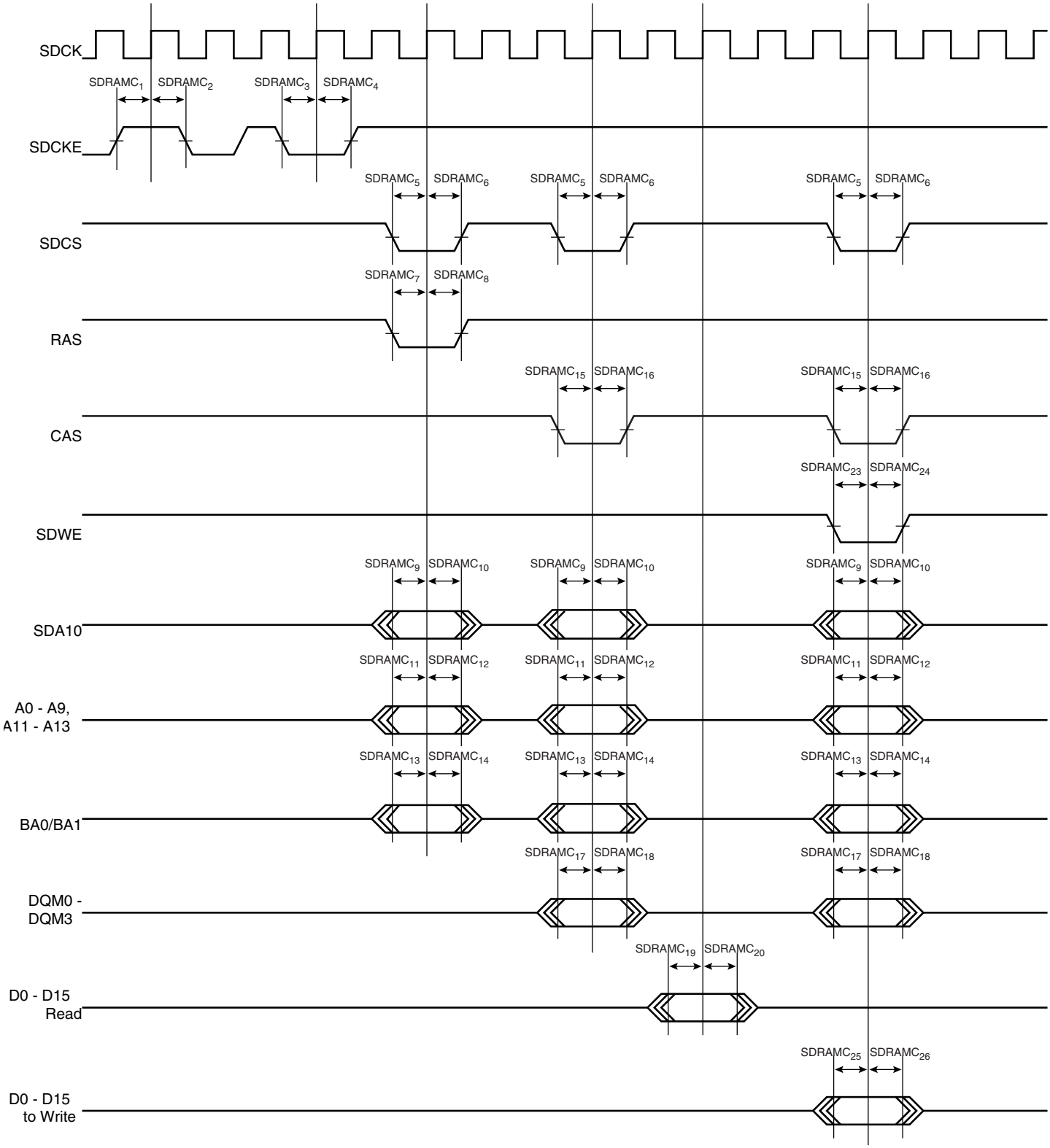
Table 10-36. SDRAM Clock Signal

Symbol	Parameter	Conditions	Min.	Max.	Unit
$SDRAMC_1$	SDCKE High before SDCK Rising Edge		7.4		ns
$SDRAMC_2$	SDCKE Low after SDCK Rising Edge		3.2		ns
$SDRAMC_3$	SDCKE Low before SDCK Rising Edge		7		ns
$SDRAMC_4$	SDCKE High after SDCK Rising Edge		2.9		ns
$SDRAMC_5$	SDCS Low before SDCK Rising Edge		7.5		ns
$SDRAMC_6$	SDCS High after SDCK Rising Edge		1.6		ns
$SDRAMC_7$	RAS Low before SDCK Rising Edge		7.2		ns
$SDRAMC_8$	RAS High after SDCK Rising Edge		2.3		ns
$SDRAMC_9$	SDA10 Change before SDCK Rising Edge		7.6		ns
$SDRAMC_{10}$	SDA10 Change after SDCK Rising Edge		1.9		ns
$SDRAMC_{11}$	Address Change before SDCK Rising Edge		6.2		ns
$SDRAMC_{12}$	Address Change after SDCK Rising Edge		2.2		ns

Table 10-36. SDRAM Clock Signal

Symbol	Parameter	Conditions	Min.	Max.	Unit
$SDRAMC_{13}$	Bank Change before SDCK Rising Edge		6.3		ns
$SDRAMC_{14}$	Bank Change after SDCK Rising Edge		2.4		ns
$SDRAMC_{15}$	CAS Low before SDCK Rising Edge		7.4		ns
$SDRAMC_{16}$	CAS High after SDCK Rising Edge		1.9		ns
$SDRAMC_{17}$	DQM Change before SDCK Rising Edge		6.4		ns
$SDRAMC_{18}$	DQM Change after SDCK Rising Edge		2.2		ns
$SDRAMC_{19}$	D0-D15 in Setup before SDCK Rising Edge		9		ns
$SDRAMC_{20}$	D0-D15 in Hold after SDCK Rising Edge		0		ns
$SDRAMC_{23}$	SDWE Low before SDCK Rising Edge		7.6		ns
$SDRAMC_{24}$	SDWE High after SDCK Rising Edge		1.8		ns
$SDRAMC_{25}$	D0-D15 Out Valid before SDCK Rising Edge		7.1		ns
$SDRAMC_{26}$	D0-D15 Out Valid after SDCK Rising Edge		1.5		ns

Figure 10-7. SDRAMC Signals relative to SDCK.



10.11 JTAG Characteristics

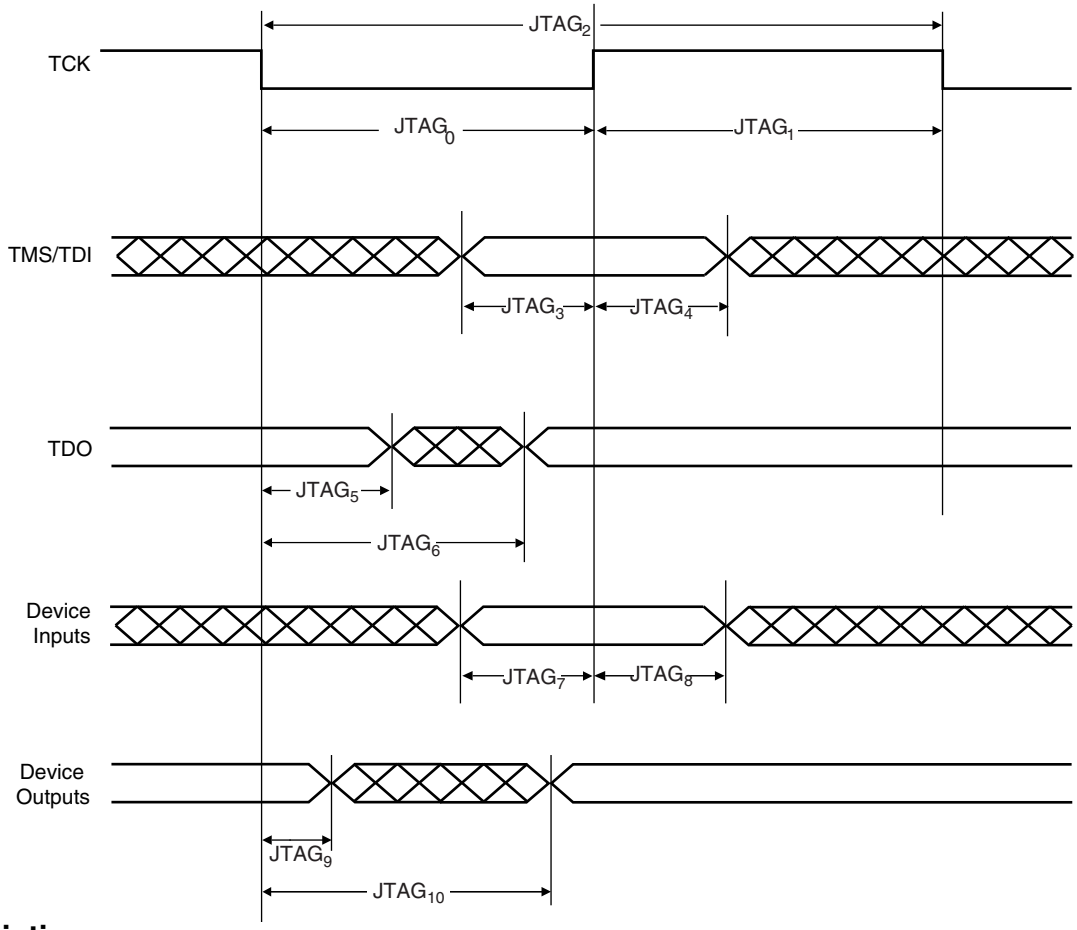
10.11.1 JTAG Interface Signals

Table 10-37. JTAG Interface Timing Specification

Symbol	Parameter	Conditions [1]	Min.	Max.	Unit
$JTAG_0$	TCK Low Half-period		6		ns
$JTAG_1$	TCK High Half-period		3		ns
$JTAG_2$	TCK Period		9		ns
$JTAG_3$	TDI, TMS Setup before TCK High		1		ns
$JTAG_4$	TDI, TMS Hold after TCK High		0		ns
$JTAG_5$	TDO Hold Time		4		ns
$JTAG_6$	TCK Low to TDO Valid			6	ns
$JTAG_7$	Device Inputs Setup Time				ns
$JTAG_8$	Device Inputs Hold Time				ns
$JTAG_9$	Device Outputs Hold Time				ns
$JTAG_{10}$	TCK to Device Outputs Valid				ns

1. V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 40pF

Figure 10-8. JTAG Interface Signals



10.12 SPI Characteristics

Figure 10-9. SPI Master mode with (CPOL= NCPHA= 0) or (CPOL= NCPHA= 1)

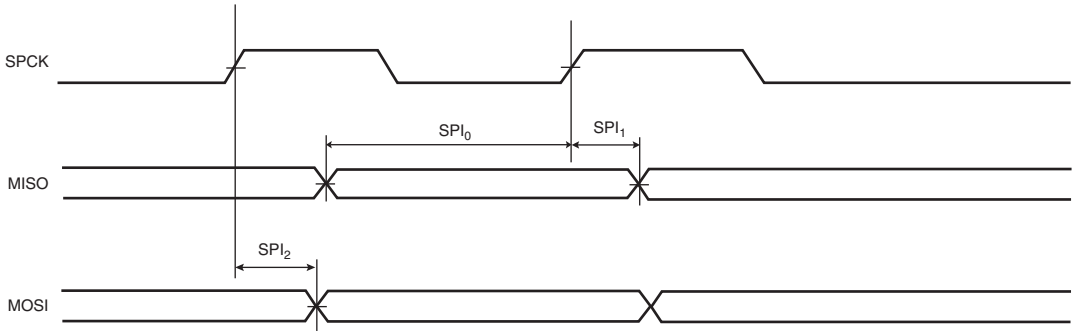


Figure 10-10. SPI Master mode with (CPOL= 0 and NCPHA= 1) or (CPOL= 1 and NCPHA= 0)

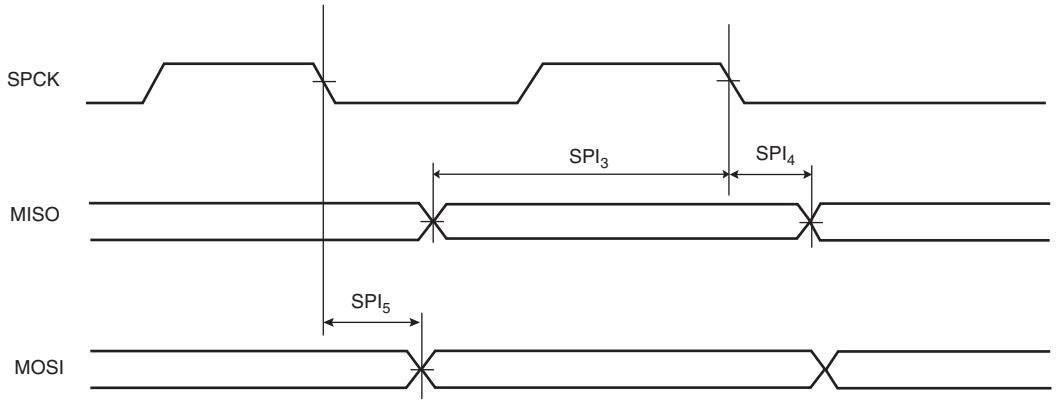


Figure 10-11. SPI Slave mode with (CPOL= 0 and NCPHA= 1) or (CPOL= 1 and NCPHA= 0)

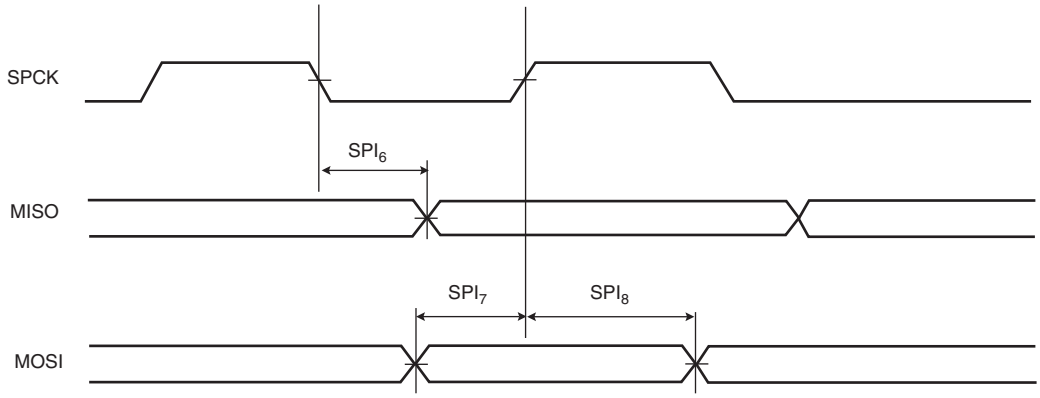


Figure 10-12. SPI Slave mode with (CPOL= NCPHA= 0) or (CPOL= NCPHA= 1)

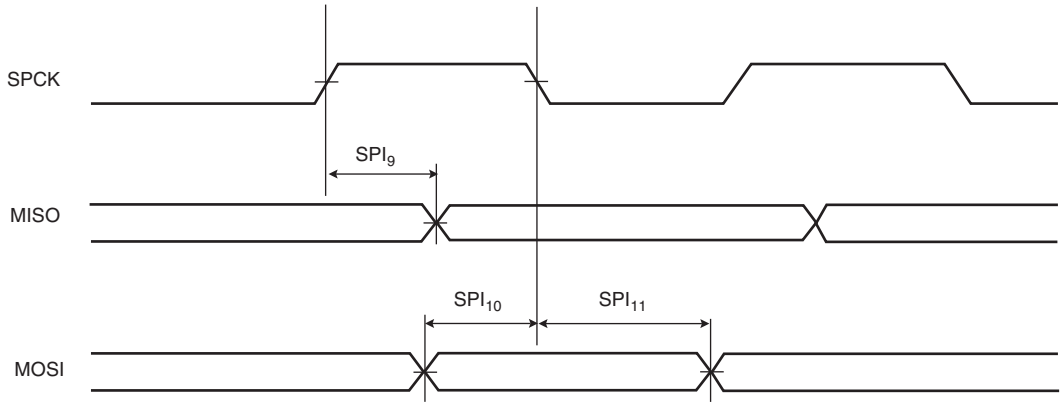


Table 10-38. SPI Timings

Symbol	Parameter	Conditions [1]	Min.	Max.	Unit
SPI_0	MISO Setup time before SPCK rises (master)	3.3V domain	22 + $(t_{CPMCK})/2$ [2]		ns
SPI_1	MISO Hold time after SPCK rises (master)	3.3V domain	0		ns
SPI_2	SPCK rising to MOSI Delay (master)	3.3V domain		7	ns
SPI_3	MISO Setup time before SPCK falls (master)	3.3V domain	22 + $(t_{CPMCK})/2$ [3]		ns
SPI_4	MISO Hold time after SPCK falls (master)	3.3V domain	0		ns
SPI_5	SPCK falling to MOSI Delay master)	3.3V domain		7	ns
SPI_6	SPCK falling to MISO Delay (slave)	3.3V domain		26.5	ns
SPI_7	MOSI Setup time before SPCK rises (slave)	3.3V domain	0		ns
SPI_8	MOSI Hold time after SPCK rises (slave)	3.3V domain	1.5		ns
SPI_9	SPCK rising to MISO Delay (slave)	3.3V domain		27	ns
SPI_{10}	MOSI Setup time before SPCK falls (slave)	3.3V domain	0		ns
SPI_{11}	MOSI Hold time after SPCK falls (slave)	3.3V domain	1		ns

1. 3.3V domain: V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 40 pF
2. t_{CPMCK}: Master Clock period in ns.
3. t_{CPMCK}: Master Clock period in ns.

10.13 MCI

The High Speed MultiMedia Card Interface (MCI) supports the MultiMedia Card (MMC) Specification V4.2, the SD Memory Card Specification V2.0, the SDIO V1.1 specification and CE-ATA V1.1.

10.14 Flash Memory Characteristics

The following table gives the device maximum operating frequency depending on the field FWS of the Flash FSR register. This field defines the number of wait states required to access the Flash Memory. Flash operating frequency equals the CPU/HSB frequency.

Table 10-39. Flash Operating Frequency

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F_{FOP}	Flash Operating Frequency	FWS = 0			36	MHz
		FWS = 1			66	MHz

Table 10-40. Parts Programming Time

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{FPP}	Page Programming Time			4		ms
T_{FFP}	Fuse Programming Time			0.5		ms
T_{FCE}	Chip erase Time			8		ms

Table 10-41. Flash Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N_{FARRAY}	Flash Array Write/Erase cycle				100K	cycle
N_{FFUSE}	General Purpose Fuses write cycle				1000	cycle
T_{FDR}	Flash Data Retention Time			15		year

11. Mechanical Characteristics

11.1 Thermal Considerations

11.1.1 Thermal Data

Table 11-1 summarizes the thermal resistance data depending on the package.

Table 11-1. Thermal Resistance Data

Symbol	Parameter	Condition	Package	Typ	Unit
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	TQFP144	40.3	°C/W
θ_{JC}	Junction-to-case thermal resistance		TQFP144	9.5	
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	TFBGA144	28.5	°C/W
θ_{JC}	Junction-to-case thermal resistance		TFBGA144	6.9	
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	VFBGA100	31.1	°C/W
θ_{JC}	Junction-to-case thermal resistance		VFBGA100	6.9	

11.1.2 Junction Temperature

The average chip-junction temperature, T_J, in °C can be obtained from the following:

1. $T_J = T_A + (P_D \times \theta_{JA})$
2. $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

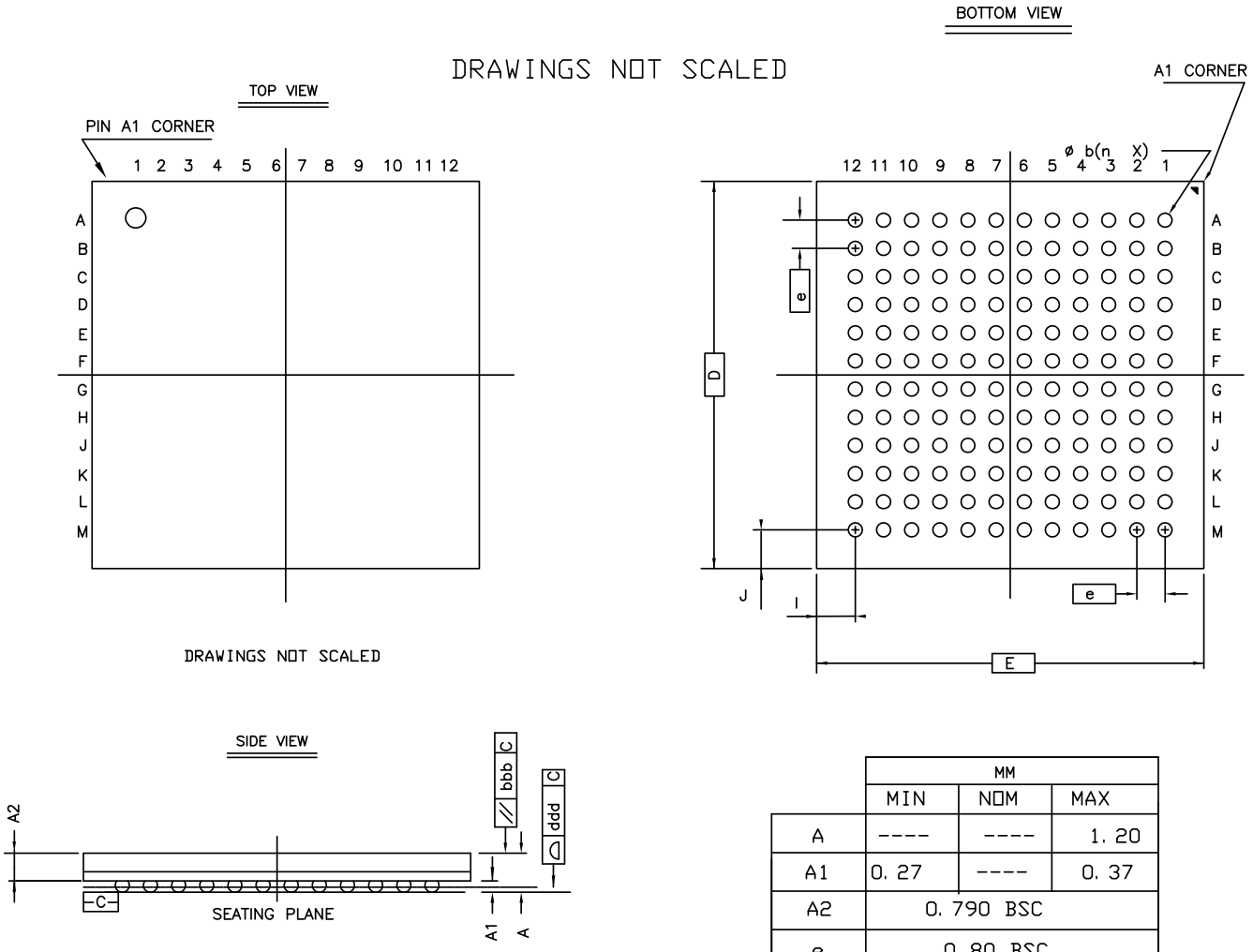
where:

- θ_{JA} = package thermal resistance, Junction-to-ambient (°C/W), provided in Table 11-1 on page 73.
- θ_{JC} = package thermal resistance, Junction-to-case thermal resistance (°C/W), provided in Table 11-1 on page 73.
- $\theta_{HEAT\ SINK}$ = cooling device thermal resistance (°C/W), provided in the device datasheet.
- P_D = device power consumption (W) estimated from data provided in the section "Regulator characteristics" on page 49.
- T_A = ambient temperature (°C).

From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature T_J in °C.

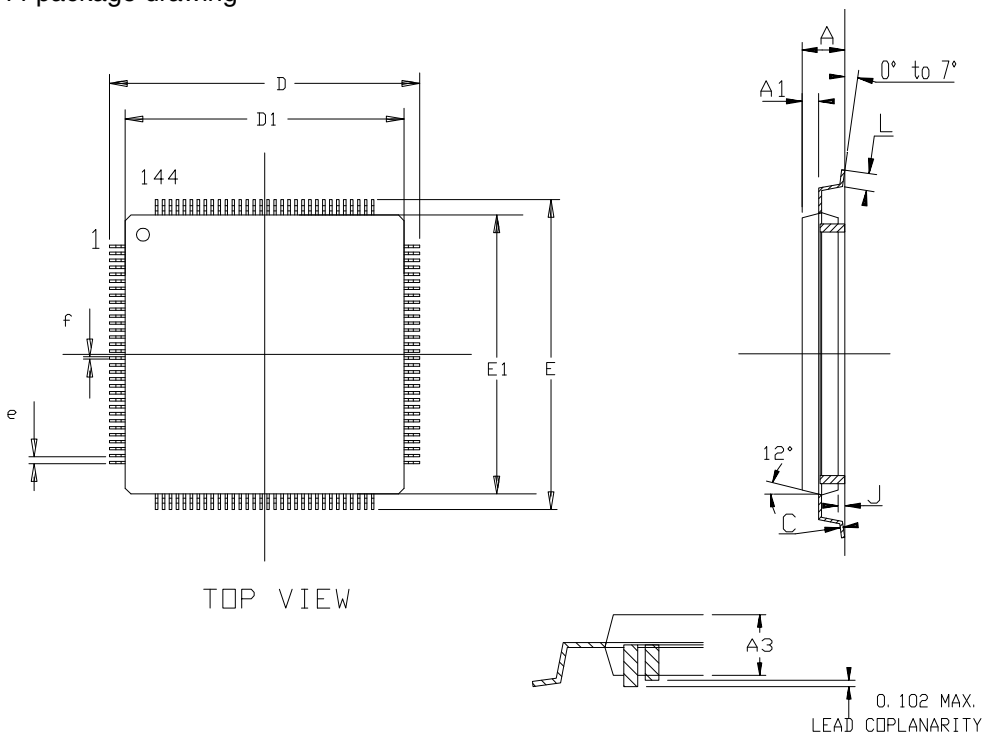
11.2 Package Drawings

Figure 11-1. TFBGA 144 package drawing



	MM		
	MIN	NOM	MAX
A	----	----	1.20
A1	0.27	----	0.37
A2	0.790 BSC		
e	0.80 BSC		
b	0.38	----	0.48
E/D	11.00 BSC		
I/J	1.100 REF		
ddd	coplar 0.120		
bbb	coplar 0.200		

Figure 11-2. LQFP-144 package drawing



	MM			INCH		
	Min	Nom	Max	Min	Nom	Max
A	–	–	1.60	–	–	.063
C	0.09	–	0.20	.004	–	.008
A3	1.35	1.40	1.45	.053	.055	.057
D	21.90	22.00	22.10	.862	.866	.870
D1	19.90	20.00	20.10	.783	.787	.791
E	21.90	22.00	22.10	.862	.866	.870
E1	19.90	20.00	20.10	.783	.787	.791
J	0.05	–	0.15	.002	–	.006
L	0.45	0.60	0.75	.018	.024	.030
e	0.50 BSC			.0197 BSC		
f	0.22 BSC			.009 BSC		

Table 11-2. Device and Package Maximum Weight

1300	mg

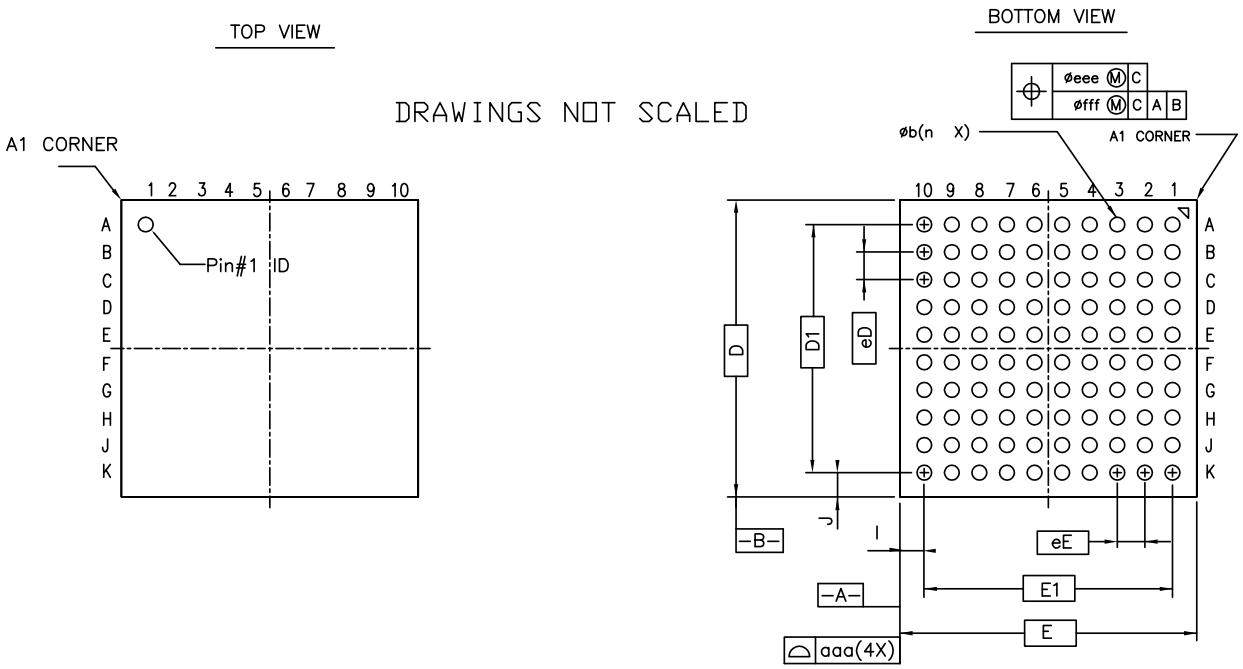
Table 11-3. Package Characteristics

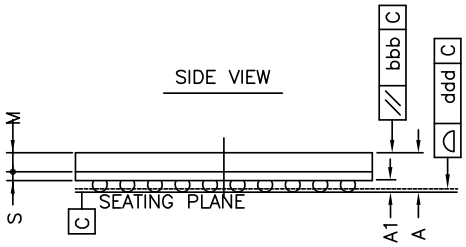
Moisture Sensitivity Level	MSL3

Table 11-4. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

Figure 11-3. VFBGA-100 package drawing





	MM		
	MIN	NOM	MAX
A	----	----	1.000
A1	0.220	----	0.320
M	0.450 BSC		
S	0.210 BSC		
b	0.300	----	0.400
E/D	7.00 +/- 0.100		
e	0.65 BSC		
I/J	0.570		
ddd	copla: 0.080		
bbb	mold flatness: 0.100		

11.3 Soldering Profile

Table 11-5 gives the recommended soldering profile from J-STD-20.

Table 11-5. Soldering Profile

Profile Feature	Green Package
Average Ramp-up Rate (217°C to Peak)	3°C/Second max
Preheat Temperature 175°C ±25°C	150-200°C
Time Maintained Above 217°C	60-150 seconds
Time within 5°C of Actual Peak Temperature	30 seconds
Peak Temperature Range	260 (+0/-5°C)
Ramp-down Rate	6°C/Second max.
Time 25°C to Peak Temperature	8 minutes max

Note: It is recommended to apply a soldering temperature higher than 250°C.

A maximum of three reflow passes is allowed per component.

12. Ordering Information

Device	Ordering Code	Package	Conditioning	Temperature Operating Range
AT32UC3A3256S	AT32UC3A3256S-ALUT	144-lead LQFP	Tray	Industrial (-40·C to 85·C)
	AT32UC3A3256S-ALUR	144-lead LQFP	Reels	Industrial (-40·C to 85·C)
	AT32UC3A3256S-CTUT	144-ball TFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A3256S-CTUR	144-ball TFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A3256	AT32UC3A3256-ALUT	144-lead LQFP	Tray	Industrial (-40·C to 85·C)
	AT32UC3A3256-ALUR	144-lead LQFP	Reels	Industrial (-40·C to 85·C)
	AT32UC3A3256-CTUT	144-ball TFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A3256-CTUR	144-ball TFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A3128S	AT32UC3A3128S-ALUT	144-lead LQFP	Tray	Industrial (-40·C to 85·C)
	AT32UC3A3128S-ALUR	144-lead LQFP	Reels	Industrial (-40·C to 85·C)
	AT32UC3A3128S-CTUT	144-ball TFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A3128S-CTUR	144-ball TFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A3128	AT32UC3A3128-ALUT	144-lead LQFP	Tray	Industrial (-40·C to 85·C)
	AT32UC3A3128-ALUR	144-lead LQFP	Reels	Industrial (-40·C to 85·C)
	AT32UC3A3128-CTUT	144-ball TFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A3128-CTUR	144-ball TFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A364S	AT32UC3A364S-ALUT	144-lead LQFP	Tray	Industrial (-40·C to 85·C)
	AT32UC3A364S-ALUR	144-lead LQFP	Reels	Industrial (-40·C to 85·C)
	AT32UC3A364S-CTUT	144-ball TFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A364S-CTUR	144-ball TFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A364	AT32UC3A364-ALUT	144-lead LQFP	Tray	Industrial (-40·C to 85·C)
	AT32UC3A364-ALUR	144-lead LQFP	Reels	Industrial (-40·C to 85·C)
	AT32UC3A364-CTUT	144-ball TFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A364-CTUR	144-ball TFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A4256S	AT32UC3A4256S-C1UT	100-ball VFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A4256S-C1UR	100-ball VFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A4256	AT32UC3A4256-C1UT	100-ball VFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A4256-C1UR	100-ball VFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A4128S	AT32UC3A4128S-C1UT	100-ball VFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A4128S-C1UR	100-ball VFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A4128	AT32UC3A4128-C1UT	100-ball VFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A4128-C1UR	100-ball VFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A464S	AT32UC3A464S-C1UT	100-ball VFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A464S-C1UR	100-ball VFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A464	AT32UC3A464-C1UT	100-ball VFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A464-C1UR	100-ball VFBGA	Reels	Industrial (-40·C to 85·C)

13. Errata

13.1 Rev. G

13.1.1 Processor and Architecture

1. **LDM instruction with PC in the register list and without ++ increments Rp**
   For LDM with PC in the register list: the instruction behaves as if the ++ field is always set, ie the pointer is always updated. This happens even if the ++ field is cleared. Specifically, the increment of the pointer is done in parallel with the testing of R12.
   Fix/Workaround
   None.

2. **Hardware breakpoints on MAC instructions may corrupt the destination registerof the MAC instruction.**
   Fix/Workaround
   Place breakpoints on earlier or later instructions.

3. **When the main clock is RCSYS, TIMER_CLOCK5 is equal to PBA clock**
   When the main clock is generated from RCSYS, TIMER_CLOCK5 is equal to PBA Clock and not PBA Clock / 128.
   Fix/workaround
   None.

4. **Clock sources will not be stopped in STATIC sleep mode if the difference between CPU and PBx division factor is too big.**
   If the division factor between the CPU/HSB and PBx frequencies is more than 4 when going to a sleep mode where the system RC oscillator is turned off, then high speed clock sources will not be turned off. This will result in a significantly higher power consumption during the sleep mode.
   Fix/Workaround
   Before going to sleep modes where the system RC oscillator is stopped, make sure that the factor between the CPU/HSB and PBx frequencies is less than or equal to 4.

13.1.2 MPU

1. **Privilege violation when using interrupts in application mode with protected system stack**
   If the system stack is protected by the MPU and an interrupt occurs in application mode, an MPU DTLB exception will occur.
   Fix/Workaround
   Make a DTLB Protection (Write) exception handler which permits the interrupt request to be handled in privileged mode.

13.1.3 ADC

1. **Sleep Mode activation needs additional A to D conversion**
   If the ADC sleep mode is activated when the ADC is idle the ADC will not enter sleep mode before after the next AD conversion.

   Fix/Workaround
   Activate the sleep mode in the mode register and then perform an AD conversion.

13.1.4 USART

1. **The NER register always returns zero.**
   Fix/Workaround
   None

13.1.5 SPI

1. **SPI Disable does not work in Slave mode**
   Fix/workaround
   Read the last received data then perform a Software reset.

2. **SPI Bad Serial Clock Generation on 2nd chip_select when SCBR = 1, CPOL=1 and NCPHA=0**
   When multiple CS are in use, if one of the baudrate equals to 1 and one of the others doesn't equal to 1, and CPOL=1 and CPHA=0, then an additional pulse will be generated on SCK.
   Fix/workaround
   When multiple CS are in use, if one of the baudrate equals 1, the other must also equal 1 if CPOL=1 and CPHA=0.

3. **SPI RDR.PCS is not correct**
   The PCS (Peripheral Chip Select) field in the SPI RDR (Receive Data Register) does not correctly indicate the value on the NPCS pins at the end of a transfer.
   Fix/Workaround
   Do not use the PCS field of the SPI RDR.

4. **SPI data transfer hangs with CSAAT=1 in CSR0 and MODFDIS=0 in MR**
   When CSAAT=1 in CSR0 and mode fault detection is enabled (MODFDIS=0 in MR), the SPI module will not start a data transfer.
   Fix/Workaround
   Disable mode fault detection by writing a one to MODFDIS in MR.

5. **Disabling SPI has no effect on the TDRE flag**
   Disabling SPI has no effect on TDRE whereas the write data command is filtered when SPI is disabled. This means that as soon as the SPI is disabled it becomes impossible to reset the TDRE flag by writing in the TDR. So if the SPI is disabled during a PDCA transfer, the PDCA will continue to write data in the TDR (as TDRE stays high) until its buffer is empty, and all data written after the disable command is lost.
   Fix/Workaround
   Disable the PDCA, 2 NOP (minimum), disable SPI. When you want to continue the transfer: Enable SPI, enable PDCA.

13.1.6 PDCA

1. **PCONTROL.CHxRES is nonfunctional**
   PCONTROL.CHxRES is nonfunctional. Counters are reset at power-on, and cannot be reset by software.
   Fix/Workaround
   Software needs to keep history of performance counters.

2. **Transfer error will stall a transmit peripheral handshake interface.**
   If a tranfer error is encountered on a channel transmitting to a peripheral, the peripheral handshake of the active channel will stall and the PDCA will not do any more transfers on the affected peripheral handshake interface.

Fix/workaround:
Disable and then enable the peripheral after the transfer error.

13.1.7 AES

1. **URAD (Unspecified Register Access Detection Status) does not detect read accesses to the write-only KEYW[5..8]R registers**
   Fix/Workaround
   None.

13.1.8 HMATRIX

1. **In the HMATRIX PRAS and PRBS registers MxPR fields are only two bits**
   In the HMATRIX PRAS and PRBS registers MxPR fields are only two bits wide, instead of four bits. The unused bits are undefined when reading the registers.
   Fix/Workaround
   Mask undefined bits when reading PRAS and PRBS.

13.1.9 TWIM

1. **TWIM SR.IDLE goes high immediately when NAK is received**
   When a NAK is received and there is a non-zero number of bytes to be transmitted, SR.IDLE goes high immediately and does not wait for the STOP condition to be sent. This does not cause any problem just by itself, but can cause a problem if software waits for SR.IDLE to go high and then immediately disables the TWIM by writing a one to CR.MDIS. Disabling the TWIM causes the TWCK and TWD pins to go high immediately, so the STOP condition will not be transmitted correctly.
   Fix/Workaround
   If possible, do not disable the TWIM. If it is absolutely necessary to disable the TWIM, there must be a software delay of at least two TWCK periods between the detection of SR.IDLE==1 and the disabling of the TWIM.

13.2 Rev. E

13.2.1 General

1. **3.3V supply monitor is not available on revE.**
   3.3V supply monitor is not available on revE.
   Fix/workaround
   None.

2. **Service access bus (SAB) can not access DMACA registers.**
   Workaround
   None.

3. **Increased Power Consumption in VDDIO in sleep modes.**
   If the OSC0 is enabled in crystal mode when entering a sleep mode where the OSC0 is disabled, this will lead to an increased power consumption in VDDIO.
   Workaround
   Disable OSC0 manually through the Power Manager (PM) before going to any sleep modes where the OSC0 is disabled automatically, or pull down or up XIN0 or XOUT0 with 1Mohm resistor.

4. **When the main clock is RCSYS, TIMER_CLOCK5 is equal to PBA clock**
   When the main clock is generated from RCSYS, TIMER_CLOCK5 is equal to PBA Clock and not PBA Clock / 128.
   Fix/workaround
   None.

5. **Clock sources will not be stopped in STATIC sleep mode if the difference between CPU and PBx division factor is too big.**
   If the division factor between the CPU/HSB and PBx frequencies is more than 4 when going to a sleep mode where the system RC oscillator is turned off, then high speed clock sources will not be turned off. This will result in a significantly higher power consumption during the sleep mode.
   Fix/Workaround
   Before going to sleep modes where the system RC oscillator is stopped, make sure that the factor between the CPU/HSB and PBx frequencies is less than or equal to 4.

6. **Increased Power Consumption in VDDIN in sleep modes**
   Increased Power Consumption in VDDIN in sleep modes.
   Fix/Workaround
   Set to 1b bit CORRS4 of the the ECCHRS mode register (MD). In C-code: *((volatile int*) (0xFFFE2404))= 0x400;

13.2.2 Processor and Architecture

1. **LDM instruction with PC in the register list and without ++ increments Rp**
   For LDM with PC in the register list: the instruction behaves as if the ++ field is always set, ie the pointer is always updated. This happens even if the ++ field is cleared. Specifically, the increment of the pointer is done in parallel with the testing of R12.
   Fix/Workaround
   None.

2. **Hardware breakpoints on MAC instructions may corrupt the destination registerof the MAC instruction.**
   Fix/Workaround
   Place breakpoints on earlier or later instructions.

13.2.3 MPU

1. **Privilege violation when using interrupts in application mode with protected system stack**
   If the system stack is protected by the MPU and an interrupt occurs in application mode, an MPU DTLB exception will occur.
   Fix/Workaround
   Make a DTLB Protection (Write) exception handler which permits the interrupt request to be handled in privileged mode.

13.2.4 ADC

1. **Sleep Mode activation needs additional A to D conversion**
   If the ADC sleep mode is activated when the ADC is idle the ADC will not enter sleep mode before after the next AD conversion.

   Fix/Workaround

Activate the sleep mode in the mode register and then perform an AD conversion.

13.2.5 SPI

1. **SPI Bad Serial Clock Generation on 2nd chip_select when SCBR = 1, CPOL=1 and NCPHA=0**
   When multiple CS are in use, if one of the baudrate equals to 1 and one of the others doesn't equal to 1, and CPOL=1 and CPHA=0, then an additional pulse will be generated on SCK.
   Fix/workaround
   When multiple CS are in use, if one of the baudrate equals 1, the other must also equal 1 if CPOL=1 and CPHA=0.

2. **SPI Disable does not work in Slave mode**
   Fix/workaround
   Read the last received data then perform a Software reset.

3. **SPI RDR.PCS is not correct**
   The PCS (Peripheral Chip Select) field in the SPI RDR (Receive Data Register) does not correctly indicate the value on the NPCS pins at the end of a transfer.
   Fix/Workaround
   Do not use the PCS field of the SPI RDR.

4. **SPI data transfer hangs with CSAAT=1 in CSR0 and MODFDIS=0 in MR**
   When CSAAT=1 in CSR0 and mode fault detection is enabled (MODFDIS=0 in MR), the SPI module will not start a data transfer.
   Fix/Workaround
   Disable mode fault detection by writing a one to MODFDIS in MR.

5. **Disabling SPI has no effect on the TDRE flag**
   Disabling SPI has no effect on TDRE whereas the write data command is filtered when SPI is disabled. This means that as soon as the SPI is disabled it becomes impossible to reset the TDRE flag by writing in the TDR. So if the SPI is disabled during a PDCA transfer, the PDCA will continue to write data in the TDR (as TDRE stays high) until its buffer is empty, and all data written after the disable command is lost.
   Fix/Workaround
   Disable the PDCA, 2 NOP (minimum), disable SPI. When you want to continue the transfer: Enable SPI, enable PDCA.

13.2.6 USART

1. **The NER register always returns zero.**
   Fix/Workaround
   None.

2. **USART - RTS output signal does not function properly in hardware handshaking mode**
   The RTS signal is not generated properly when the USART receives data in hardware handshaking mode. When the Peripheral DMA receive buffer becomes full, the RTS output should go high, but it will stay low.
   Fix/Workaround
   Do not use the hardware handshaking mode of the USART. If it is necessary to drive the RTS output high when the Peripheral DMA receive buffer becomes full, use the normal mode of the USART. Configure the Peripheral DMA Controller to signal an interrupt when the receive buffer is full. In the interrupt handler code, write a one to the RTSDIS bit in the

USART Control Register (CR). This will drive the RTS output high. After the next DMA transfer is started and a receive buffer is available, write a one to the RTSEN bit in the USART CR so that RTS will be driven low.

3. **USART in ISO7816 mode Only in T1: RX impossible after any TX**
   Fix/workaround
   Reset the TX transceiver by setting RSTTX field in CR register, then configure MR register and CR register.

13.2.7 PDCA

1. **PCONTROL.CHxRES is nonfunctional**
   PCONTROL.CHxRES is nonfunctional. Counters are reset at power-on, and cannot be reset by software.
   Fix/Workaround
   Software needs to keep history of performance counters.

2. **Transfer error will stall a transmit peripheral handshake interface.**
   If a tranfer error is encountered on a channel transmitting to a peripheral, the peripheral handshake of the active channel will stall and the PDCA will not do any more transfers on the affected peripheral handshake interface.
   Fix/workaround:
   Disable and then enable the peripheral after the transfer error.

13.2.8 AES

1. **URAD (Unspecified Register Access Detection Status) does not detect read accesses to the write-only KEYW[5..8]R registers**
   Fix/Workaround
   None.

13.2.9 HMATRIX

1. **In the HMATRIX PRAS and PRBS registers MxPR fields are only two bits**
   In the HMATRIX PRAS and PRBS registers MxPR fields are only two bits wide, instead of four bits. The unused bits are undefined when reading the registers.
   Fix/Workaround
   Mask undefined bits when reading PRAS and PRBS.

13.2.10 TWIM

1. **TWIM SR.IDLE goes high immediately when NAK is received**
   When a NAK is received and there is a non-zero number of bytes to be transmitted, SR.IDLE goes high immediately and does not wait for the STOP condition to be sent. This does not cause any problem just by itself, but can cause a problem if software waits for SR.IDLE to go high and then immediately disables the TWIM by writing a one to CR.MDIS. Disabling the TWIM causes the TWCK and TWD pins to go high immediately, so the STOP condition will not be transmitted correctly.
   Fix/Workaround
   If possible, do not disable the TWIM. If it is absolutely necessary to disable the TWIM, there must be a software delay of at least two TWCK periods between the detection of SR.IDLE==1 and the disabling of the TWIM.

13.2.11 MCI

1. **The busy signal of the responses R1b is not taken in account (excepting for CMD12 STOP_TRANSFER).**
   It is not possible to know the busy status of the card during the response (R1b) for the commands CMD7, CMD28, CMD29, CMD38, CMD42, CMD56.
   Fix/Workaround
   The card busy line should be polled through the GPIO pin for commands CMD7, CMD28, CMD29, CMD38, CMD42 and CMD56. The GPIO alternate configuration should be restored after.

13.3 Rev. D

13.3.1 General

1. **3.3V supply monitor is not available on revE.**
   Flash register FGPFRLO[30:29] (FGPFRLO GP29,GP30 and GP31) are reserved and must not be used.
   Fix/workaround
   None.

2. **Service access bus (SAB) can not access DMACA registers.**
   Workaround
   None.

13.3.2 Processor and Architecture

1. **LDM instruction with PC in the register list and without ++ increments Rp**
   For LDM with PC in the register list: the instruction behaves as if the ++ field is always set, ie the pointer is always updated. This happens even if the ++ field is cleared. Specifically, the increment of the pointer is done in parallel with the testing of R12.
   Fix/Workaround
   None.

2. **RETE instruction does not clear SREG[L] from interrupts.**
   The RETE instruction clears SREG[L] as expected from exceptions.
   Fix/Workaround
   When using the STCOND instruction, clear SREG[L] in the stacked value of SR before returning from interrupts with RETE.

3. **Exceptions when system stack is protected by MPU**
   RETS behaves incorrectly when MPU is enabled and MPU is configured so that system stack is not readable in unprivileged mode.
   Fix/Workaround
   Workaround 1: Make system stack readable in unprivileged mode,
   or
   Workaround 2: Return from supervisor mode using rete instead of rets. This requires :
   1. Changing the mode bits from 001b to 110b before issuing the instruction.
   Updating the mode bits to the desired value must be done using a single mtsr instruction so it is done atomically. Even if this step is described in general as not safe in the UC technical reference guide, it is safe in this very specific case.
   2. Execute the RETE instruction.

4. **Multiply instructions do not work on RevD.**

All the multiply instructions do not work.
Fix/Workaround
Do not use the multiply instructions.

5. **Hardware breakpoints on MAC instructions may corrupt the destination registerof the MAC instruction.**
Fix/Workaround
Place breakpoints on earlier or later instructions.

13.3.3 MPU

1. **Privilege violation when using interrupts in application mode with protected system stack**
If the system stack is protected by the MPU and an interrupt occurs in application mode, an MPU DTLB exception will occur.
Fix/Workaround
Make a DTLB Protection (Write) exception handler which permits the interrupt request to be handled in privileged mode.

13.3.4 ADC

1. **Sleep Mode activation needs additional A to D conversion**
If the ADC sleep mode is activated when the ADC is idle the ADC will not enter sleep mode before after the next AD conversion.

Fix/Workaround
Activate the sleep mode in the mode register and then perform an AD conversion.

13.3.5 SPI

1. **SPI Bad Serial Clock Generation on 2nd chip_select when SCBR = 1, CPOL=1 and NCPHA=0**
When multiple CS are in use, if one of the baudrate equals to 1 and one of the others doesn't equal to 1, and CPOL=1 and CPHA=0, then an additional pulse will be generated on SCK.
Fix/workaround
When multiple CS are in use, if one of the baudrate equals 1, the other must also equal 1 if CPOL=1 and CPHA=0.

2. **SPI Disable does not work in Slave mode**
Fix/workaround
Read the last received data then perform a Software reset.

13.3.6 TWI

1. **TWIM Version Register is zero**
TWIM Version Register (VR) is zero instead of 0x100.
Fix/Workaround
None.

13.3.7 USART

1. **The NER register always returns zero.**
Fix/Workaround:
None.

2. **USART - RTS output signal does not function properly in hardware handshaking mode**
   The RTS signal is not generated properly when the USART receives data in hardware handshaking mode. When the Peripheral DMA receive buffer becomes full, the RTS output should go high, but it will stay low.
   Fix/Workaround
   Do not use the hardware handshaking mode of the USART. If it is necessary to drive the RTS output high when the Peripheral DMA receive buffer becomes full, use the normal mode of the USART. Configure the Peripheral DMA Controller to signal an interrupt when the receive buffer is full. In the interrupt handler code, write a one to the RTSDIS bit in the USART Control Register (CR). This will drive the RTS output high. After the next DMA transfer is started and a receive buffer is available, write a one to the RTSEN bit in the USART CR so that RTS will be driven low.

3. **USART in ISO7816 mode Only in T1: RX impossible after any TX**
   Fix/workaround
   Reset the TX transceiver by setting RSTTX field in CR register, then configure MR register and CR register.

13.3.8 PDCA

1. **PCONTROL.CHxRES is nonfunctional**
   PCONTROL.CHxRES is nonfunctional. Counters are reset at power-on, and cannot be reset by software.
   Fix/Workaround
   Software needs to keep history of performance counters.

13.3.9 AES

1. **URAD (Unspecified Register Access Detection Status) does not detect read accesses to the write-only KEYW[5..8]R registers**
   Fix/Workaround
   None.

14. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

14.1 Rev. C – 03/10

1. Updated the datasheet with new revision G features.

14.2 Rev. B – 08/09

1. Updated the datasheet with new device AT32UC3A4.

14.3 Rev. A – 03/09

1. Initial revision.