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Advanced Information
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T138AF Video Display Controller

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1 Introduction

1.1 Features

- **Cost Effective Highly Integrated Triple ADC + ITU656/601 Decoder + digital RGB + 2D Video Decoder + 8051 + OSD + Scalar + Keystone + TCON + TTL/DAC + DC-to-DC + LED/CCFL controls**
  - Integrates 10-bit Triple Analog to Digital Converters (ADC) & Phase Locked Loop (PLL), for supporting CVBS, S-Video, YPbPr(480i) and RGB inputs
  - Scaler supports 2-D adaptive intra-field de-interlacer and non-linear 16:9 aspect ration.
  - Requires no external Frame Buffer Memory for de-interlace.
  - Integrate ITU656/601_8/L601_16 Decoder
  - Support digital RGB565/666/888 inputs
  - Built-in 8051 MCU
  - Advanced On Screen Display (OSD) function
  - Programmable Timing Controller (TCON) most panel interfaces
  - Multi-standard color decoder with 2D adaptive comb filter
  - Innovative and flexible design to reduce total system cost
- **Triple 10-bits ADCs**
  - 80MSPS Conversion Rate ADC
  - Built-in Pre-amp, mid-level & ground clamp
  - Automatic Clamp Control for CVBS, Y and C
  - Programmable Static Gain Control or Automatic Gain Control for CVBS or Y/C
  - Max Input configuration up to 6xCVBS, 3xS-video
  - Build-in Line-Lock PLL for RGB and YPbPr.
  - Phases Tracking and Boundary for adjusting input quality.
  - RGB input resolution supported up-to SXGA
- **Digital Video Enhancement**
  - Separate Luminance and Chroma Enhancer
  - Y (Luma) Supports Luminance BLE/WLE, DLTi., Contrast and Brightness adjustment
  - C (Chroma) Supports DCTI, Saturation and Hue adjustment.
- **FIR Based Advanced Scaling Engine**
  - Coefficient based sharpness filters
  - Independent vertical and horizontal scaling
  - 16:9 Non-linear Aspect ratio
  - Keystone adjustment
- **Crystal Oscillator Circuit**
  - Direct interface to a (27.0MHz) Crystal
  - Also provide a buffered clock output for external Micro-controller
- **LCD Interface**
  - Provides 3x256 Gamma correction for panel compensation
  - Supports image pan functions
  - Programmable Timing Controller
  - Built-in software adjustable VCOM voltage
  - RGB Triple DAC and/or 24-bit TTL output
  - Integrated high efficiency DC-DC power conversion unit for gate and source drivers reduces energy consumption
  - Integrated TFT-LCD backlight inverter drive unit supports LED typed backlight
  - Software adjustable lamp dimming
  - Output(LCD) resolution support up-to XGA
- **Built-in On Screen Display Engine**
  - 8K/16K/24K-word OSD1 and 8K/16K-word OSD2 memory
  - Supports text or bitmap modes
  - Supports character blinking and overlay functions
  - Fully programmable character mapping
  - Supports alpha blending & Zoom-in/Zoom-out function
  - Built-in 114+ fonts (18x12, 24x16 each)
  - Pattern-Filled background
  - Optional fonts stored in off-chip serial ROM
- **Digital Test Pattern Generator**
  - Programmable standard & special panel burn-in test patterns
  - Support special border frame blocking mode
- **Misc.**
  - Supports 2-wire I^2C (Slave/Master)
  - Supports external SPI flash ROM with Cache
  - Supports free run OSD mode
  - Supports SAR*4
  - Supports Touch Panel I/F
  - Pulse Width Modulation Outputs
  - General Purpose Input/Output (GPIO)
  - Built-in 8051 MCU with Cache and expanded access buffers.
- **Power Supply: +1.8V, +3.3V and +5V**
- **Package: 128-pin LQFP**

1.2 General Description

The T138AF is a highly integrated All-in-one Visual Processor that provides major cost saving solution for the portable applications. T138AF has built-in high performance Triple ADCs, TCON, triple DACs output and/or 24-bits TTL output. Scaling Machine with sophisticated upscaling and downscaling algorithms. The Innovative integrated "Frame-Buffer-Less" De-interlacer can significantly reduce system cost. The T138AF also integrates enhanced two layer OSD engines. The device can interface to an external micro-controller through 2-wire serial bus interface or use internal MCU (8051) with ROM code in external SPI Flash ROM. It supports smooth keystone scaling for projector

1.3 Applications

1. Small to medium sized displayer, In-car TV
2. Video Door Phone
3. Digital Photo Frame
4. Projector

1.4 System Architecture

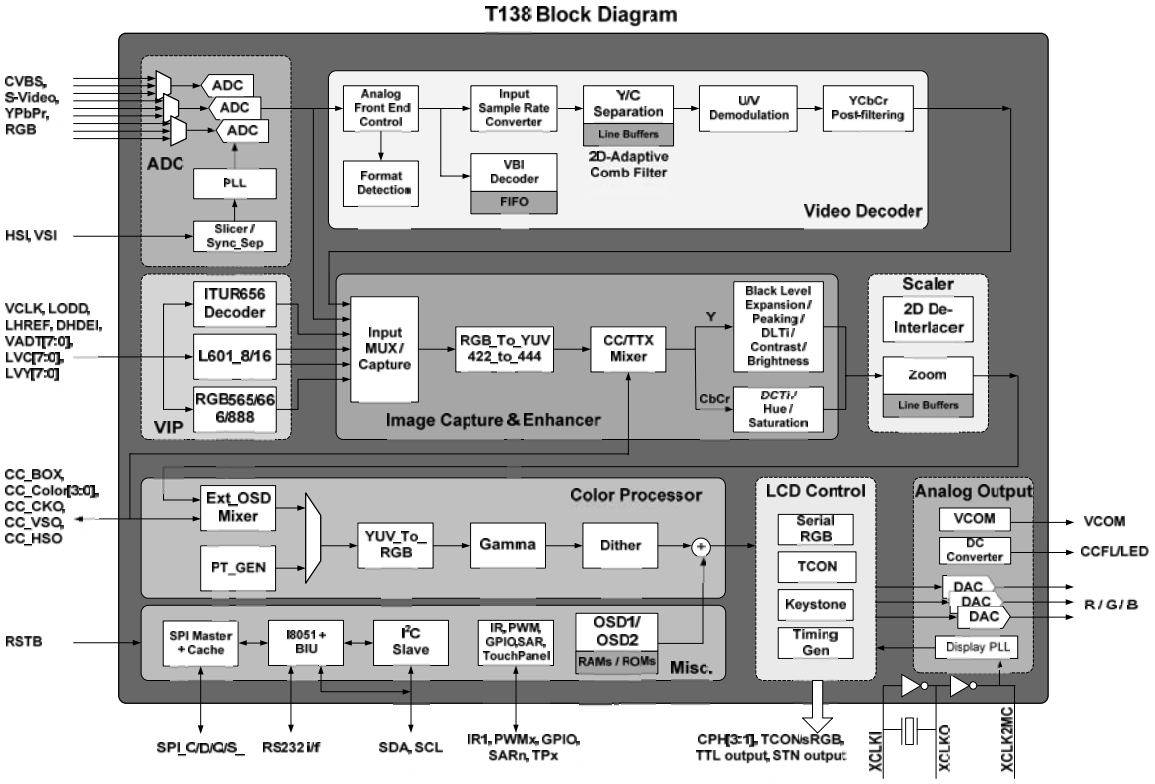


Figure 1-1 System Architecture

1.5 System Configurations

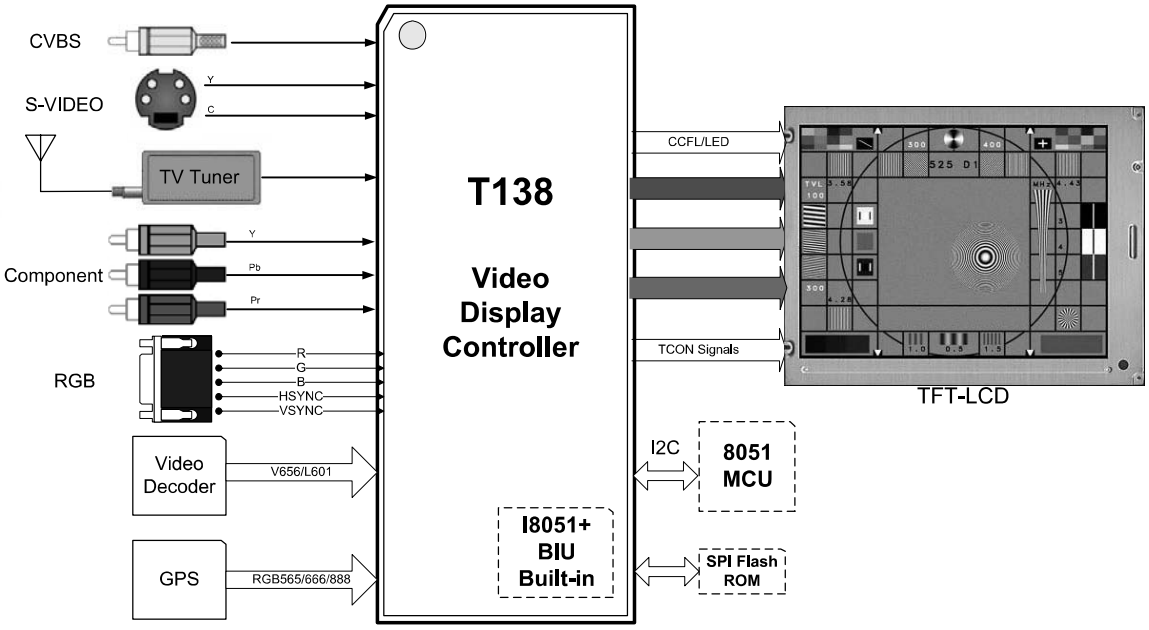


Figure 1-2 System Configurations

1.6 Pinout Diagram

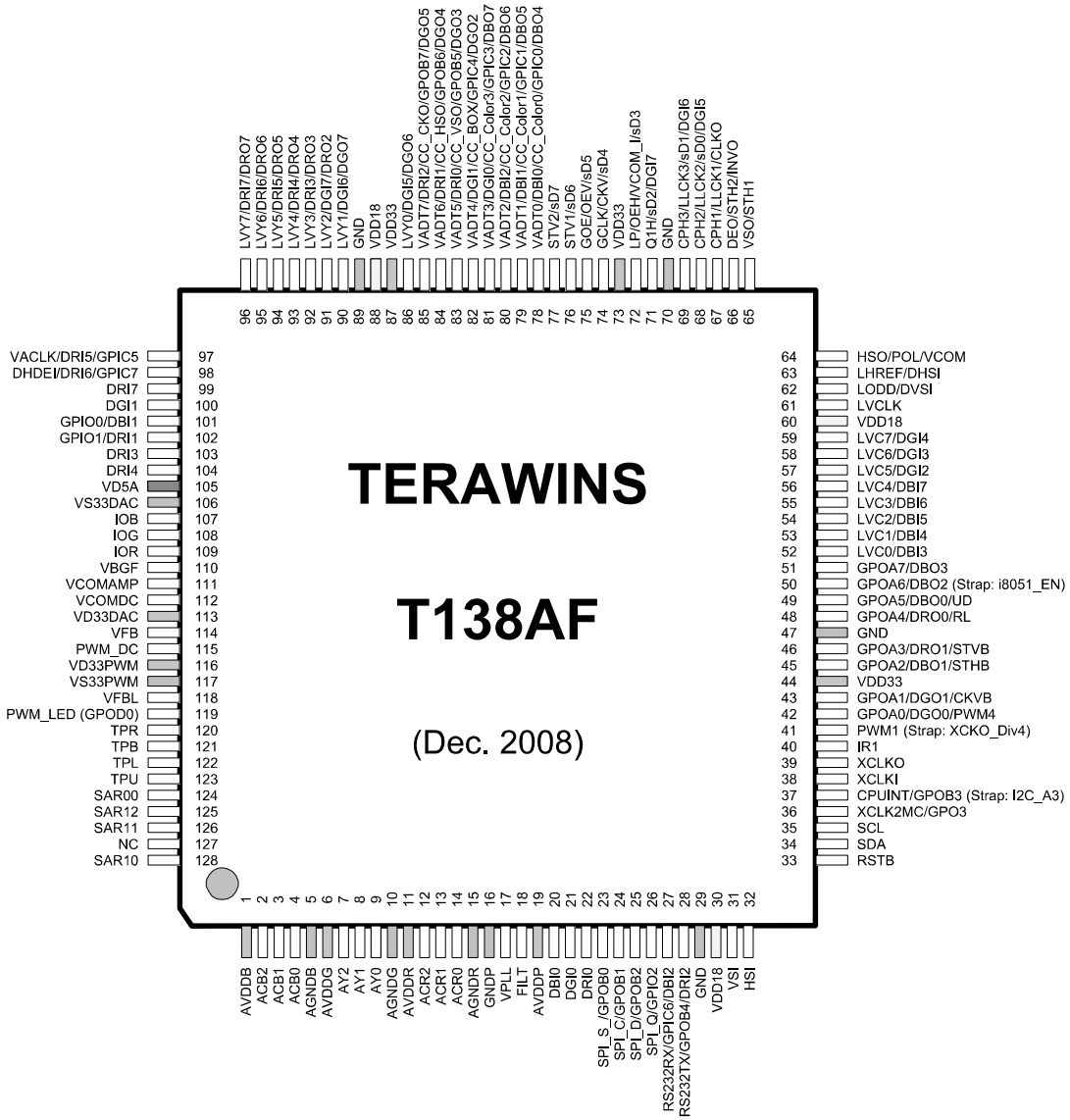


Figure 1-3 T138AFF Pinout Diagram

1.7 Pin Description

Table 1-1 T138AFF Pin Description

Symbol	Pin #	Type	Description
Power Supplies			
VDD18	30, 60, 88	PWR	+1.8V digital core power supply
VDD33	44, 73, 87	PWR	+3.3V digital output power supply
AVDDB	1	PWR	+3.3V analog power supply for ADC channel 2
AVDDG	6	PWR	+3.3V analog power supply for ADC channel 1
AVDDR	11	PWR	+3.3V analog power supply for ADC channel 0
VD5A	105	PWR	+5.0V analog power supply for DAC
VD33DAC	113	PWR	+3.3V analog power supply for DAC
VD33PWM	116	PWR	+3.3V analog power supply for DC Converter
AVDDP	19	PWR	+3.3V analog power supply for PLL
GND	29, 47, 70, 89	GND	Digital ground
AGNDB	5	GND	Analog ground for ADC channel 2
AGNDG	10	GND	Analog ground for ADC channel 1
AGNDR	15	GND	Analog ground for ADC channel 0
VS33DAC	106	GND	Analog ground for DAC
VS33PWM	117	GND	Analog ground for DC Converter
GNDP	16	GND	Analog ground for PLL
Output Interface Signals			
IOR	109	AO	Channel R current output
IOG	108	AO	Channel G current output
IOB	107	AO	Channel B current output
VCOMAMP	111	AO	VCOM output
VCOMDC	112	AO	VCOM output
VCOM_i	72	DI, P/D	VCOM input
LLCk1	67	DO, P/D	Output Data Clock
LLCk2	68	DO, P/D	Output Data Clock
LLCk3	69	DO, P/D	Output Data Clock
Timing Controller Interface Signals			
POL/VCOM	64	DO, P/D	Horizontal Polarity Output Signal. Share w/ HSO
STH1	65	DO, P/D	Horizontal Start Pulse 1 Signal. Share w/ VSO
STH2	66	DO, P/D	Horizontal Start Pulse 2 Signal. Share w/ DEO
Q1H	71	DO, P/D	Panel polarity control
LP/OEH	72	DO, P/D	Latch pulse for column driver
GCLK/CKV	74	DO, P/D	Gate driver clock
GOE/OEV	75	DO, P/D	Gate driver output enable
STV1	76	DO, P/D	Gate driver start pulse
STV2	77	DO, P/D	Gate driver start pulse
CKVB	43	DO, P/D	Inverse output of gate driver clock
STHB	45	DO, P/D	Inverse output of horizontal start pulse
STVB	46	DO, P/D	Inverse output of gate driver start pulse
UD	49	DO, P/D	Panel UP/Down Control
RL	48	DO, P/D	Panel Right/Left Control

Symbol	Pin #	Type	Description
Power Management Signals			
VFB	114	AI	Feedback of DC-DC current
VPWM (PWM_DC)	115	AO	PWM output, connect o external N-channel power MOSFET
VFBI/VFBL	118	AI	Feedback of Lamp current
VPWMP/PWM_LED	119	AO	PWM output, drive PMOSFET switch
Parallel Panel TTL Interface Signals			
CLKO	67	DO, P/D	Pixel clock
DRO[7:0]	96~91, 46, 48	DO, P/D	Red channel output data
DGO[7:0]	90, 86~82, 43~42	DO, P/D	Green channel output data
DBO[7:0]	81~78, 51~50, 45, 49	DO, P/D	Blue channel output data
Serial Panel Interface Signals			
VSO	65	DO, P/D	Vertical Synchronization Output Control Signal. Share w/ STH1
HSO	64	DO, P/D	Horizontal Synchronization Output Control Signal. Share w/ POL/VCOM
DEO	66	DO, P/D	Horizontal Output Data Enable Signal. Share w/ STH2
CLKO	67	DO, P/D	sPanel clock
sD0~sD7	68, 69,71, 72,74~77	DO, P/D	sPanel data, share w/ TCON signals
Touch Panel and SAR ADC Signals			
TPR	120	AIO	Touch Panel Right sense/control
TPB	121	AIO	Touch Panel Bottom sense/control
TPL	122	AIO	Touch Panel Left sense/control
TPU	123	AIO	Touch Panel Upper sense/control
SAR00	124	AI	SAR ADC input 00 (for keypads sense)
SAR12	125	AI	SAR ADC input 12
SAR11	126	AI	SAR ADC input 11
SAR10	128	AI	SAR ADC input 10
Configuration Interface Signals			
SPI_CSB	23	DIO, P/U	Chip select to SPI Flash ROM (active low)
SPI_CLK	24	DIO, P/D	Clock to SPI Flash ROM
SPI_D	25	DIO, P/D	Output data to SPI Flash ROM
SPI_Q	26	DIO, P/U	Input data from SPI Flash ROM
RSTB	33	DI, P/U	Whole chip reset.
SDA	34	DIO, P/U	2-wire serial bus data. Power down does not affect SDA.
SCL	35	DIO, P/U	2-wire serial bus clock. Power down does not affect SCL. This pin should be high when RSTB asserted for avoid entering Scan test mode.
XCLK2MC	36	DO	Buffered XCLKI for external microprocessor.
CPUINT (A3)	37	DIO, P/U	Internal Interrupt. This pin is a reset strap pin for I^2C device address. When RSTB goes high, if this pin is high, then default I^2C device address is 50h, else 40h.
ADC, PLL, Slicer Interface			
ACB2	2	AI	Analog input 2 of channel 2
ACB1	3	AI	Analog input 1 of channel 2
ACB0	4	AI	Analog input 0 of channel 2

Symbol	Pin #	Type	Description
AY2	7	AI	Analog input 2 of channel 1
AY1	8	AI	Analog input 1 of channel 1
AY0	9	AI	Analog input 0 of channel 1
ACR2	12	AI	Analog input 2 of channel 0
ACR1	13	AI	Analog input 1 of channel 0
ACR0	14	AI	Analog input 0 of channel 0
VSI	31	DI, P/D	RGB Vertical Synchronous input
HSI	32	DI, P/U	RGB Horizontal Synchronous input
VPLL	17	AI	PLL Reference
FILT	18	AI	PLL filter
Video-In Interface: A656			
VADT0~7	78~85	DI, P/D	Video data port of the 1st ITU-656 input port
VACLK	97	DI, P/D	Video clock of the 1st ITU-656 (2x pixel rate)
Video-In Interface: B656			
LVC0~7	52~59	DI, P/D	Video data port of the 2nd ITU-656
LVCLK	61	DI, P/D	Video clock of the 2nd ITU-656 (2x pixel rate)
Video-In Interface: L601_8bit			
LVC0~7	52~59	DI, P/D	Video data port of 8-bit 601 or Chroma
LVCLK	61	DI, P/D	Video clock (2x pixel rate)
LODD/LVSYNC	62	DI, P/D	ITU-601 Odd or VSync input
LHREF/LHSYNC	63	DI, P/D	ITU-601 HREF(HDE) or HSync input
Video-In Interface: L601_16bit			
LVC0~7	52~59	DI, P/D	Video chroma data port of 16-bit 601
LVY0~7	86, 90~96	DI, P/D	Video Luma data port of 16-bit 601
LVCLK	61	DI, P/D	Video clock (1x pixel rate)
LODD/LVSYNC	62	DI, P/D	ITU-601 Odd or VSync input
LHREF/LHSYNC	63	DI, P/D	ITU-601 HREF(HDE) or HSync input
Video-In Interface: RGB565, RGB666, RGB777, RGB888 When NO TTL output			
DRI3~7	92~96	DI, P/D	Digital RGB input: 5 MSB bits of Color R
DGI2~7	57~59, 86, 90~91	DI, P/D	Digital RGB input: 6 MSB bits of Color G
DBI3~7	52~56	DI, P/D	Digital RGB input: 5 MSB bits of Color B
LVCLK	61	DI, P/D	Video clock (1x pixel rate)
DVSI	62	DI, P/D	Digital RGB VSync input
DHSI	63	DI, P/D	Digital RGB HSync input
DHDEI	98	DI, P/D	Digital RGB Horizontal Data Enable input (optional)
DRI0~2	83~85	DI, P/D	Digital RGB input: 3 LSB bits of Color R
DGI0~1	81, 82	DI, P/D	Digital RGB input: 2 LSB bits of Color G
DBI0~2	78~80	DI, P/D	Digital RGB input: 3 LSB bits of Color B
Video-In Interface: RGB565, RGB666, RGB888 When TTL output			
DRI0~7	22, 102, 28, 103~104, 97~99	DI, P/D	Digital RGB input: 7 MSB bits of Color R
DGI0~7	21, 100, 57~59, 68~69, 71	DI, P/D	Digital RGB input: 7 MSB bits of Color G
DBI0~7	20, 101, 27, 52~56	DI, P/D	Digital RGB input: 7 MSB bits of Color B
LVCLK	61	DI, P/D	Video clock (1x pixel rate)
DVSI	62	DI, P/D	Digital RGB VSync input
DHSI	63	DI, P/D	Digital RGB HSync input

Symbol	Pin #	Type	Description
DHDEI	98	DI, P/D	Digital RGB Horizontal Data Enable input (optional)
General Purpose Input Output Signals			
GPIO0~2	101~102, 26	DIO, P/U	GPIO port, direction: input/output/Open-Drain
GPO3	36	DO	GPO3 port, for output control
GPOA0~5, GPOA6 (i8051_En), GPOA7	42, 43, 45, 46, 48~51	DO, P/D	GPOA port, for output controls. GPOA6 is a reset strap pin for enabling internal 8051 or not. When RSTB goes high, if this pin is high, the internal 8051 is enabled; else disabled.
GPOB0~7	23~25, 37, 28, 83~85	DO, P/D	GPOB port, for output controls.
GPIC0~7	78~82, 97, 27, 98	DI, P/D	GPIC port, for input controls
GPOD0	119	DO, P/D	GPOD port, for output control
CC/Ext_OSD Mixer interface Signals			
CC_CKO	85	DIO, P/D	Operation clock output for Closed Caption or External OSD
CC_HSO	84	DIO, P/D	Horizontal Position reference output for Closed Caption or External OSD
CC_VSO	83	DIO, P/D	Vertical Position reference output for Closed Caption or External OSD
CC_BOX	82	DIO, P/D	The input active window (BOX) of Closed Caption or External OSD Mixer
CC_Color0~3	78~81	DIO, P/D	The input color of Closed Caption or External OSD Mixer
Misc. Signals			
XCLKI	38	DI	Output PLL reference clock input and I2C, timer operating clock
XCLKO	39	DO	Output PLL reference clock output
RS232RX	27	DI, P/U	RS232 Receiving signal
RS232TX	28	DO, P/U	RS232 Transmitting signal
IR1	40	DI, P/U	IR input
PWM1	41	DIO, P/D	Pulse Width Modulation 1 for backlight control / Volume / …
PWM4	42	DIO, P/D	Pulse Width Modulation 2 for backlight control / Volume / …
VBGF	110	AI	DAC voltage reference output

2 Theory of Operations

2.1 I²C Command Protocol

Before your tester writes I²C commands to T138, slave address must be set at 50h. The timing sequence can be shown as below. After 4 cycles, the tester can get started IIC commands. CPUINT(A3) can affect slave address. Set it low for 40h, and high for 50h.

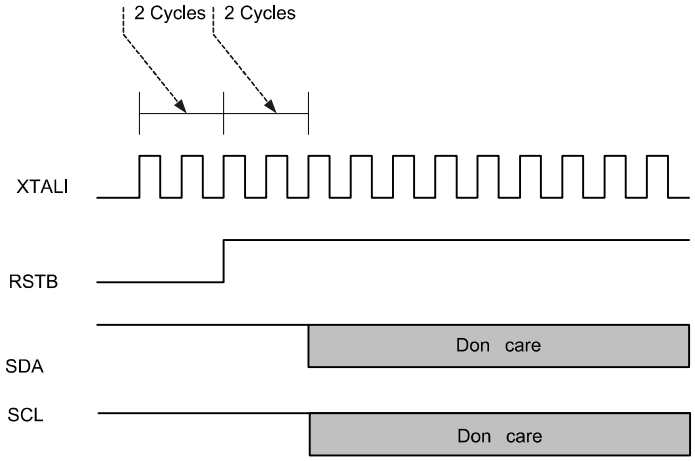


Figure 2-1 Power-Up Initialization

When tester issues commands to the T138, the only way the user can program the T138 is using the 2-wire serial bus protocol. This section describes the 2-wire serial bus protocol. Data transfers on the 2-wire serial bus are initiated with a START condition and are terminated with a STOP condition. Normal data on the SDA line must be stable during the high period of the SCL. The transition on the SDA is only allowed while SCL is low. The START condition is unique case and is defined by a high-to-low transition on the SDA while the SCL is high. The STOP condition is a unique case and is defined by a low-to-high transition on the SDA while the SCL is high. Each data packet on the 2-wire serial bus consists of 8 bits of data followed by an ACK bit. Data is transferred with MSB first. The transmitter releases the SDA line during the ACK bit and the receiver of data transfer must drive the SDA line low during the ACK bit to acknowledge receipt of the data. The frequency of SCL can be from 50 KHz up to 1 MHz.

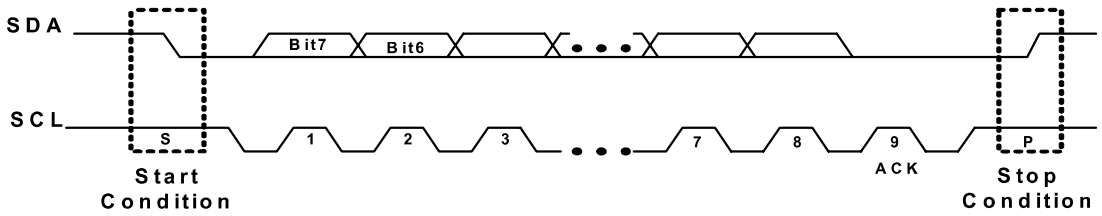


Figure 2-2 Basic I²C Bus Protocol

The timing below shows a typical T138 I²C single byte write command,

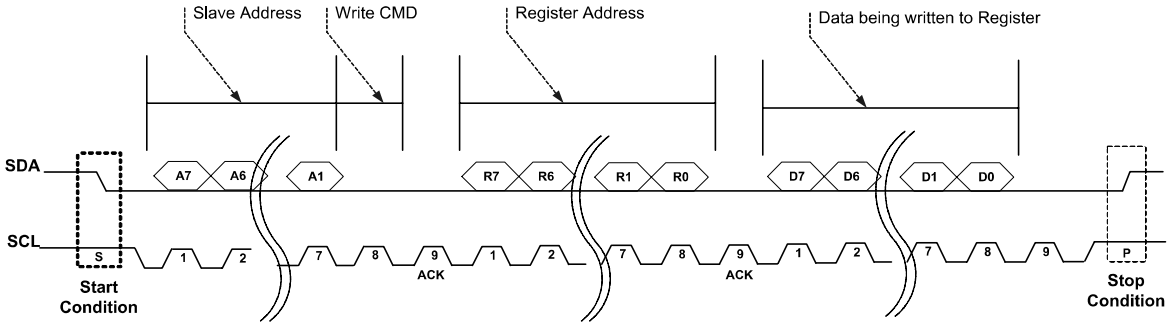


Figure 2-3 T138 I²C Single Byte Write Command

The timing below shows a typical T138 I²C single byte read command,

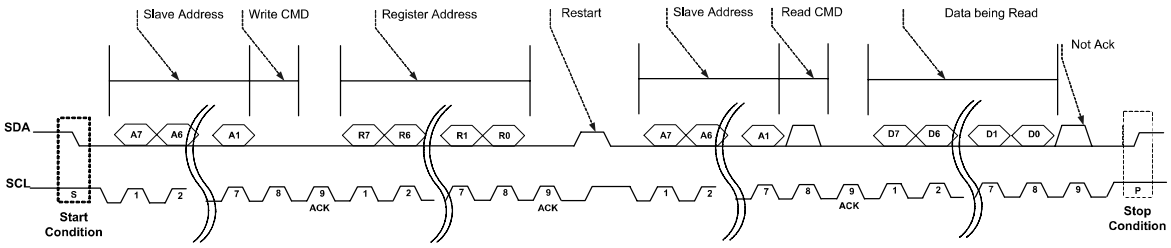


Figure 2-4 T138 I²C Single Byte Write Command

2.2 Analog Front End

T138 contains 3 ADCs in Analog Front End. Each channel of ADCs can digitalize SDTV signals from analog to digital. The figure shown below can describe how to select a SDTV signal from 3 inputs prior to ADC.

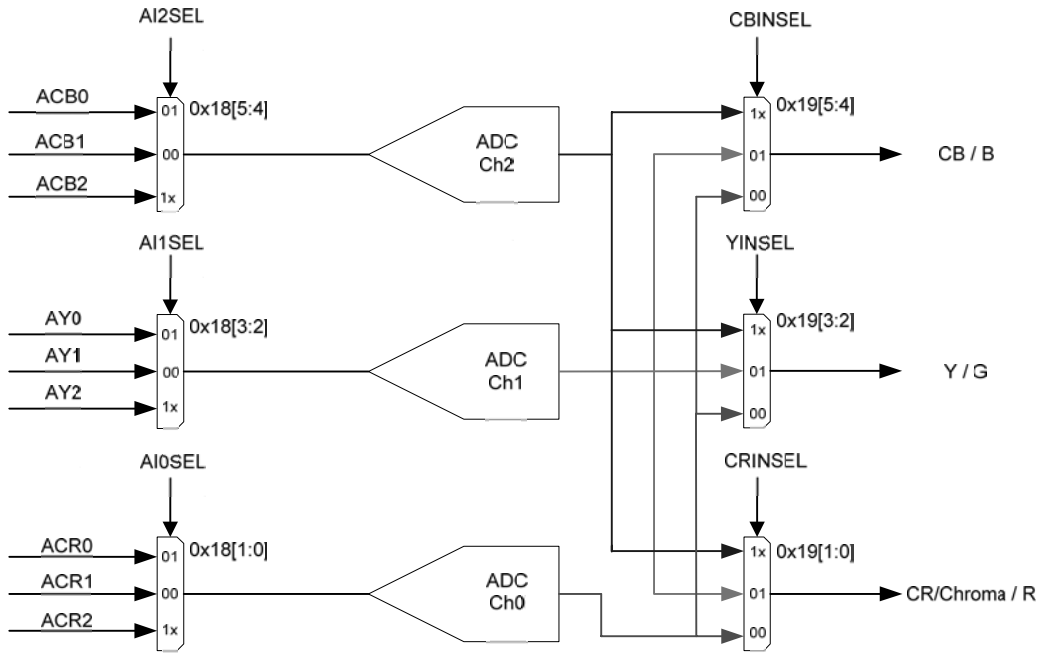


Figure 2-5 Analog Front End MUX

2.3 Y/C Separation and Chroma Decoder

A composite video has luma(Y) and chromal information mixed in the same video signal. This video signal can also be represented by the equation below,

$$CVBS = Y + U * Sin(wt) + V * \cos(wt)$$

Where $w = 2\pi f_{SC}$, f_{SC} =3.58Mhz if NTSC, f_{SC} =4.43Mhz if PAL

The figure below shows a typical composite signal. The 2-D adaptive comb filter inside T138 is designed to separate Y and C from a composite video signal.

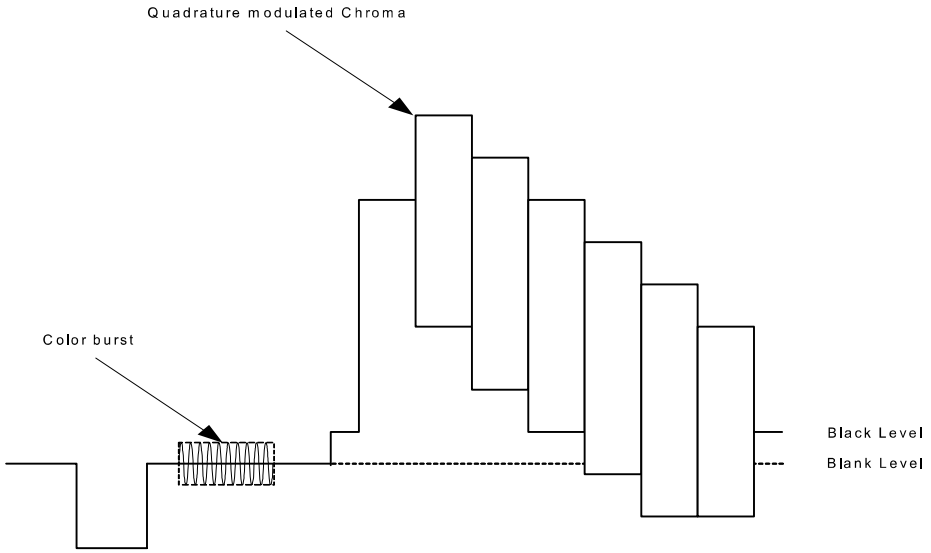


Figure 2-6 CVBS Input

. The conventional 3-line comb filter fails to separate Y and C if there is a vertical transition. The 2-D adaptive comb filter is based on equally weighting factors that color changes along vertical and horizontal edges. Let the amount of color change along vertical and horizontal direction DCv and DCh, the weighting factor can be expressed as following equations,

$$Wh = \frac{DCv}{DCv + DCh}$$
$$Wv = \frac{DCh}{DCv + DCh}$$

By employing adaptive method, chroma can be recovered by following equation,
$C = Ch * Wh + Cv * Wv$

After Y/C separation, Y and C should look like waveforms shown as in following figure. Y only contains low frequency part, while C contains high frequency part that is centered around sub-carrier f_{SC}.

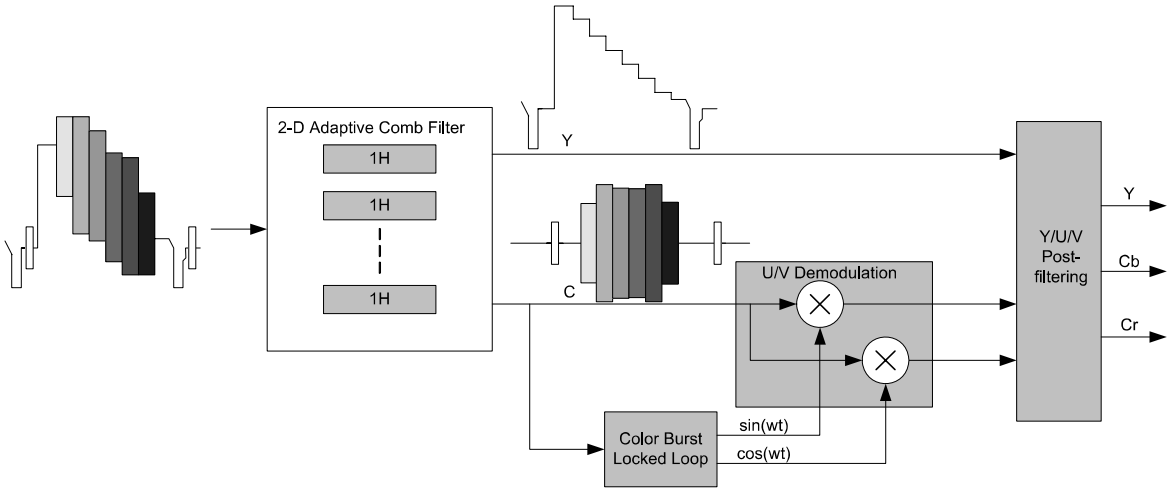


Figure 2-7 Separate Y/Cb/Cr

2.4 Digital Color Transient Improvement (DCTI)

Usually, a composite or S-video SDTV signal may have bandwidth limitation that causes the loss chroma detail around two different color bars. Two pictures shown below illustrate the result before and after DCTI block. Without DCTI(the upper picture), we may see color transient wider than several pixels. A slow transient edge usually blurs image. T138 DCTI algorithm can sharpen those color transient edges. The lower picture shows that chroma data is enhanced by increasing the slope of edge transient without introducing the ring effects.

Figure 2-8 DCTI

2.5 Black-Level Extension (BLE)

Black Level Expansion (BLE) can enhance image contrast that makes dark regions of image darker, while bright regions remain unchanged. The figure shown below is BLE transfer function.

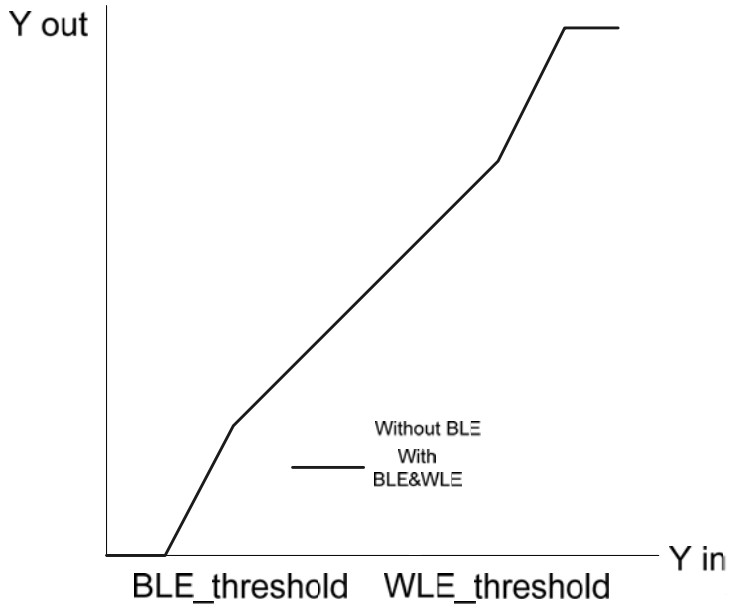


Figure 2-9 Black Level and White Level Extension

$$Yout = Yin - (BLE\_Yoffset - Yin) * BLE\_Gain / 16, \text{ while } Yin < BLE\_Threshold$$

$$Yout = Yin + (Yin - WLE\_Yoffset) * WLE\_Gain / 16, \text{ while } Yin > BLE\_Threshold$$

Where $BLE\_Yoffset$ and BLE_Gain could be programmed by register P0_6Fh; $WLE\_Yoffset$ and WLE_Gain could be programmed by register P0_6Fh and P0_64h respectively.

2.6 Color Space Converter

A pixel in YcbCr color space can be converted to RGB color space by using following equations,

$$R = YCoef\_R * (Y - 16) + /- CbCoef\_R * (Cb - 128) + CrCoef\_R * (Cr - 128)$$

$$G = YCoef\_G * (Y - 16) - CbCoef\_G * (Cb - 128) - CrCoef\_G * (Cr - 128)$$

$$B = YCoef\_B * (Y - 16) + CbCoef\_B * (Cb - 128) + /- CrCoef\_B * (Cr - 128)$$

The equations shown as below correspond to a typical YcbCR-to-RGB converter.

2.7 FIR Scalar

FIR Scaler can scale input H/V sizes to fit any LCD panel resolution. The flexible and independent H/V scalers allow users to program display area in 16:9 Full mode, 16:9 non-linear wide mode and 4:3 mode. FIR scaler also provides coefficient-based 2-D sharpness that can sharpen detail of picture.

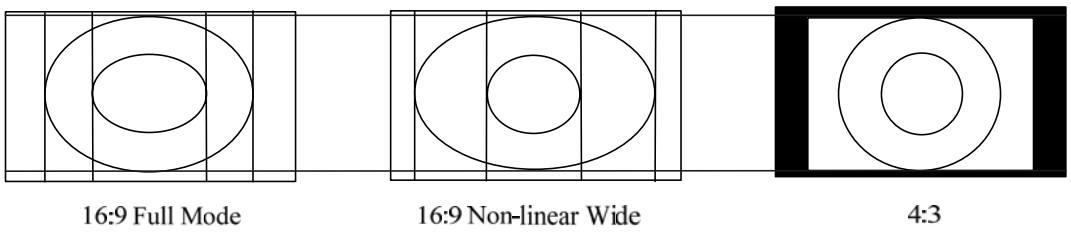


Figure 2-10 Aspect Ratio Adjusting

2.8 Gamma Correction

The relation between input video signal and LCD panel may exist non-linear transfer function such as figure shown below,

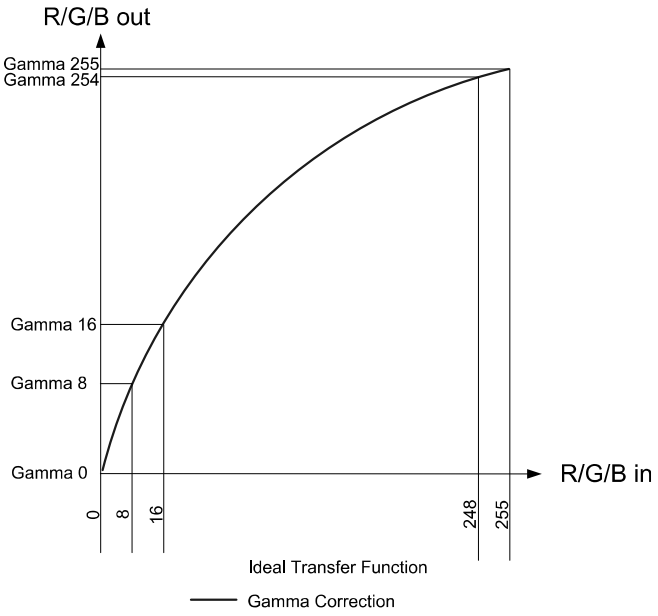


Figure 2-11 Gamma LUT

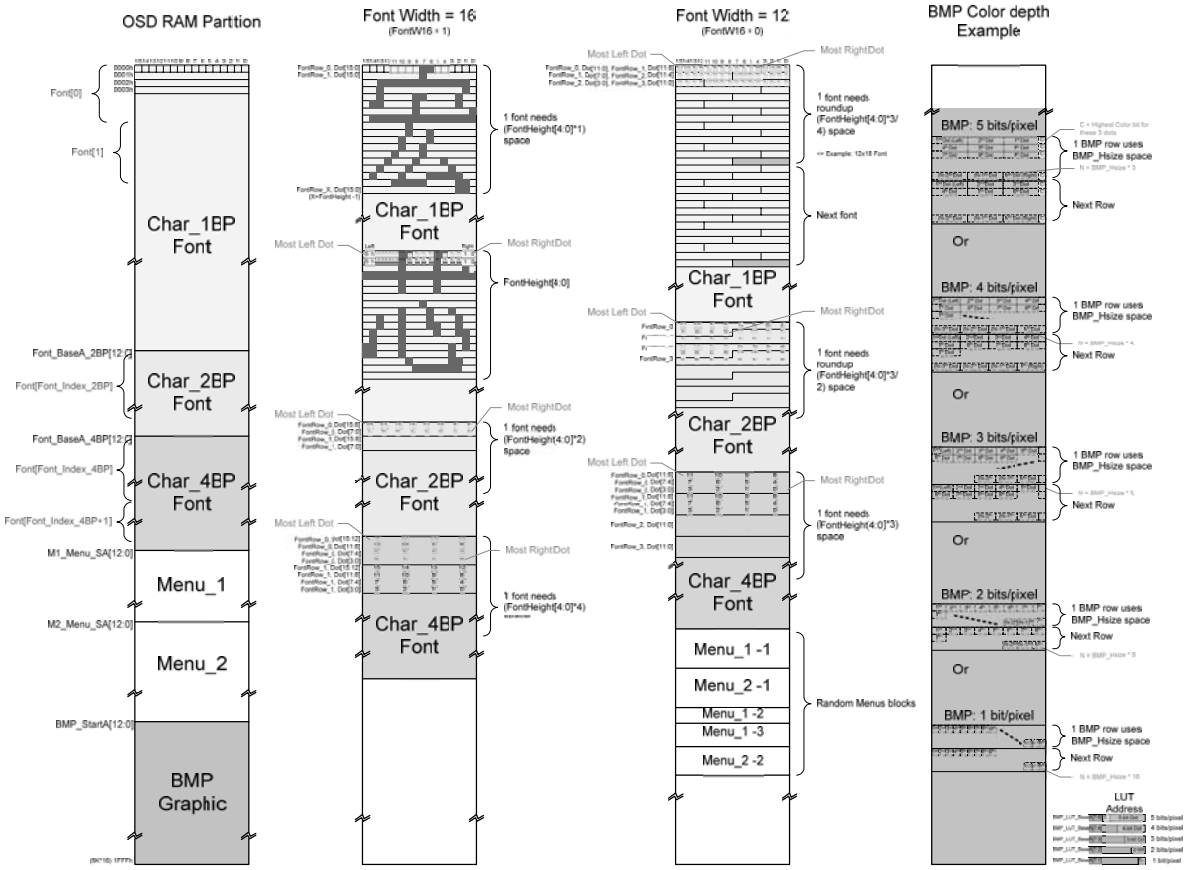
T138AF uses 256-entries for point-to-point gamma LUTs. Each point can be programmed via register at P0_93h and P0_94h.

2.9 OSD1

The OSD1 in T138 is improved in rendering and efficient memory usage. The legacy OSD is either one thread Menu or one graphic (BMP) mode. T138 OSD1 supports two threads menus and 1 graphic rendering simultaneously. So it will be easier to have menu control and Closed Caption.

2.9.1 OSD1 RAM Partition

The OSD1 Font/Menus/BMP memory share the same built-in 8Kx16 or 16Kx16 or 24Kx16 SRAM, depends on bonding option.



2.9.2 OSD1 Register Map

I/O Port	Groups	Index	Description
A0h – OSD1_Index A1h – OSD1_Data	Global Setting	00h	OSD1 Enable/Blinking Register
		01h	Font Size
		02h	Char2BP Font Index Base
		03h	Char4BP Font Index Base
		04h	Char2BP Font Memory Base Address, LSB
		05h	Char2BP Font Memory Base Address, MSB
		06h	Char4BP Font Memory Base Address, LSB
		07h	Char4BP Font Memory Base Address, MSB
		08h	OSD1 Color LUT Address port
		09h	OSD1 Color LUT Data Port
		0Ah	OSD1 Window Shadow
		0Bh	Global Alpha Blending Control
		0Ch	Char1BP color high bits offset
		0Dh	ROM Font Index Base
		0Fh	Revision ID
	Menu-1 Setting	10h	Menu-1 Enable
		11h	Menu-1 Start Address, LSB
		12h	Menu-1 Start Address, MSB
		13h	Menu-1 End Address, LSB
		14h	Menu-1 End Address, MSB
	ROM Font	16h	ROM Font Memory Base Address, LSB
		17h	ROM Font Memory Base Address, MSB
	Menu-2 Setting	18h	Menu-2 Enable
		19h	Menu-2 Start Address, LSB
		1Ah	Menu-2 Start Address, MSB
		1Bh	Menu-2 End Address, LSB
		1Ch	Menu-2 End Address, MSB
	BMP Setting	20h	BMP Control Register
		21h	BMP Start Address, LSB
		22h	BMP Start Address, MSB
		23h	BMP Alpha Blending Control
		24h	BMP Horizontal Size, LSB
		25h	BMP Horizontal Size, MSB
		26h	BMP Vertical Size, LSB
		27h	BMP Vertical Size, MSB
		28h	BMP Position, Horizontal Start, LSB
		29h	BMP Position, Horizontal Start, MSB
		2Ah	BMP Position, Vertical Start, LSB
		2Bh	BMP Position, Vertical Start, MSB
		2Ch	BMP LUT Base Address
		2Dh	BMP Background Color

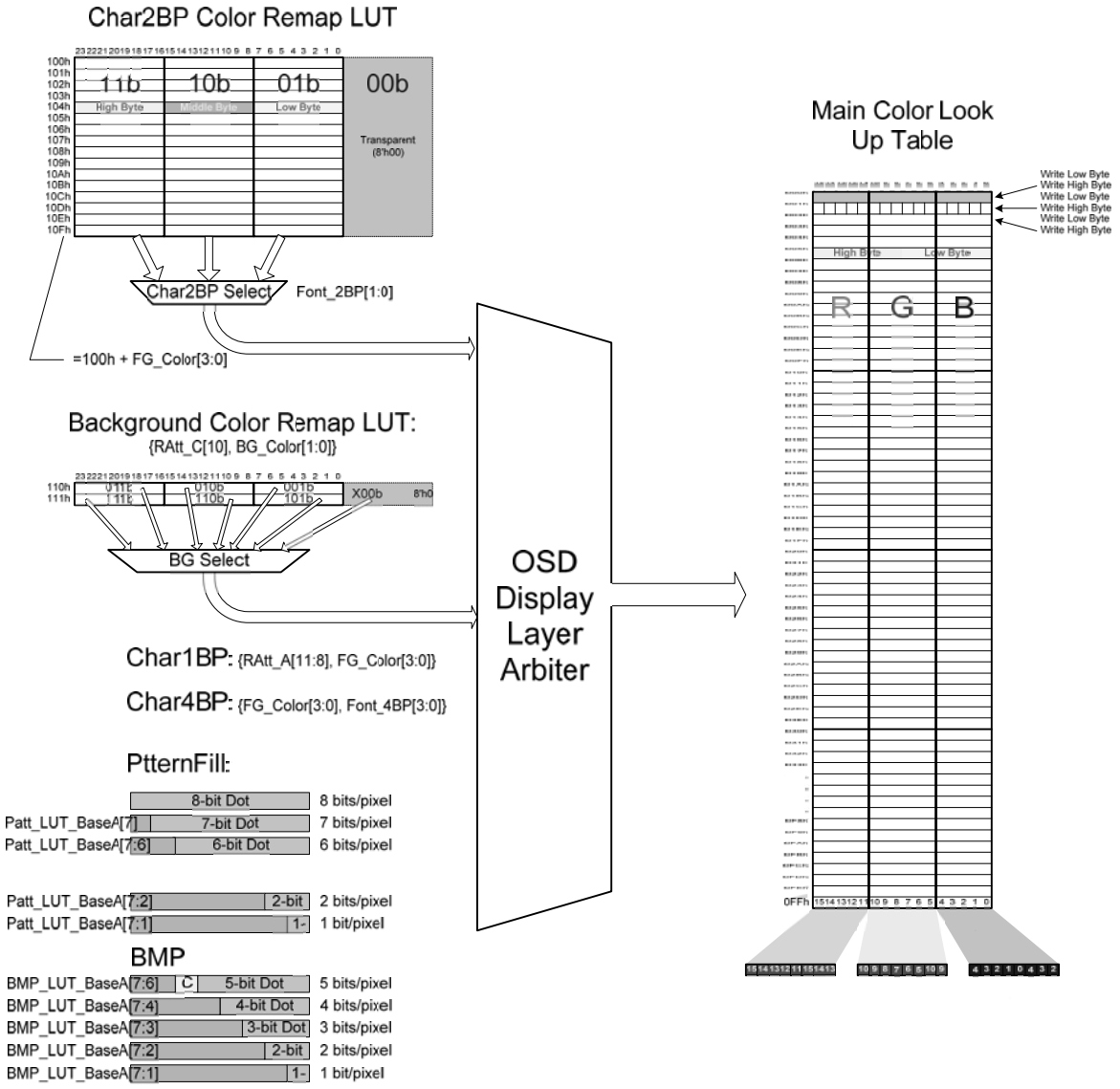
I/O Port	Groups	Index	Description
	Block Write	40h	Block Write Data LSB
		41h	Block Write Data MSB
		42h	Block Write Starting Address LSB
		43h	Block Write Starting Address MSB
		44h	Block Write Count
		45h	Block Write Control
A2h – ORAM_A			OSD1 RAM Address Port of Starting Access (LSB A[7:0] first, then MSB A[12:8]).
A3h – ORAM_D			OSD1 RAM Data Port (Low Byte first, then High Byte). After two Writes, the address will be increased by 1.

2.9.3 OSD1 Color Scheme

For drawing a graphic menu, a colorful icon or logo, …., T138 OSD1 provides 1BPP (one bit per pixel) ~ 5BPP (5 bits per pixel) BMP coding. For n-BPP BMP, it has one background color and (2^n – 1) foreground colors.

For character menus with pre-defined fonts, T138 OSD1 provides mono characters (Char1BP) and color characters (Char2BP, Char4BP), randomly mix-able. So that, simple icon can be implemented by color characters. The color mapping of character/menu is more complicate, please refer to the following drawing.

The OSD1 main Color LUT is 256 entries SRAM, color in RGB565 format.



2.9.4 Character RAM Format

T138 OSD1 character decoding supports 512 fonts. By setting FontROM, Char2BP and Char4BP Font Index Base, we could assign different percentage for those character fonts, depends on application, menu color requirement, memory size, fonts replacing.

The character “MENU” in T138 OSD1 is combined with 1~n character “ROW”s, each ROW can have its own rendering behavior, such as alpha blending, position, zooming ratio, color groups, border/shadow modes, row length,…, these are defined as ROW Attributes (Ratt, current version supports 8 types). Or, few rows can share the same setting without redefining those Ratt.

2.9.4.1 Character Format

Each character is 16-bits length, includes foreground/background color, blinking, font index.

Bit	Symbol	Description
[15:14]	BG_Color[1:0]	Background Color, which combined with the Ratt_C<10> to become 3 bit, selects 6 background remap colors. If both 0, then transparent background.
[13]	Blink	Enable this Character display with blinking feature.
[12:9]	FG_Color[3:0]	Foreground (FG) Color, depends font index is Char1BP, Char2BP or Char4BP: 1. When Char1BP, these 4 bits as FG LSB 4 bits, combine with Ratt_A<11:8> (as FG MSB 4 bits), total 8 bits for selecting color LUT as character FG color. If the value is set as 0000b, then there will be no foreground, i.e. transparent. (Char1BP only) 2. When Char2BP, these 4 bits select one of 16 Char2BP remap LUT. Each Char2BP remap LUT entry is 3*8 bits for 2BP font pixel value: 01b, 10b and 11b. For 2BP font pixel value = 00b, then it will render as transparent. 3. When Char4BP, these 4 bits as FG MSB, then combine with 4BP font pixel 4 bits value to become 8 bits for addressing LUT. For 4BP font pixel value = 0000b, then it will render as transparent.
[8:0]	Char_Index[8:0]	Character Address (Index), selects the character font (i.e., 0,1,2,.. A,B,C, a,b,c,$,%,…). If the value is number N, then it selects the N^{th} font, and that font starting address is (N x Font_Height). The Font_Height is defined in OSD1_01h<4:0>.

2.9.4.2 Row Attribute Alpha-Blending Type Format (Ratt_A)

Bit	Symbol	Description
[15:12]	Ratt_ID = 1101b	Must set value 1101b for Ratt_A
[11:8]	FGC_1BP[7:4]	Defines the MSB 4 bits for Char1BP FG color for current row or below in same thread menu.
[7:6]	Reserved	
[5:4]	FG_aB_Mode[1:0]	Defines the FG alpha-Blending mode (see OSD1 configuration register OSD1_0B for detail) for current row or below in same thread menu.
[3:0]	aB_Src_Percentage[3:0]	Defines the alpha-Blending ratio (of source video/graphic) for current row or below in same thread menu.

2.9.4.3 Row Attribute Character Type Format (Ratt_C)

This Ratt_C is a must-have attribute for each menu row, and those content in OSD1 memory followed will be rendering as characters, not other row attributes except exceeding the row length (see Row_Length[5:0] below).

Bit	Symbol	Description
[15:13]	Ratt_ID = 000b	Must set value 000b for Ratt_C
[12]	Skip_This	When set to 1, the following one character row of current thread menu could be skipped, and continues the next row instead.
[11]	End_After	When set to 1, the following all character rows of current thread menu will be skipped.
[10]	BG_RGB[2]	Background color bit 2, combined with the BG_Color[1:0] in each character become 3 bits to select background remap color.
[9:8]	CharHeight_Scale[1:0]	Defines the enlarge ratio (x1, x2, x3, x4) of the character height of the menu rows following and after.
[7:6]	CharWidth_Scale[1:0]	Defines the enlarge ratio (x1, x2, x3, x4) of the character width of the menu rows following and after.
[5:0]	Row_Length[5:0]	Indicates the following character row length (how many characters), valid value range is 1 to 63.

2.9.4.4 Row Attribute Dummy Type Format (Ratt_D)

This Ratt_D is a dummy attribute, it is used for replacing other non-Ratt_C type attributes when changing rendering behavior if need, also it is used when switch between rows with different BDS behavior, 4 lines will be inserted.

Bit	Symbol	Description
[15:4]	Ratt_ID = E00h	Must set value E00h for Ratt_D
[3:2]	Reserved	
[1:0]	Ratt_ID = E00Xh	Two MSB (Jump_MenuA[14:13])

2.9.4.5 Row Attribute Gap Type Format (Ratt_G)

This Ratt_G is used to insert fix vertical null lines between menu rows.

Bit	Symbol	Description
[15:13]	Ratt_ID = 001b	Must set value 001b for Ratt_G
[12:11]	Reserved	
[10:0]	Gap[10:0]	Line number inserted before the following menu row.

2.9.4.6 Row Attribute Jump Menu Type Format (Ratt_J)

This Ratt_J is used to redirect menu to other assigned new menu block in OSD1 memory. This is useful for controlling menu flows.

Bit	Symbol	Description
[15:14]	Ratt_ID = 10b	Must set value 10b for Ratt_J
[13]	Jump_En	Set to 1 enables the menu jump to new assigned address in Ratt_J<12:0>. When set to 0, this Ratt_J has no effect.
[12:0]	Jump_MenuA[12:0]	Jump to the OSD1 RAM address, which should still point to a row attribute of menu.

2.9.4.7 Row Attribute Horizontal Position Type Format (Ratt_H)

Bit	Symbol	Description
[15:13]	Ratt_ID = 011b	Must set value 011b for Ratt_H
[12:11]	Reserved	
[10:0]	Hstart[10:0]	Set the horizontal start position of the following menu rows.

2.9.4.8 Row Attribute Vertical Position Type Format (Ratt_V)

Bit	Symbol	Description
[15:13]	Ratt_ID = 010b	Must set value 010b for Ratt_V
[12:11]	Reserved	
[10:0]	Vstart[10:0]	Set the vertical start position of the following menu rows.

2.9.5 OSD1 Configuration Registers

2.9.5.1 OSD1 Enable/Blinking Register

Address Offset: OSD1_00h Access: Read/Write
Default Value: 0Ah Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	OSD1_En	Set to 1 for globally enabling OSD1 function.
[6]	R/W	Color_1_Half	Set to 1 for allowing shadow effect when color value is 1
[5:4]	R/W	CRAM_ByteAccess[1:0]	Byte Access mode when programming character of menu: 0Xb: Word access (LSB first, then MSB byte) 10b: LSB only (not affect font index >= 256) 11b: MSB only (character BG/FG colors, Blinking, and Index bit 8)
[3:2]	R/W	BlinkFreq[1:0]	Blinking Frequency Select (internal 4x BCLK for Blinking State Machine). Set 00b for Refresh Rate /16; 01b for 1/32; 10b for 1/64; 11b for 1/128.
[1:0]	R/W	BlinkDuty[1:0]	For adjusting the blinking duty cycle, Set: 00b for Global Blink Off, i.e., 0% Background, 100% OSD2. 01b for 25% Background, 75% OSD2. 10b for 50% Background, 50% OSD2. 11b for 75% Background, 25% OSD2.

2.9.5.2 OSD1 Font Size Register

Address Offset: OSD1_01h Access: Read/Write
Default Value: 12h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	vDE_from_VS	Shift OSD1 more up
[6]	R/W	hDE_from_HS	Shift OSD1 more left
[5]	R/W	FontW16	Set Font Width: 0b: Font Width = 12 1b: Font Width = 16
[4:0]	R/W	FontHeight[4:0]	Font Height, valid value between 1 and 24

2.9.5.3 OSD1 Char2BP Font Index Base Register

Address Offset: OSD1_02h Access: Read/Write
Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Font_Index_2BP[8:1]	Defines the Char2BP font index base (offset). When character index small than this value*2 will be decoded as Char1BP (mono char). And if the character index greater than or equal to this value*2 will be decoded as Char2BP (<= Font_Index_4BP * 2).

2.9.5.4 OSD1 Char4BP Font Index Base Register

Address Offset: OSD1_03h Access: Read/Write
Default Value: C0h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Font_Index_4BP[8:1]	Defines the Char4BP font index base (offset). When character index small than this value*2 will be decoded as Char1BP (mono char) or Char2BP; else, Char4BP.

2.9.5.5 OSD1 Char2BP Font Memory Base Address LSB Register

Address Offset: OSD1_04h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Font_BaseA_2BP[7:0]	Defines the Char2BP font in memory, start with this base address (offset).

2.9.5.6 OSD1 Char2BP Font Memory Base Address MSB Register

Address Offset: OSD1_05h Access: Read/Write
Default Value: 0Ch Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6:0]	R/W	Font_BaseA_2BP[14:8]	Defines the Char2BP font in memory, start with this base address (offset).

2.9.5.7 OSD1 Char4BP Font Memory Base Address LSB Register

Address Offset: OSD1_06h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Font_BaseA_4BP[7:0]	Defines the Char4BP font in memory, start with this base address (offset).

2.9.5.8 OSD1 Char4BP Font Memory Base Address MSB Register

Address Offset: OSD1_07h Access: Read/Write
Default Value: 0Fh Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6:0]	R/W	Font_BaseA_4BP[14:8]	Defines the Char4BP font in memory, start with this base address (offset).

2.9.5.9 OSD1 LUT Address Register

Address Offset: OSD1_08h Access: Write Only
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	WO	LUT_A[8:1]	Assign access pointer of Color LUT. When assigning, LUT_A[0] always = 0. LUT[0..255] are main color LUT (16-bits); LUT[256..271] are Char2BP remap LUT (24-bits); LUT[272..273]are BMP remap LUT (24-bits).

2.9.5.10 OSD1 LUT Data Port Register

Address Offset: OSD1_09h Access: Write Only
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	WO	LUT_D[7:0]	Data written to this port will overwrite OSD1 LUT.

2.9.5.11 OSD1 Window Shadow Width/Height Register

Address Offset: OSD1_0Ah Access: Read/Write
Default Value: 46h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	Wx_ShadowWidth[3:0]	Defines the shadow width (count in 2 dots).
[3:0]	R/W	Wx_ShadowHeight[3:0]	Defines the shadow height (count in 2 lines).

2.9.5.12 OSD1 Global Alpha-Blending Control Register

Address Offset: OSD1_0Bh Access: Read/Write
Default Value: 1Ah Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	Global_aB_Control	Set to 1 for all the alpha-blending behavior of Menu-1, Menu-2 and BMP are control by this register; Set to 0 for separate controls.
[6]	RO	Reserved	
[5:4]	R/W	Global_FG_aB_Mode [1:0]	Defines global alpha-blending for foreground when BG already alpha-Blended: 00b: All FG need alpha-Blended if BG is alpha-Blended; 01b: All FG no need alpha-Blended; 10b: All FG no need alpha-Blended, except their color is LUT[1]; 11b: All FG no need alpha-Blended, except their color is LUT[1..3];
[3:0]	R/W	Global_aB_SrcPercent [3:0]	Defines the percentage of source image/video for mixed with OSD1 menu.

2.9.5.13 OSD1 Char1BP Color High bits Register

Address Offset: OSD1_0Ch Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	RO	Reserved	
[3:0]	R/W	FGC_1BP_Color[7:4]	Defines the Char1BP FG color [7:4]

2.9.5.14 OSD1 FontROM Index Base Register

Address Offset: OSD1_0Dh Access: Read/Write
Default Value: 40h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	FontROM_IndexBase [8:1]	For font index value less than this value is mono character (Char1BP) RAM font segment; For font index >= this value but less than Char2BP_IndexBase is mono character (Char1BP) ROM font segment.

2.9.5.15 OSD1 Revision ID Register

Address Offset: OSD1_0Fh Access: Read Only
Default Value: 31h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	Revision_ID[7:0]	

2.9.5.16 OSD1 Menu-1 Enable Register

Address Offset: OSD1_10h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	M1_En	Set to 1 enable Menu-1 thread to display
[6:0]	RO	Reserved	

2.9.5.17 OSD1 Menu-1 Start Address LSB Register

Address Offset: OSD1_11h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	M1_Menu_SA[7:0]	Point to the 1st row attribute of Menu-1 in OSD1 RAM.

2.9.5.18 OSD1 Menu-1 Start Address MSB Register

Address Offset: OSD1_12h Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6:0]	R/W	M1_Menu_SA[14:8]	Point to the 1st row attribute of Menu-1 in OSD1 RAM.

2.9.5.19 OSD1 Menu-1 End Address LSB Register

Address Offset: OSD1_13h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	M1_Menu_EA[7:0]	Point to the end of Menu-1 in OSD1 RAM.

2.9.5.20 OSD1 Menu-1 End Address MSB Register

Address Offset: OSD1_14h Access: Read/Write
Default Value: 14h Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6:0]	R/W	M1_Menu_EA[14:8]	Point to the end of Menu-1 in OSD1 RAM.

2.9.5.21 OSD1 FontROM Base Address LSB Register

Address Offset: OSD1_16h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Font_BaseA_ROM[7:0]	Point to the start address in ROM, i.e., point to the 1st Font in ROM.

2.9.5.22 OSD1 FontROM Base Address MSB Register

Address Offset: OSD1_17h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	RO	Reserved	
[4:0]	R/W	Font_BaseA_ROM[12:8]	Point to the start address in ROM, i.e., point to the 1st Font in ROM.

2.9.5.23 OSD1 Menu-2 Enable Register

Address Offset: OSD1_18h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	M2_En	Set to 1 enable Menu-2 thread to display
[6:0]	RO	Reserved	

2.9.5.24 OSD1 Menu-2 Start Address LSB Register

Address Offset: OSD1_19h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	M2_Menu_SA[7:0]	Point to the 1st row attribute of Menu-2 in OSD1 RAM.

2.9.5.25 OSD1 Menu-2 Start Address MSB Register

Address Offset: OSD1_1Ah Access: Read/Write
Default Value: 15h Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6:0]	R/W	M2_Menu_SA[14:8]	Point to the 1st row attribute of Menu-2 in OSD1 RAM.

2.9.5.26 OSD1 Menu-2 End Address LSB Register

Address Offset: OSD1_1Bh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	M2_Menu_EA[7:0]	Point to the end of Menu-2 in OSD1 RAM.

2.9.5.27 OSD1 Menu-2 End Address MSB Register

Address Offset: OSD1_1Ch Access: Read/Write
Default Value: 16h Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6:0]	R/W	M2_Menu_EA[14:8]	Point to the end of Menu-2 in OSD1 RAM.

2.9.5.28 OSD1 BMP Control Register

Address Offset: OSD1_20h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	BMP_En	Set to 1 enable BMP to display
[6:4]	R/W	BMP_Nbpp	Defines current BMP for displaying is N bits per pixel. 000b: Reserved 001b: 1 bit/pixel 010b: 2 bits/pixel 011b: 3 bits/pixel 100b: 4 bits/pixel 101b: 5 bits/pixel 11Xb: 5 bits/pixel
[3:2]	R/W	BMP_Extra_Height[1:0]	BMP enlarge ratio in vertical direction: x1, x2, x3, x4 lines
[1:0]	R/W	BMP_Extra_Width[1:0]	BMP enlarge ratio in horizontal direction: x1, x2, x3, x4 dots

2.9.5.29 OSD1 BMP Start Address LSB Register

Address Offset: OSD1_21h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	BMP_SA[7:0]	Point to the top-left dot of BMP for displaying in OSD1 RAM.

2.9.5.30 OSD1 BMP Start Address MSB Register

Address Offset: OSD1_22h Access: Read/Write
Default Value: 0Bh Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6:0]	R/W	BMP_SA[14:8]	Point to the top-left dot of BMP for displaying in OSD1 RAM.

2.9.5.31 OSD1 BMP Alpha-Blending Control Register

Address Offset: OSD1_23h Access: Read/Write
Default Value: 1Ah Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:4]	R/W	BMP_FG_aB_Mode[1:0]	Defines BMP alpha-blending for foreground when BG already alpha-Blended: 00b: All FG need alpha-Blended if BG is alpha-Blended; 01b: All FG no need alpha-Blended; 10b: All FG no need alpha-Blended, except their color is LUT[1]; 11b: All FG no need alpha-Blended, except their color is LUT[1..3];
[3:0]	R/W	BMP_aB_SrcPercent [3:0]	Defines the percentage of source image/video for mixed with OSD1 BMP.

2.9.5.32 OSD1 BMP Horizontal Size LSB Register

Address Offset: OSD1_24h Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	BMP_Hsize[7:0]	Defines the horizontal size of BMP for displaying in OSD1 RAM. Unit is how many words (16-bits) count (before enlarged).

2.9.5.33 OSD1 BMP Horizontal Size MSB Register

Address Offset: OSD1_25h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	BMP_Hsize[10:8]	Defines the horizontal size of BMP for displaying in OSD1 RAM.

2.9.5.34 OSD1 BMP Vertical Size LSB Register

Address Offset: OSD1_26h Access: Read/Write
Default Value: 60h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	BMP_Hsize[7:0]	Defines the vertical size of BMP for displaying in OSD1 RAM. Unit is how many lines count (before enlarged).

2.9.5.35 OSD1 BMP Vertical Size MSB Register

Address Offset: OSD1_27h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	BMP_Hsize[10:8]	Defines the vertical size of BMP for displaying in OSD1 RAM.

2.9.5.36 OSD1 BMP Horizontal Start Position LSB Register

Address Offset: OSD1_28h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	BMP_HStart[7:0]	Defines the left boundary position of BMP for displaying, count in display clocks.

2.9.5.37 OSD1 BMP Horizontal Start Position MSB Register

Address Offset: OSD1_29h Access: Read/Write
Default Value: 03h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	BMP_HStart[10:8]	Defines the left boundary position of BMP for displaying.

2.9.5.38 OSD1 BMP Vertical Start Position LSB Register

Address Offset: OSD1_2Ah Access: Read/Write
Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	BMP_VStart[7:0]	Defines the top boundary position of BMP for displaying, count in lines.

2.9.5.39 OSD1 BMP Vertical Start Position MSB Register

Address Offset: OSD1_2Bh Access: Read/Write
Default Value: 02h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	BMP_VStart[10:8]	Defines the top boundary position of BMP for displaying.

2.9.5.40 OSD1 BMP LUT Base Address Register

Address Offset: OSD1_2Ch Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7:1]	R/W	BMP_LUT_BaseA[7:1]	Defines the LUT offset. For N-BPP BMP, its LUT segment starts with {BMP_LUT_BaseA[7:N], N'b0};
[0]	RO	Reserved	

2.9.5.41 OSD1 BMP Background Color Register

Address Offset: OSD1_2Dh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description

[7:0]	R/W	BMP_BG_Color[7:0]	Defines the address of one LUT as BMP background color.

2.9.5.42 OSD1 Block Write Data LSB Register

Address Offset: OSD1_40h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	OSD1_BlockWr_D[7:0]	LSB Data to be block fill

2.9.5.43 OSD1 Block Write Data MSB Register

Address Offset: OSD1_41h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	OSD1_BlockWr_D[15:8]	MSB Data to be block fill

2.9.5.44 OSD1 Block Write Starting Address LSB Register

Address Offset: OSD1_42h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	OSD1_BlockWr_SA[7:0]	Starting Address of block fill

2.9.5.45 OSD1 Block Write Starting Address MSB Register

Address Offset: OSD1_43h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6:0]	R/W	OSD1_BlockWr_SA[14:8]	Starting Address of block fill

2.9.5.46 OSD1 Block Write Length Register

Address Offset: OSD1_44h Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	OSD1_BlockWr_L[7:0]	Block fill length (count)

2.9.5.47 OSD1 Block Write Control Register

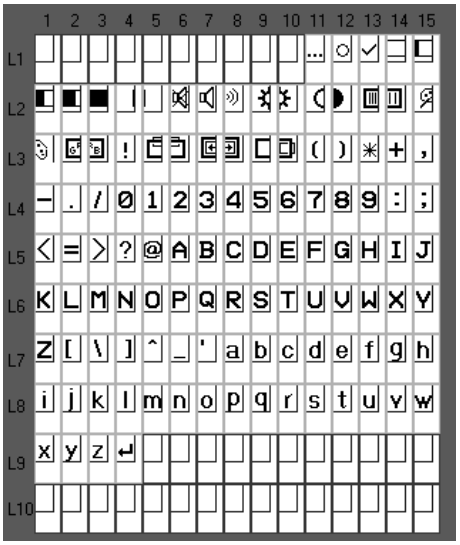
Address Offset: OSD1_45h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	WO/ RO	OSD1_BlockWr_Trig OSD1_BlockWr_Done	Set to 1 to trigger block fill operation Get 1 means the block fill operation is done
[6]	R/W	OSD1_BlockWr_mode	
[5:0]	R/W	OSD1_BlockWr_L[13:8]	Block fill length (count)

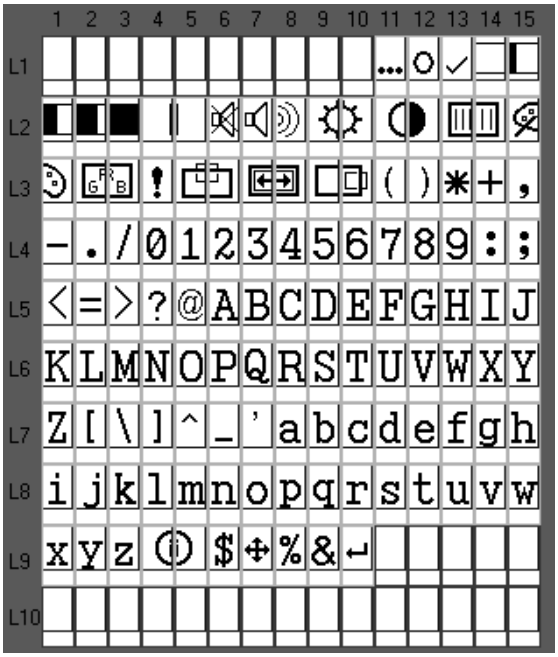
2.9.5.48 OSD1 ROM Font Sets

In addition to 6Kx16 SRAM for download-able fonts, this LCD controller also support two sets of build-in ROM Fonts

2.9.5.48.1 Size=18x12, 114+ fonts



2.9.5.48.2 Size=24x16, 120 fonts

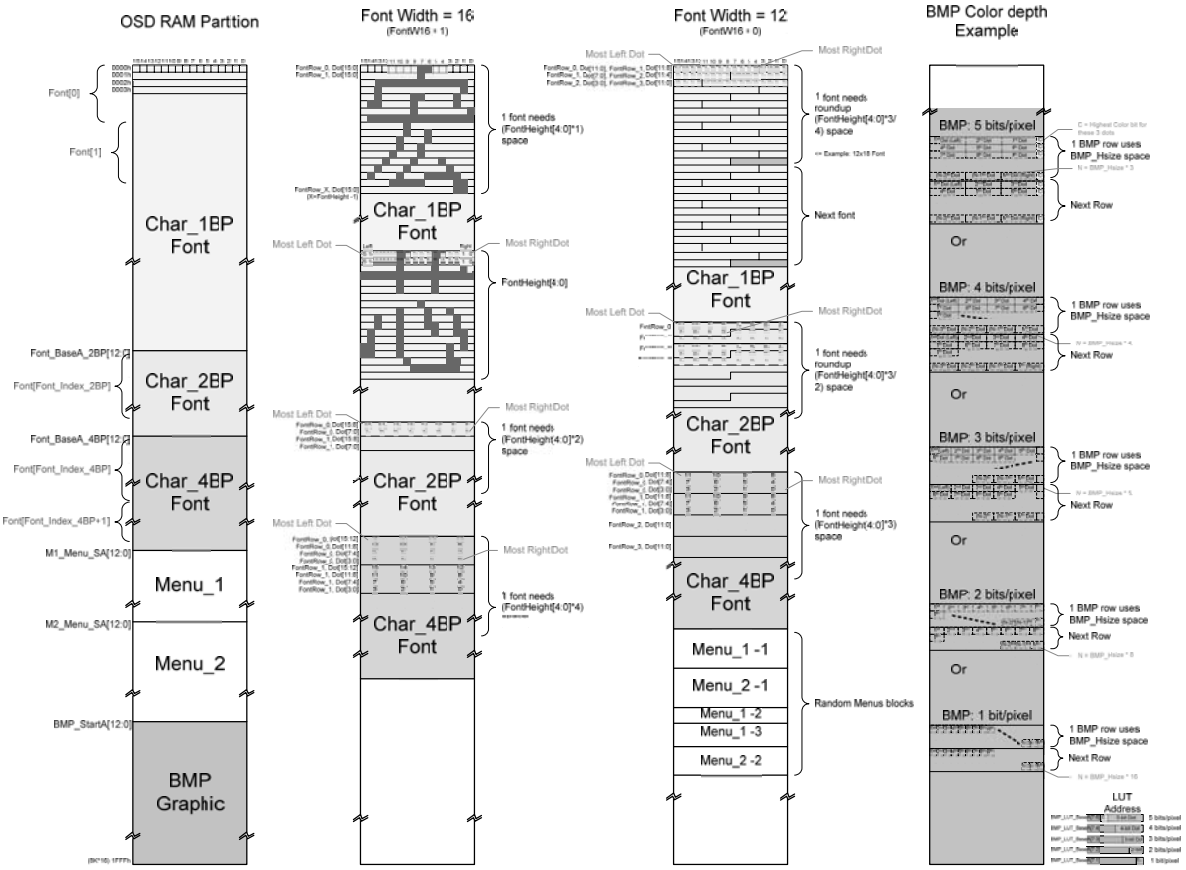


2.10 OSD2

The OSD2 in T138 is improved in rendering and efficient memory usage. The legacy OSD is either one thread Menu or one graphic (BMP) mode. T138 OSD2 supports two threads menus and 1 graphic rendering simultaneously. So it will be easier to have menu control and Closed Caption.

2.10.1 OSD2 RAM Partition

The OSD2 Font/Menus/BMP memory share the same built-in 8Kx16 or 16Kx16 SRAM, depends on bonding option.



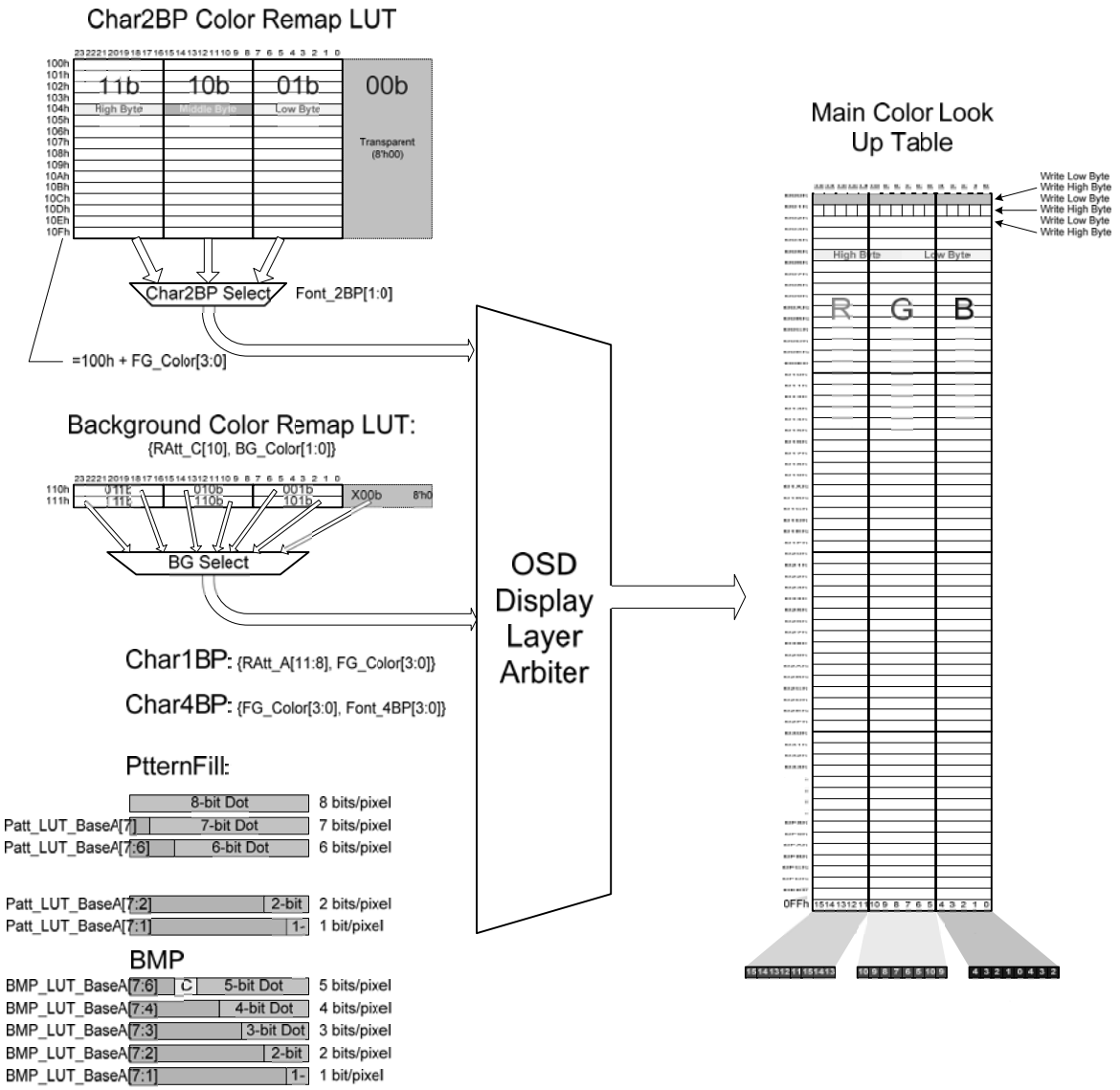
2.10.2 OSD2 Register Map

I/O Port	Groups	Index	Description
A8h – OSD2_Index A9h – OSD2_Data	Global Setting	00h	OSD2 Enable/Blinking Register
		01h	Font Size
		02h	Char2BP Font Index Base
		03h	Char4BP Font Index Base
		04h	Char2BP Font Memory Base Address, LSB
		05h	Char2BP Font Memory Base Address, MSB
		06h	Char4BP Font Memory Base Address, LSB
		07h	Char4BP Font Memory Base Address, MSB
		08h	OSD2 Color LUT Address port
		09h	OSD2 Color LUT Data Port
		0Ah	OSD2 Window Shadow
		0Bh	Global Alpha Blending Control
		0Ch	Char1BP color high bits offset
		0Dh	ROM Font Index Base
		0Eh	OSD2 Extra 8K words SRAM
		0Fh	Revision ID
	Menu-1 Setting	10h	Menu-1 Enable
		11h	Menu-1 Start Address, LSB
		12h	Menu-1 Start Address, MSB
		13h	Menu-1 End Address, LSB
		14h	Menu-1 End Address, MSB
	ROM Font	16h	ROM Font Memory Base Address, LSB
		17h	ROM Font Memory Base Address, MSB
	Menu-2 Setting	18h	Menu-2 Enable
		19h	Menu-2 Start Address, LSB
		1Ah	Menu-2 Start Address, MSB
		1Bh	Menu-2 End Address, LSB
		1Ch	Menu-2 End Address, MSB
	BMP Setting	20h	BMP Control Register
		21h	BMP Start Address, LSB
		22h	BMP Start Address, MSB
		23h	BMP Alpha Blending Control
		24h	BMP Horizontal Size, LSB
		25h	BMP Horizontal Size, MSB
		26h	BMP Vertical Size, LSB
		27h	BMP Vertical Size, MSB
		28h	BMP Position, Horizontal Start, LSB
		29h	BMP Position, Horizontal Start, MSB
		2Ah	BMP Position, Vertical Start, LSB
		2Bh	BMP Position, Vertical Start, MSB
		2Ch	BMP LUT Base Address
		2Dh	BMP Background Color

I/O Port	Groups	Index	Description
A8h – OSD2_Index A9h – OSD2_Data	Pattern Fill	30h	Patt Control Register
		31h	Patt LUT Base Address
		32h	Patt Horizontal Size
		33h	Patt Vertical Size
		34h	Patt Row Shift
		35h	Patt Alpha Blending Control
		36h	OSD2 BIST result and Patt Enlarge
		37h	Patt RAM Write Data Port
		38h	Patt Horizontal Start, LSB
		39h	Patt Horizontal Start, MSB
		3Ah	Patt Vertical Start, LSB
		3Bh	Patt Vertical Start, MSB
		3Ch	Patt Horizontal End, LSB
		3Dh	Patt Horizontal End, MSB
		3Eh	Patt Vertical End, LSB
		3Fh	Patt Vertical End, MSB
	Block Write	40h	Block Write Data LSB
		41h	Block Write Data MSB
		42h	Block Write Starting Address LSB
		43h	Block Write Starting Address MSB
		44h	Block Write Count
		45h	Block Write Control
AAh – ORAM_A			OSD2 RAM Address Port of Starting Access (LSB A[7:0] first, then MSB A[12:8]).
ABh – ORAM_D			OSD2 RAM Data Port (Low Byte first, then High Byte). After two Writes, the address will be increased by 1.

2.10.3 OSD2 Color Scheme

For drawing a graphic menu, a colorful icon or logo, …., T138 OSD2 provides 1BPP (one bit per pixel) ~ 5BPP (5 bits per pixel) BMP coding. For n-BPP BMP, it has one background color and (2^n – 1) foreground colors. For character menus with pre-defined fonts, T138 OSD2 provides mono characters (Char1BP) and color characters (Char2BP, Char4BP), randomly mix-able. So that, simple icon can be implemented by color characters. The color mapping of character/menu is more complicate, please refer to the following drawing. The OSD2 main Color LUT is 256 entries SRAM, color in RGB565 format.



2.10.4 Character RAM Format

T138 OSD2 character decoding supports 512 fonts. By setting FontROM, Char2BP and Char4BP Font Index Base, we could assign different percentage for those character fonts, depends on application, menu color requirement, memory size, fonts replacing, ...

The character “MENU” in T138 OSD2 is combined with 1~n character “ROW”s, each ROW can have its own rendering behavior, such as alpha blending, position, zooming ratio, color groups, border/shadow modes, row length,…, these are defined as ROW Attributes (RAtt, current version supports 8 types). Or, few rows can share the same setting without redefining those RAtt.

2.10.4.1 Character Format

Each character is 16-bits length, includes foreground/background color, blinking, font index.

Bit	Symbol	Description
[15:14]	BG_Color[1:0]	Background Color, which combined with the RAtt_C<10> to become 3 bit, selects 6 background remap colors. If both 0, then transparent background.
[13]	Blink	Enable this Character display with blinking feature.
[12:9]	FG_Color[3:0]	Foreground (FG) Color, depends font index is Char1BP, Char2BP or Char4BP: 1. When Char1BP, these 4 bits as FG LSB 4 bits, combine with RAtt_A<11:8> (as FG MSB 4 bits), total 8 bits for selecting color LUT as character FG color. If the value is set as 0000b, then there will be no foreground, i.e. transparent. (Char1BP only) 2. When Char2BP, these 4 bits select one of 16 Char2BP remap LUT. Each Char2BP remap LUT entry is 3*8 bits for 2BP font pixel value: 01b, 10b and 11b. For 2BP font pixel value = 00b, then it will render as transparent. 3. When Char4BP, these 4 bits as FG MSB, then combine with 4BP font pixel 4 bits value to become 8 bits for addressing LUT. For 4BP font pixel value = 0000b, then it will render as transparent.
[8:0]	Char_Index[8:0]	Character Address (Index), selects the character font (i.e., 0,1,2,.. A,B,C, a,b,c,$,%,…). If the value is number N, then it selects the N^{th} font, and that font starting address is (N x Font_Height). The Font_Height is defined in OSD2_01h<4:0>.

2.10.4.2 Row Attribute Alpha-Blending Type Format (RAtt_A)

Bit	Symbol	Description
[15:12]	RAtt_ID = 1101b	Must set value 1101b for RAtt_A
[11:8]	FGC_1BP[7:4]	Defines the MSB 4 bits for Char1BP FG color for current row or below in same thread menu.
[7:6]	Reserved	
[5:4]	FG_aB_Mode[1:0]	Defines the FG alpha-Blending mode (see OSD2 configuration register OSD2_0B for detail) for current row or below in same thread menu.
[3:0]	aB_Source_Percentage[3 0]	Defines the alpha-Blending ratio (of source video/graphic) for current row or below in same thread menu.

2.10.4.3 Row Attribute Character Type Format (RAtt_C)

This RAtt_C is a must-have attribute for each menu row, and those content in OSD2 memory followed will be rendering as characters, not other row attributes except exceeding the row length (see Row_Length[5:0] below).

Bit	Symbol	Description
[15:13]	RAtt_ID = 000b	Must set value 000b for RAtt_C
[12]	Skip_This	When set to 1, the following one character row of current thread menu could be skipped, and continues the next row instead.
[11]	End_After	When set to 1, the following all character rows of current thread menu will be skipped.
[10]	BG_RGB[2]	Background color bit 2, combined with the BG_Color[1:0] in each character become 3 bits to select background remap color.
[9:8]	CharHeight_Scale[1:0]	Defines the enlarge ratio (x1, x2, x3, x4) of the character height of the menu rows following and after.
[7:6]	CharWidth_Scale[1:0]	Defines the enlarge ratio (x1, x2, x3, x4) of the character width of the menu rows following and after.
[5:0]	Row_Length[5:0]	Indicates the following character row length (how many characters), valid value range is 1 to 63.

2.10.4.4 Row Attribute Dummy Type Format (RAtt_D)

This RAtt_D is a dummy attribute, it is used for replacing other non-RAtt_C type attributes when changing rendering behavior if need, also it is used when switch between rows with different BDS behavior, 4 lines will be inserted.

Bit	Symbol	Description
[15:4]	RAtt_ID = E00h	Must set value E00h for RAtt_D
[3:1]	Reserved	
[0]	Jump_MenuA[13]	Jump to the OSD2 RAM address, which should still point to a row attribute of menu. Set this MSB before RAtt_J.

2.10.4.5 Row Attribute Gap Type Format (RAtt_G)

This RAtt_G is used to insert fix vertical null lines between menu rows.

Bit	Symbol	Description
[15:13]	RAtt_ID = 001b	Must set value 001b for RAtt_G
[12:11]	Reserved	
[10:0]	Gap[10:0]	Line number inserted before the following menu row.

2.10.4.6 Row Attribute Jump Menu Type Format (RAtt_J)

This RAtt_J is used to redirect menu to other assigned new menu block in OSD2 memory. This is useful for controlling menu flows.

Bit	Symbol	Description
[15:14]	RAtt_ID = 10b	Must set value 10b for RAtt_J
[13]	Jump_En	Set to 1 enables the menu jump to new assigned address in RAtt_J<12:0>. When set to 0, this RAtt_J has no effect.
[12:0]	Jump_MenuA[12:0]	Jump to the OSD2 RAM address, which should still point to a row attribute of menu.

2.10.4.7 Row Attribute Horizontal Position Type Format (RAtt_H)

Bit	Symbol	Description
[15:13]	RAtt_ID = 011b	Must set value 011b for RAtt_H
[12:11]	Reserved	
[10:0]	HStart[10:0]	Set the horizontal start position of the following menu rows.

2.10.4.8 Row Attribute Vertical Position Type Format (RAtt_V)

Bit	Symbol	Description
[15:13]	RAtt_ID = 010b	Must set value 010b for RAtt_V
[12:11]	Reserved	
[10:0]	VStart[10:0]	Set the vertical start position of the following menu rows.

2.10.5 OSD2 Configuration Registers

2.10.5.1 OSD2 Enable/Blinking Register

Address Offset: OSD2_00h Access: Read/Write
Default Value: 0Ah Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	OSD2_En	Set to 1 for globally enabling OSD2 function.
[6]	R/W	Color_1_Half	Set to 1 for allowing shadow effect when color value is 1
[5:4]	R/W	CRAM_ByteAccess[1:0]	Byte Access mode when programming character of menu: 0Xb: Word access (LSB first, then MSB byte) 10b: LSB only (not affect font index >= 256) 11b: MSB only (character BG/FG colors, Blinking, and Index bit 8)
[3:2]	R/W	BlinkFreq[1:0]	Blinking Frequency Select (internal 4x BCLK for Blinking State Machine). Set 00b for Refresh Rate /16; 01b for 1/32; 10b for 1/64; 11b for 1/128.
[1:0]	R/W	BlinkDuty[1:0]	For adjusting the blinking duty cycle, Set: 00b for Global Blink Off, i.e., 0% Background, 100% OSD2. 01b for 25% Background, 75% OSD2. 10b for 50% Background, 50% OSD2. 11b for 75% Background, 25% OSD2.

2.10.5.2 OSD2 Font Size Register

Address Offset: OSD2_01h Access: Read/Write
Default Value: 12h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	vDE_from_VS	Shift OSD1 more up
[6]	R/W	hDE_from_HS	Shift OSD1 more left
[5]	R/W	FontW16	Set Font Width: 0b: Font Width = 12 1b: Font Width = 16
[4:0]	R/W	FontHeight[4:0]	Font Height, valid value between 1 and 24

2.10.5.3 OSD2 Char2BP Font Index Base Register

Address Offset: OSD2_02h Access: Read/Write
Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Font_Index_2BP[8:1]	Defines the Char2BP font index base (offset). When character index small than this value*2 will be decoded as Char1BP (mono char). And if the character index greater than or equal to this value*2 will be decoded as Char2BP (<= Font_Index_4BP * 2).

2.10.5.4 OSD2 Char4BP Font Index Base Register

Address Offset: OSD2_03h Access: Read/Write
Default Value: C0h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Font_Index_4BP[8:1]	Defines the Char4BP font index base (offset). When character index small than this value*2 will be decoded as Char1BP (mono char) or Char2BP; else, Char4BP.

2.10.5.5 OSD2 Char2BP Font Memory Base Address LSB Register

Address Offset: OSD2_04h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Font_BaseA_2BP[7:0]	Defines the Char2BP font in memory, start with this base address (offset).

2.10.5.6 OSD2 Char2BP Font Memory Base Address MSB Register

Address Offset: OSD2_05h Access: Read/Write
Default Value: 0Ch Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6:0]	R/W	Font_BaseA_2BP[14:8]	Defines the Char2BP font in memory, start with this base address (offset).

2.10.5.7 OSD2 Char4BP Font Memory Base Address LSB Register

Address Offset: OSD2_06h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Font_BaseA_4BP[7:0]	Defines the Char4BP font in memory, start with this base address (offset).

2.10.5.8 OSD2 Char4BP Font Memory Base Address MSB Register

Address Offset: OSD2_07h Access: Read/Write
Default Value: 0Fh Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6:0]	R/W	Font_BaseA_4BP[14:8]	Defines the Char4BP font in memory, start with this base address (offset).

2.10.5.9 OSD2 LUT Address Register

Address Offset: OSD2_08h Access: Write Only
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	WO	LUT_A[8:1]	Assign access pointer of Color LUT. When assigning, LUT_A[0] always = 0. LUT[0..255] are main color LUT (16-bits); LUT[256..271] are Char2BP remap LUT (24-bits); LUT[272..273]are BMP remap LUT (24-bits).

2.10.5.10 OSD2 LUT Data Port Register

Address Offset: OSD2_09h Access: Write Only
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	WO	LUT_D[7:0]	Data written to this port will overwrite OSD2 LUT.

2.10.5.11 OSD2 Window Shadow Width/Height Register

Address Offset: OSD2_0Ah Access: Read/Write
Default Value: 46h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	Wx_ShadowWidth[3:0]	Defines the shadow width (count in 2 dots).
[3:0]	R/W	Wx_ShadowHeight[3:0]	Defines the shadow height (count in 2 lines).

2.10.5.12 OSD2 Global Alpha-Blending Control Register

Address Offset: OSD2_0Bh Access: Read/Write
Default Value: 1Ah Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	Global_aB_Control	Set to 1 for all the alpha-blending behavior of Menu-1, Menu-2 and BMP are control by this register; Set to 0 for separate controls.
[6]	RO	Reserved	
[5:4]	R/W	Global_FG_aB_Mode [1:0]	Defines global alpha-blending for foreground when BG already alpha-Blended: 00b: All FG need alpha-Blended if BG is alpha-Blended; 01b: All FG no need alpha-Blended; 10b: All FG no need alpha-Blended, except their color is LUT[1]; 11b: All FG no need alpha-Blended, except their color is LUT[1..3];
[3:0]	R/W	Global_aB_SrcPercent [3:0]	Defines the percentage of source image/video for mixed with OSD2 menu.

2.10.5.13 OSD2 Char1BP Color High bits Register

Address Offset: OSD2_0Ch Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	RO	Reserved	
[3:0]	R/W	FGC_1BP_Color[7:4]	Defines the Char1BP FG color [7:4]

2.10.5.14 OSD2 FontROM Index Base Register

Address Offset: OSD2_0Dh Access: Read/Write
Default Value: 40h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	FontROM_IndexBase [8:1]	For font index value less than this value is mono character (Char1BP) RAM font segment; For font index >= this value but less than Char2BP_IndexBase is mono character (Char1BP) ROM font segment.

2.10.5.15 OSD2 Extra 8K Word Config Register

Address Offset: OSD2_0Eh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	Extra8K4OSD2	1: 16K words for OSD2 & 16K words for OSD1 0: 8K words for OSD2 & 24K words for OSD1
[6:0]	RO	Reserved	

2.10.5.16 OSD2 Revision ID Register

Address Offset: OSD2_0Fh Access: Read Only
Default Value: 31h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	Revision_ID[7:0]	

2.10.5.17 OSD2 Menu-1 Enable Register

Address Offset: OSD2_10h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	M1_En	Set to 1 enable Menu-1 thread to display
[6:0]	RO	Reserved	

2.10.5.18 OSD2 Menu-1 Start Address LSB Register

Address Offset: OSD2_11h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	M1_Menu_SA[7:0]	Point to the 1st row attribute of Menu-1 in OSD2 RAM.

2.10.5.19 OSD2 Menu-1 Start Address MSB Register

Address Offset: OSD2_12h Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:0]	R/W	M1_Menu_SA[13:8]	Point to the 1st row attribute of Menu-1 in OSD2 RAM.

2.10.5.20 OSD2 Menu-1 End Address LSB Register

Address Offset: OSD2_13h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	M1_Menu_EA[7:0]	Point to the end of Menu-1 in OSD2 RAM.

2.10.5.21 OSD2 Menu-1 End Address MSB Register

Address Offset: OSD2_14h Access: Read/Write
Default Value: 14h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:0]	R/W	M1_Menu_EA[13:8]	Point to the end of Menu-1 in OSD2 RAM.

2.10.5.22 OSD2 FontROM Base Address LSB Register

Address Offset: OSD2_16h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Font_BaseA_ROM[7:0]	Point to the start address in ROM, i.e., point to the 1st Font in ROM.

2.10.5.23 OSD2 FontROM Base Address MSB Register

Address Offset: OSD2_17h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	RO	Reserved	
[4:0]	R/W	Font_BaseA_ROM[12:8]	Point to the start address in ROM, i.e., point to the 1st Font in ROM.

2.10.5.24 OSD2 Menu-2 Enable Register

Address Offset: OSD2_18h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	M2_En	Set to 1 enable Menu-2 thread to display
[6:0]	RO	Reserved	

2.10.5.25 OSD2 Menu-2 Start Address LSB Register

Address Offset: OSD2_19h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	M2_Menu_SA[7:0]	Point to the 1st row attribute of Menu-2 in OSD2 RAM.

2.10.5.26 OSD2 Menu-2 Start Address MSB Register

Address Offset: OSD2_1Ah Access: Read/Write
Default Value: 15h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:0]	R/W	M2_Menu_SA[13:8]	Point to the 1st row attribute of Menu-2 in OSD2 RAM.

2.10.5.27 OSD2 Menu-2 End Address LSB Register

Address Offset: OSD2_1Bh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	M2_Menu_EA[7:0]	Point to the end of Menu-2 in OSD2 RAM.

2.10.5.28 OSD2 Menu-2 End Address MSB Register

Address Offset: OSD2_1Ch Access: Read/Write
Default Value: 16h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:0]	R/W	M2_Menu_EA[13:8]	Point to the end of Menu-2 in OSD2 RAM.

2.10.5.29 OSD2 BMP Control Register

Address Offset: OSD2_20h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	BMP_En	Set to 1 enable BMP to display
[6:4]	R/W	BMP_Nbpp	Defines current BMP for displaying is N bits per pixel. 000b: Reserved 001b: 1 bit/pixel 010b: 2 bits/pixel 011b: 3 bits/pixel 100b: 4 bits/pixel 101b: 5 bits/pixel 11Xb: 5 bits/pixel
[3:2]	R/W	BMP_Extra_Height[1:0]	BMP enlarge ratio in vertical direction: x1, x2, x3, x4 lines
[1:0]	R/W	BMP_Extra_Width[1:0]	BMP enlarge ratio in horizontal direction: x1, x2, x3, x4 dots

2.10.5.30 OSD2 BMP Start Address LSB Register

Address Offset: OSD2_21h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	BMP_SA[7:0]	Point to the top-left dot of BMP for displaying in OSD2 RAM.

2.10.5.31 OSD2 BMP Start Address MSB Register

Address Offset: OSD2_22h Access: Read/Write
Default Value: 0Bh Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:0]	R/W	BMP_SA[13:8]	Point to the top-left dot of BMP for displaying in OSD2 RAM.

2.10.5.32 OSD2 BMP Alpha-Blending Control Register

Address Offset: OSD2_23h Access: Read/Write
Default Value: 1Ah Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:4]	R/W	BMP_FG_aB_Mode[1:0]	Defines BMP alpha-blending for foreground when BG already alpha-Blended: 00b: All FG need alpha-Blended if BG is alpha-Blended; 01b: All FG no need alpha-Blended; 10b: All FG no need alpha-Blended, except their color is LUT[1]; 11b: All FG no need alpha-Blended, except their color is LUT[1..3];
[3:0]	R/W	BMP_aB_SrcPercent [3:0]	Defines the percentage of source image/video for mixed with OSD2 BMP.

2.10.5.33 OSD2 BMP Horizontal Size LSB Register

Address Offset: OSD2_24h Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	BMP_HSize[7:0]	Defines the horizontal size of BMP for displaying in OSD2 RAM. Unit is how many words (16-bits) count (before enlarged).

2.10.5.34 OSD2 BMP Horizontal Size MSB Register

Address Offset: OSD2_25h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	BMP_HSize[10:8]	Defines the horizontal size of BMP for displaying in OSD2 RAM.

2.10.5.35 OSD2 BMP Vertical Size LSB Register

Address Offset: OSD2_26h Access: Read/Write
Default Value: 60h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	BMP_HSize[7:0]	Defines the vertical size of BMP for displaying in OSD2 RAM. Unit is how many lines count (before enlarged).

2.10.5.36 OSD2 BMP Vertical Size MSB Register

Address Offset: OSD2_27h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	BMP_HSize[10:8]	Defines the vertical size of BMP for displaying in OSD2 RAM.

2.10.5.37 OSD2 BMP Horizontal Start Position LSB Register

Address Offset: OSD2_28h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	BMP_HStart[7:0]	Defines the left boundary position of BMP for displaying, count in display clocks.

2.10.5.38 OSD2 BMP Horizontal Start Position MSB Register

Address Offset: OSD2_29h Access: Read/Write
Default Value: 03h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	BMP_HStart[10:8]	Defines the left boundary position of BMP for displaying.

2.10.5.39 OSD2 BMP Vertical Start Position LSB Register

Address Offset: OSD2_2Ah Access: Read/Write
Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	BMP_VStart[7:0]	Defines the top boundary position of BMP for displaying, count in lines.

2.10.5.40 OSD2 BMP Vertical Start Position MSB Register

Address Offset: OSD2_2Bh Access: Read/Write
Default Value: 02h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	BMP_VStart[10:8]	Defines the top boundary position of BMP for displaying.

2.10.5.41 OSD2 BMP LUT Base Address Register

Address Offset: OSD2_2Ch Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7:1]	R/W	BMP_LUT_BaseA[7:1]	Defines the LUT offset. For N-BPP BMP, its LUT segment starts with {BMP_LUT_BaseA[7:N], N'b0};
[0]	RO	Reserved	

2.10.5.42 OSD2 BMP Background Color Register

Address Offset: OSD2_2Dh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	BMP_BG_Color[7:0]	Defines the address of one LUT as BMP background color.

2.10.5.43 OSD2 Pattern_Fill Control Register

Address Offset: OSD2_30h Access: Read/Write
Default Value: 48h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	Patt_En	Set to 1 enable Pattern_Fill to display
[6:4]	R/W	Patt_ColorDepth[2:0]	Defines nBP color: 000b: 8BPP 001b: 1BPP 010b: 2BPP 011b: 3BPP 100b: 4BPP 101b: 5BPP 110b: 6BPP 111b: 7BPP
[3:2]	R/W	Patt_RAM_Bit[1:0]	Defines the usage in Pattern RAM: 00b: 1 bit/pixel 01b: 2 bits/pixel 10b: 4 bits/pixel 11b: 8 bits/pixel
[1]	R/W	Patt_Independ_AB	Set to 1 for independent Alpha-Blending setting for Pattern_Fill; set to 0 for by OSD2_0B
[0]	WO	Reset_PRAM_Pointer	Write 1 to reset the Pattern RAM pointer for loading pattern data

2.10.5.44 OSD2 Pattern_Fill LUT Base Address Register

Address Offset: OSD2_31h Access: Read/Write
Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:7]	R/W	Patt_LUT_BaseA[7:0]	Defines the MSB color in LUT for PatternFill color. Bit 0 is not used.

2.10.5.45 OSD2 Pattern_Fill Pattern Horizontal Size Register

Address Offset: OSD2_32h Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Patt_HSize[7:0]	For repeated pattern, this defines its width in the unit: Byte.

2.10.5.46 OSD2 Pattern_Fill Pattern Vertical Size Register

Address Offset: OSD2_33h Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Patt_VSize[7:0]	For repeated pattern, this defines its height in the unit: line.

2.10.5.47 OSD2 Pattern_Fill Pattern Row Shift Register

Address Offset: OSD2_34h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Patt_Row_Shift[7:0]	For repeated pattern, this defines horizontal shift in the unit: Byte, to build a delta-type pattern.

2.10.5.48 OSD2 Pattern_Fill Color High Bits Register

Address Offset: OSD2_35h Access: Read/Write
Default Value: 05h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	RO	Reserved	
[3:0]	R/W	Patt_aB_ SourcePencent[3:0]	Alpha Blending percentage (n/16) for Filled patterns only. If set 0000b, alpha blending is disabled (0/16 * Original Video Source + 8/8 * PatternFill display); If set 0001b, blending as 1/16 * Original Video Source + 15/16 * PatternFill display; . . . If set N, blending as N/16 * Original Video Source + (16-N)/16 * PatternFill display;

2.10.5.49 OSD2 BIST Result and Pattern Enlarge Register

Address Offset: OSD2_36h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO	OSD2_ORAM_Fail	After OSD BIST done, get 1 in this bit shows the OSD2 Font/Menu RAM is failed.
[6]	RO	OSD2_ORAM2_Fail	After OSD BIST done, get 1 in this bit shows the OSD2 Font/Menu RAM is failed.
[5]	RO	OSD2_PRAM_Fail	After OSD BIST done, get 1 in this bit shows the OSD2 PatternFill RAM is failed.
[4]	RO	OSD2_FontROMFail	After OSD BIST done, get 1 in this bit shows the OSD2 Font ROM is failed.
[3:2]	R/W	Patt_V_Enlarge[1:0]	For each repeated pattern, enlarge it in verical direction
[1:0]	R/W	Patt_H_Enlarge[1:0]	For each repeated pattern, enlarge it in horizontal direction

2.10.5.50 OSD2 Pattern_Fill Pattern RAM Write Port Register

Address Offset: OSD2_37h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	WO	PRAM_WrD_Port[10:8]	For building pattern, need to load via writing pattern to PRAM (Pattern RAM). After reset PRAM pointer, the PRAM pointer will increase after each burst write.

2.10.5.51 OSD2 Pattern_Fill Position, Horizontal Start LSB Register

Address Offset: OSD2_38h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Patt_HStart[7:0]	Allowable pattern display region: horizontal start

2.10.5.52 OSD2 Pattern_Fill Position, Horizontal Start MSB Register

Address Offset: OSD2_39h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	Patt_HStart[10:8]	Allowable pattern display region: horizontal start

2.10.5.53 OSD2 Pattern_Fill Position, Vertical Start LSB Register

Address Offset: OSD2_3Ah Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Patt_VStart[7:0]	Allowable pattern display region: vertical start

2.10.5.54 OSD2 Pattern_Fill Position, Vertical Start MSB Register

Address Offset: OSD2_3Bh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	Patt_VStart[10:8]	Allowable pattern display region: vertical start

2.10.5.55 OSD2 Pattern_Fill Position, Horizontal End LSB Register

Address Offset: OSD2_3Ch Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Patt_HEnd[7:0]	Allowable pattern display region: horizontal End

2.10.5.56 OSD2 Pattern_Fill Position, Horizontal End MSB Register

Address Offset: OSD2_3Dh Access: Read/Write
Default Value: 01h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	Patt_HEnd[10:8]	Allowable pattern display region: horizontal End

2.10.5.57 OSD2 Pattern_Fill Position, Vertical End LSB Register

Address Offset: OSD2_3Eh Access: Read/Write
Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Patt_VEnd[7:0]	Allowable pattern display region: vertical End

2.10.5.58 OSD2 Pattern_Fill Position, Vertical End MSB Register

Address Offset: OSD2_3Fh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	Patt_VEnd[10:8]	Allowable pattern display region: vertical End

2.10.5.59 OSD2 Block Write Data LSB Register

Address Offset: OSD2_40h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	OSD2_BlockWr_D[7:0]	LSB Data to be block fill

2.10.5.60 OSD2 Block Write Data MSB Register

Address Offset: OSD2_41h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	OSD2_BlockWr_D[15:8]	MSB Data to be block fill

2.10.5.61 OSD2 Block Write Starting Address LSB Register

Address Offset: OSD2_42h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	OSD2_BlockWr_SA[7:0]	Starting Address of block fill

2.10.5.62 OSD2 Block Write Starting Address MSB Register

Address Offset: OSD2_43h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:0]	R/W	OSD2_BlockWr_SA[13:8]	Starting Address of block fill

2.10.5.63 OSD2 Block Write Length Register

Address Offset: OSD2_44h Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	OSD2_BlockWr_L[7:0]	Block fill length (count)

2.10.5.64 OSD2 Block Write Control Register

Address Offset: OSD2_45h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	WO/ RO	OSD2_BlockWr_Trig OSD2_BlockWr_Done	Set to 1 to trigger block fill operation Get 1 means the block fill operation is done
[6]	R/W	OSD2_BlockWr_mode	
[5:0]	R/W	OSD2_BlockWr_L[13:8]	Block fill length (count)

2.11 TCON(Timing Control)

2.11.1 LCD Panel Pin Assignment

In this section, we illustrate those pins connected to AU 7" TFT-LCD panel module in a T138 video system.

Table 2-19 T138 Rotation Control and LCD Panel Scanning Direction

L/R	U/D	STH	STV	Reg 0xE1	Scanning Direction
1	1	STH2	STV1	0xBC	Down-to-up, left-to-right
1	0	STH2	STV2	0xF4	Up-to-down, left-to-right
0	1	STH1	STV1	0xA8	Down-to-up, right-to-left
0	0	STH1	STV2	0xE0	Up-to-down, right-to-left

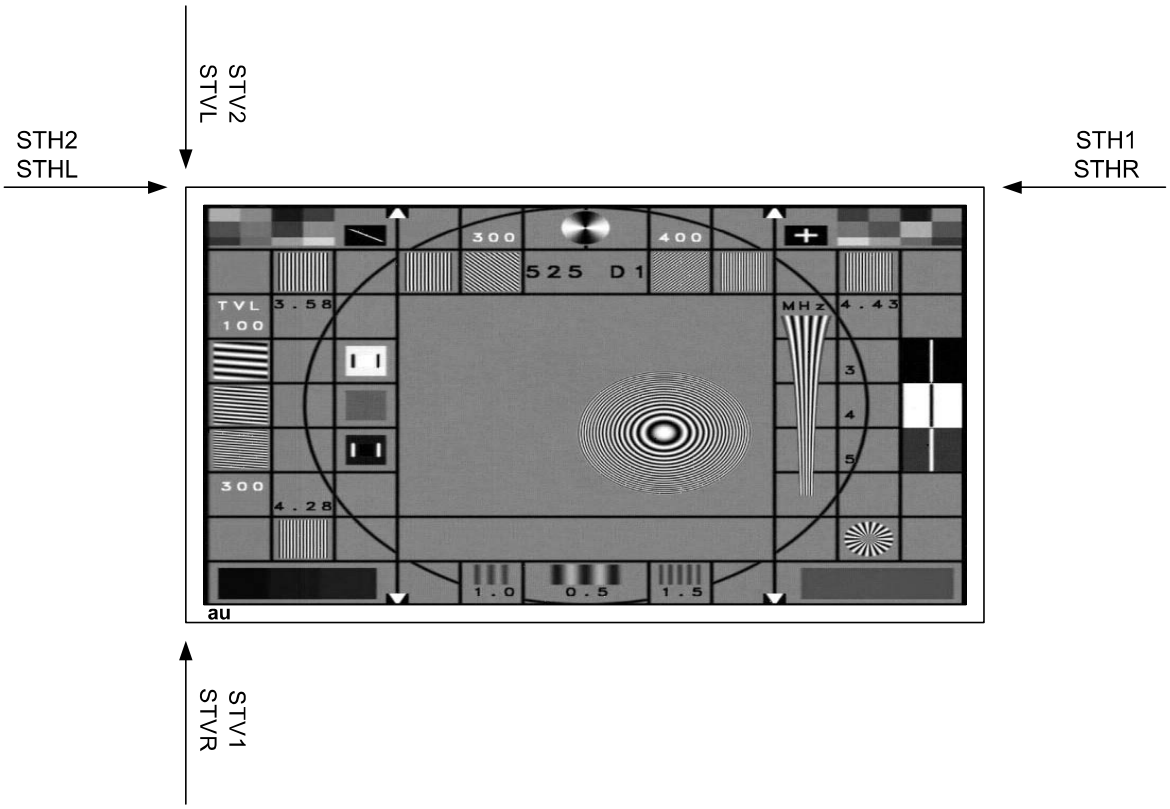


Figure 2-12 Scanning Direction of AU 7" panel

2.11.2 TCON Timing

T138 is designed for analog LCD panel. Each 24-bit color pixel must be converted into analog voltage via built-in triple DACs. The Table 2-1 shows a typical setting for AU 7" panel with 10-Mhz operation clock.

Table 2-1 T138 TCON Register Set (C8 =1Bh, C9=03, CA=03h)

Reg	Reg value	Operation
0x20	0x21	Line-inverted Control
0x21	0x79	Polarity Control
0x23,0x22	0x022D	Placement of OEH
0x24	0x0C	Duration of OEH
0x26,0x25	0x024B	Placement of POL
0x28,0x27	0x021C	Placement of GCLK
0x2A,0x29	0x0029	Duration of GCLK
0x2B	0x01	Placement of STH
0x30	0x01	Enable Placement of STV
0x32,0x31	0x01FB	Placement of GOE
0x34,0x33	0x0037	Duration of GOE
0x35	0x06	Placement of STV

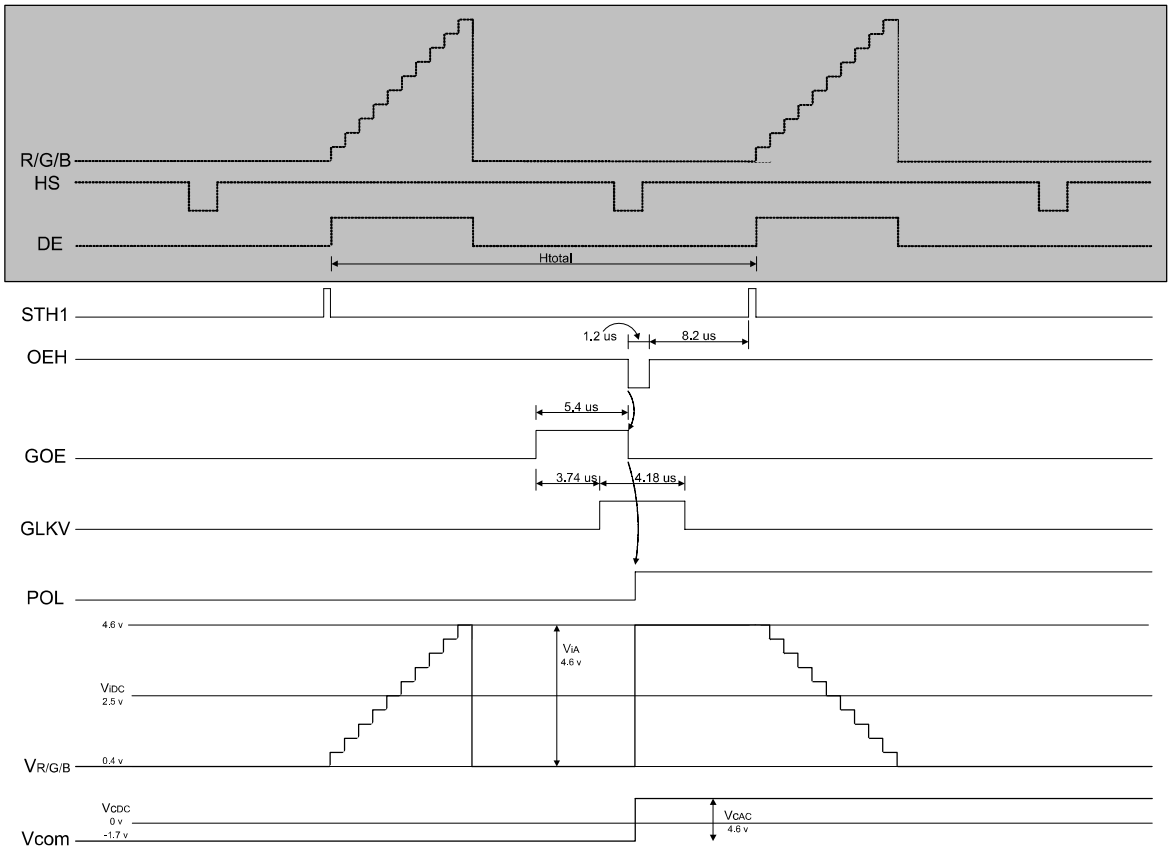


Figure 2-13 AU 7" TCON Timing Spec

The waveforms shown below illustrate TCON location counting. Each TCON signal's placement and duration are allowed to program. On the Figure 2-14, the pulse placement starts counting at the leading edge of DE. After placement counter meets the value we give to {P1_27h,P1_28h}, the duration counter starts to count until the duration meets {P1_29h,P1_2Ah}. All of location counting uses CLKO as counter clock.

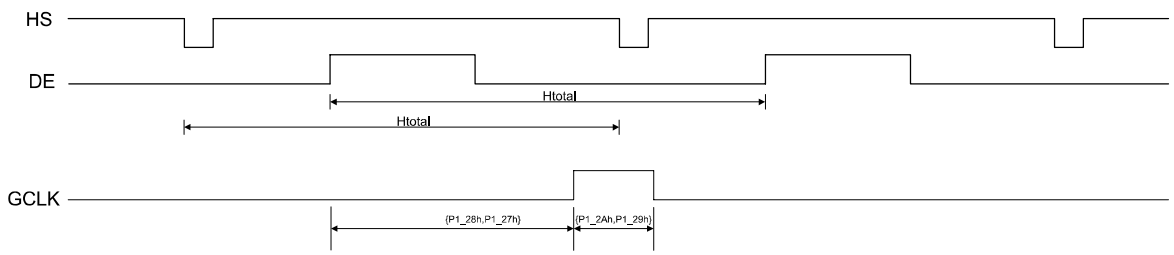


Figure 2-14 Location Counting of GCLK

3 Register Description

Serial Bus Register Set Page 0

3.1 ADC Register Set

3.1.1 Channel R Clamp Voltage Selection Register

Address Offset: 00h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	R_ClampVolt_Sel[2:0]	Channel red clamp voltage selection

3.1.2 Channel G Clamp Voltage Selection Register

Address Offset: 01h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	G_ClampVolt_Sel[2:0]	Channel green clamp voltage selection

3.1.3 Channel B Clamp Voltage Selection Register

Address Offset: 02h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	B_ClampVolt_Sel[2:0]	Channel blue clamp voltage selection

3.1.4 Sync Tip Clamp Register

Address Offset: 04h Access: Read/Write
Default Value: 2Fh Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	R/W	STip_ClampPlacement	Sync. tip clamp placement
[4:0]	R/W	STip_ClampDuration	Sync. tip clamp duration

3.1.5 Channel R Offset Tune Register

Address Offset: 05h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	DC_Cal_Blank	
[6]	R/W	B_Decrease	Channel blue decrease (1) or increase (1) by B_Offset_Tune[3:0]
[5]	R/W	G_Decrease	Channel green decrease (1) or increase (1) by G_Offset_Tune[3:0]
[4]	R/W	R_Decrease	Channel red decrease (1) or increase (1) by R_Offset_Tune[3:0]
[3:0]	R/W	R_Offset_Tune[3:0]	Channel red offset fine tune

3.1.6 Channel G, B Offset Tune Register

Address Offset: 05h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	B_Offset_Tune[3:0]	Channel blue offset fine tune
[3:0]	R/W	G_Offset_Tune[3:0]	Channel green offset fine tune

3.1.7 ADC Channel 0 Static Gain

Address Offset: 07h Access: Read/Write
Default Value: FFh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	ADCRSG	This register can set a fixed gain for ADC channel 0 when static gain control is enabled

3.1.8 ADC Channel 1 Static Gain

Address Offset: 08h Access: Read/Write
Default Value: FFh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	ADCGSG	This register can set a fixed gain for ADC channel 1 when static gain control is enabled

3.1.9 ADC Channel 2 Static Gain

Address Offset: 09h Access: Read/Write
Default Value: FFh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	ADCBSG	This register can set a fixed gain for ADC channel 2 when static gain control is enabled

3.1.10 ADC Channel 0 Offset

Address Offset: 0Ah Access: Read/Write
Default Value: 60h Size: 8 bits

Bit	Access	Symbol	Description
[7:2]	R/W	ADC_ROFF	ADC Channel 0 DC Offset Control
[1:0]	RO	Reserved	

3.1.11 ADC Channel 1 Offset

Address Offset: 0Bh Access: Read/Write
Default Value: 60h Size: 8 bits

Bit	Access	Symbol	Description
[7:2]	R/W	ADC_GOFF	ADC Channel 1 DC Offset Control
[1:0]	RO	Reserved	

3.1.12 ADC Channel 2 Offset

Address Offset: 0Ch Access: Read/Write
Default Value: 60h Size: 8 bits

Bit	Access	Symbol	Description
[7:2]	R/W	ADC_BOFF	ADC Channel 2 DC Offset Control
[1:0]	RO	Reserved	

3.1.13 ADC General Control Configuration Register

Address Offset: 0Dh Access: Read/Write
Default Value: 20h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	CLPMD[1:0]	Clamping mode Mode: Type 0, 3: Fixed window 1, 2: Locked Window
[5]	R/W	DCEN	DC Clamping Enable
[4]	R/W	DCSEL	Clamping Source Selection
[3]	R/W	Reserved	Test only, vmode
[2]	RO	DC_CAL_RDY	DC Calibration Ready
[1]	R/W	DC_CALEN	DC Calibration Enable
[0]	R/W	DC_CALMD	DC Calibration Mode Mode: Type 0: minimum 1: average

3.1.14 ADC Gain ReadBack

Address Offset: 0Eh Access: Read Only
Default Value: - Size: 6 bits

Bit	Access	Symbol	Description
[7:0]	R	adc_auto_gain	ADC automatic gain control read back.

3.1.15 ADC Power Down Control

Address Offset: 0Fh Access: Read/Write
Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	PwDn_SOY	1 for Power down SOY slicer
[6]	R/W	PD2 (B)	1: Power down 0: Power up
[5]	R/W	PD1 (G)	1: Power down 0: Power up
[4]	R/W	PD0 (R)	1: Power down 0: Power up
[3:0]	R/W	Reserved	

3.1.16 ADC Polarity Control

Address Offset: 10h Access: Read/Write
Default Value: E8h Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO/WO	HSi_Polarity / HSi_Inv_	When Read: get input HSync polarity When writing, to invert (0) or non-invert (1) input HSync
[6]	RO/WO	VSi_Polarity / VSi_Inv_	When Read: get input VSync polarity When writing, to invert (0) or non-invert (1) input VSync
[5]	R/W	Reserved	
[4]	R/W	Auto_Polarity	Set to 1 for enabling auto-adjusting HSync/VSync polarity.
[3]	R/W	Clamp_Polarity	Set to 1 for controlling Clamp positive polarity.
[2]	R/W	Clamp_Sel_GfbHS	Set to 1 to use PLL feedback HSync as clamp reference
[1]	R/W	Clamp_Leading	Set to 1 to use leading edge of HSync as clamp reference point.
[0]	R/W	Clamp_Sel_RGB	Clamp control by: 1: RGB/SOY logic, 0: VD logic.

3.1.17 YPbPr Clamping Control Register

Address Offset: 11h Access: Read/Write
Default Value: 98h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	R/W	Reserved	
[2]	R/W	BSCALE	ADC Channel 2 Clamping Mode 0: Clamp to Ground; 1: Clamp to mid-scale
[1]	R/W	GSCALE	ADC Channel 1 Clamping Mode 0: Clamp to Ground; 1: Clamp to mid-scale
[0]	R/W	RSCALE	ADC Channel 0 Clamping Mode 0: Clamp to Ground; 1: Clamp to mid-scale

3.1.18 VSync Separation Register

Address Offset: 13h Access: Read/Write
Default Value: 08h Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO	CSync_Detect_Done	flag of whether CSync Detection is done or not
[6]	RO	Fs_TooFast	Get 1 if CSync Detecting operation clock is too fast
[5]	R/W	En_CSync_Detect	Set to 1 for enabling CSync Detection function
[4]	R/W	Reserved	Reserved for chip testing, should set 0 for normal operation
[3]	R/W	Reserved	Reserved for special case, set to 1 for normal conditions
[2]	R/W	Reserved	Reserved for special case, set to 0 for normal conditions
[1:0]	R/W	Div_To14[1:0]	00b: power down or reset, 01b: XCLK/1, 10b:XCLK/2 (normal operation for XCLK=27MHz); 11b: XCLK/3

3.1.19 Sync Routine Control

Address Offset: 14h Access: Read/Write
Default Value: D1h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	HS2PLL_Polarity	HRef polarity
[6]	R/W	Coast2PLL_Polarity	Coast polarity
[5]	R/W	ADC_is_RGB	ADC Color space select: Set 1 for RGB input, 0 for YPbPr input.
[4]	R/W	HSo_Sel_Fdbk	ADC HSo source from PLL when set to 1
[3]	R/W	HRef_Sel_SOY	PLL HRef from: 1: SOY Slicer (SOY); 0: HS input pin (SS/CS)

[2]	R/W	VS_Sel_Sep	ADC VSo from: 1: VSync Detect (SOY/CS); 0: VS input pin (SS)
[1]	R/W	Coast_Sel_Sep	PLL Coast from: 1: VSync Detect (SOY/CS); 0: Ground (SS)
[0]	R/W	Reserved	Should keep in “0”

3.1.20 Line Lock PLL Divider Register 1

Address Offset: 15h Access: Read/Write
Default Value: 5Ah Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	APLL_Div[7:0]	PLL divider LSB

3.1.21 Line Lock PLL Divider Register 2

Address Offset: 16h Access: Read/Write
Default Value: C3h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	APLL_PowerDown	1: power down, 0: enable
[6]	R/W	APLL_Sel_HighFreq	Reserved for testing, 1: high freq., 0: low freq.
[5]	R/W	APLL_Reset	1: Reset Line-lock PLL 0: normal operation for RGB and SOY inputs
[4]	RO	ADC_Clock_From	ADC clock source: 1: XCLK; 0:APLL output
[3:0]	R/W	APLL_Div[11:8]	PLL divider MSB

3.1.22 VCO & Charge Pump Register

Address Offset: 17h Access: Read/Write
Default Value: 48h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	ADC_VCO	
[5:3]	R/W	ADC_ChargePump	
[2]	R/W	AutoClampV_B	1: internal auto mid-clamp, 0: external mid-clamp
[1]	R/W	AutoClampV_G	1: internal auto mid-clamp, 0: external mid-clamp
[0]	R/W	AutoClampV_R	1: internal auto mid-clamp, 0: external mid-clamp

3.1.23 Analog Source MUX Selection

Address Offset: 18h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:4]	R/W	AI2SEL (B)	Analog mux selection for ADC channel 2 00: ACB1 01: ACB0 1x: ACB2
[3:2]	R/W	AI1SEL (G)	Analog mux selection for ADC channel 1 00: AY1 01: AY0 1x: AY2
[1:0]	R/W	AI0SEL (R)	Analog mux selection for ADC channel 0 00: ACR1 01: ACR0 1x: ACR2

3.1.24 Y/Cb/Cr Data Switching Control

Address Offset: 19h Access: Read/Write
Default Value: 07h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:4]	R/W	CBINSEL	The digitaized CB or B data can be taken from one of 3 ADCs: 00: ADC Ch0 01: ADC Ch1 1X: ADC Ch2
[3:2]	R/W	YINSEL	The digitaized Y or Composite or G data can be taken from one of 3 ADCs: 00: ADC Ch0 01: ADC Ch1 1X: ADC Ch2
[1:0]	R/W	CRINSEL	The digitaized CR or Chroma or R data can be taken from one of 3 ADCs: 00: ADC Ch0 01: ADC Ch1 1X: ADC Ch2

3.1.25 ADC Analog AGC Selection

Address Offset: 1Ah Access: Read/Write
Default Value: 87h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	AGC_GAINMD	<table><tr><th>Mode</th><th>Type</th></tr><tr><td>0</td><td>Positive gain</td></tr><tr><td>1</td><td>Positive gain 1x~2x</td></tr><tr><td>2</td><td>Negative gain 1x~2x</td></tr><tr><td>3</td><td>Negative gain</td></tr></table>
[5:3]	RO	Reserved	
[2]	R/W	CB_AGC_SEL	If 0, refer to ADCBSG (P0_09h): 0: Static gain; 1: Dynamic gain
[1]	R/W	Y_AGC_SEL	If 0, refer to ADCGSG (P0_08h) 0: Static gain; 1: Dynamic gain
[0]	R/W	CR_AGC_SEL	If 0, refer to ADCRSG (P0_07h) 0: Static gain; 1: Dynamic gain

3.1.26 Blank Sync Level

Address Offset: 1Ch Access: Read/Write
Default Value: F0h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	BLANK_SL	

3.1.27 ADC Phase Setting Register

Address Offset: 20h Access: Read/Write
Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	R/W	ADC_Phase[4:0]	32 phases per clock
[2]	R/W	ADC_Clk_Div2	Clock divided by 2 if set to 1
[1]	R/W	ADC_Clk_Dly	Clock delay if set to 1
[0]	R/W	ADC_Clk_Inv	Clock inverted if set to 1

3.1.28 ADC Detection Register

Address Offset: 21h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO/WO	Done_ATK / En_ATK	When read: get flag of Phases Tracking finish or not When write, to enable Phases Tracking
[6:5]	R/W	ATK_Channel[1:0]	Select which channel to perform ATK: 00: R+G+B 01: R 10: G 11: B
[4:3]	RO	Reserved	
[2]	RO/WO	Done_Exist_ADC / En_Exist_ADC	When read: get flag of Checking ADC HS/VS finish or not When write, to enable Checking ADC HS/VS
[1]	RO	Exist_HSync	HSync input toggle when read 1
[0]	RO	Exist_VSync	HSync input toggle when read 1

3.1.29 ADC Phase Tracking Register 1

Address Offset: 22h Access: Read Only
Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	ATK_Accu[7:0]	Accumulated Phase Tracking Result

3.1.30 ADC Phase Tracking Register 2

Address Offset: 23h Access: Read Only
Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	ATK_Accu[15:8]	Accumulated Phase Tracking Result

3.1.31 ADC Phase Tracking Register 3

Address Offset: 24h Access: Read Only
Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	ATK_Accu[23:16]	Accumulated Phase Tracking Result

3.1.32 Boundary Control Register

Address Offset: 26h Access: Read/Write
Default Value: 04h Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO/WO	Done_Boundary / En_Boundary	When read: get flag of Boundary Detection finish or not When write, to enable Boundary Detection
[6]	R/W	Boundary_hDE	Check boundary when: 0: in all range 1: in HDE window
[5:3]	R/W	Boundary_Mask_HS_L	Set the do not care range near HSync leading edge
[2:0]	R/W	Boundary_Mask_HS_T	Set the do not care range near HSync trailing edge

3.1.33 Boundary Control Register

Address Offset: 27h Access: Read/Write
Default Value: 40h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Boundary_Threshold	Set the color threshold for boundary detection

3.1.34 Boundary Left LSB Register

Address Offset: 28h Access: Read Only
Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	Left_Bound[7:0]	Left Boundary Position

3.1.35 Boundary Left MSB Register

Address Offset: 29h Access: Read Only
Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	RO	Left_Bound[10:8]	Left Boundary Position

3.1.36 Boundary Right LSB Register

Address Offset: 2Ah Access: Read Only
Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	Right_Bound[7:0]	Right Boundary Position

3.1.37 Boundary Right MSB Register

Address Offset: 2Bh Access: Read Only
Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	RO	Right_Bound[10:8]	Right Boundary Position

3.1.38 Boundary Top LSB Register

Address Offset: 2Ch Access: Read Only
Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	Top_Bound[7:0]	Top Boundary Position

3.1.39 Boundary Top MSB Register

Address Offset: 2Dh Access: Read Only
Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	RO	Top_Bound[10:8]	Top Boundary Position

3.1.40 Boundary Bottom LSB Register

Address Offset: 2Eh Access: Read Only
Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	Bottom_Bound[7:0]	Bottom Boundary Position

3.1.41 Boundary Bottom MSB Register

Address Offset: 2Fh Access: Read Only
Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	RO	Bottom_Bound[10:8]	Bottom Boundary Position

3.2 Input Timing Register Set

3.2.1 De-Interlaced Process & Vertical Shadow Control Register

Address Offset: 30h Access: Read/Write
Default Value: 82h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5]	R/W	VST_CHGSEL	1:Vsync timing change determined by 8*# of XCLK 0:Vsync timing change determined by # of hsync (default) # can be assigned at Reg 0x3A
[4]	R/W	INT_EDGE	Interrupt polarity 1: positive 0: negative (default)
[3]	R/W	LB_SIZE_FIXED	This bit control capture size for Scaler. 1: Hsize and Vsize are assigned by 54h ~57h 0: sizes assigned by input sources. (default)
[2]	R/W	ENQKHS	Reserved for chip teset only, set to 0 for normal operation
[1]	R/W	ITLCPRO	Set 1 for interlaced video (default) Set 0 for non-interlaced video
[0]	R/W	ADC_Odd_in_HsVs	Set to 1 for enabling detecting Odd flag from HS/VS pins

3.2.2 Source Select Register

Address Offset: 31h Access: Read/Write
Default Value: 04h Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO	ITLCFLM	Indicates incoming video signal is interlaced if get 1
[6:4]	R/W	VIP_Sel[2:0]	Select the digital input source (VIP: Video Input): 000: A656 001: B656 010: L601_8bits 011: L601_16bits 100: Reserved 101: RGB565 110: RGB666 111: RGB888
[3:2]	R/W	InSource_Sel[1:0]	Select the input source: 00: Digital VIP input 01: select VD input (CVBS, S-Video, YPbPr) 10: Select ADC RGB, SOY(YPbPr) 11: Reserved
[1]	RO	Reserved	
[0]	RO	VBI_Field	Current VBI field information

3.2.3 Interrupt Status Register

Address Offset: 32h Access: Read-only / Write-1-to-clear
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO/W1C	INTSTS	Read to get interrupt trigger source, Write 1 to clear it. [7]: IR packet received [6]: VBI packet is valid for processing [5]: Every VSync Leading Edge [4]: Timer time out [3]: HSync Timing Changed [2]: VSync Timing Changed [1]: Lost HSync [0]: Lost VSync

3.2.4 Interrupt Mask Register

Address Offset: 33h Access: Read/Write
Default Value: FFh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	INTMASK	Set to 1 for masking relative interrupt trigger source: [7]: IR packet received [6]: VBI packet is valid for processing [5]: Every VSync Leading Edge [4]: Timer time out [3]: HSync Timing Changed [2]: VSync Timing Changed [1]: Lost HSync [0]: Lost VSync

3.2.5 Interrupt Status/Mask 2 Register

Address Offset: 34h Access: Read/Write
Default Value: 60h Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6]	R/W	Mask_ ShortVS_FreeRun	Set to 1 for masking interrupt trigger source of ShortVS_FreeRun_Trig
[5]	RO	Mask TP_Move	Set to 1 for masking interrupt trigger source of TouchPanel Moving
[4]	RO	Reserved	
[3]	RO	Reserved	
[2]	RO/W1C	ShortVS_FreeRun_Trig	Read to get ShortVS interrupt status, Write 1 to clear it
[1]	RO/W1C	TouchPanel_Move	Read to get TP_Move interrupt status, Write 1 to clear it
[0]	RO	SARn_Toggle	Read to get SARn_Toggle interrupt status

3.2.6 1ms Timer LSB Register

Address Offset: 35h Access: Read/Write
Default Value: BCh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	TM_1MS_L [7:0]	Lower byte of the number of XCLK's in half 1ms.

3.2.7 1ms Timer MSB Register

Address Offset: 36h Access: Read/Write
Default Value: 34h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	TM_1MS_H [15:8]	Higher byte of the number of XCLK's in half 1ms.

3.2.8 VSYNC Missing Counter Register

Address Offset: 37h Access: Read/Write
Default Value: 40h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	V_MISS_CNT	When no VSync toggle during this value * 1ms, trigger interrupt

3.2.9 HSYNC Missing Counter LSB Register

Address Offset: 38h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	H_MISS_CNT_L[7:0]	When no HSync toggle during this value * XCLK, trigger interrupt

3.2.10 HSYNC Missing Counter MSB Register

Address Offset: 39h Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	H_MISS_CNT_L[15:8]	

3.2.11 VSYNC Delta Difference Result Register

Address Offset: 3Ah Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	VSYNC_DLT[7:0]	When VSync period varies more than this value, trigger interrupt

3.2.12 HSYNC Delta Difference Result Register

Address Offset: 3Bh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HSYNC_DLT[7:0]	When HSync period varies more than this value, trigger interrupt

3.2.13 VD/656 Left Border Crop Register

Address Offset: 3Ch Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:0]	R/W	CROP_LEFTB	Remove noisy pixels appearing on left border. 1LSB =1 pixel

3.2.14 VD/656 VSync Offset Register

Address Offset: 3Dh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	VD_VsOfs_Mode	VD/656 VSync Offset mode: 0: Crop Top Border 1: VSync Offset, delay lines
[6]	RO	Reserved	
[5:0]	R/W	VD_VsOffset	Remove noisy pixels appearing on top border or re-shape VSync 1LSB =1 line, value 0 means disable.

3.2.15 VD/656 Left Border Crop Register

Address Offset: 3Eh Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	En_VD_VsOfs_P1	Enable VSync Offset add 1 line for even or odd field on VD path
[6]	R/W	VD_VsOfs_on_Odd	Set to 1 for selecting VD VSync Offset delay 1 line on Odd field; Set to 0 for Even field. This bit works only when En_VD_VsOfs_P1=1.
[5:0]	R/W	VD_VsBP	VD/656 VSync Back Proch (# lines)

3.2.16 Input Sync Signal Detection Register

Address Offset: 3Fh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	HSTLSPVS	1:use trailing edge of hsync to sample 0:use leading edge of hsync to sample
[6]	R/W	AUTOVSD6	When the edges of vsync and hsync are too close, input detection circuit can delay vsync 6 cycle of XCLK to avoid unstable detection 1:Automatically delay 6 cycles of XCLK if CFSEEDGE is true. 0:Dealy 6 cycles of XCLK if FCVSD6 is true
[5]	R/W	FCVSD6	AUTOVSD6 FCSVSD6T 1 x Automatically delay VSync 6 XCLK if CFSEEDGE is true 0 1 Force to delay VSync 6 XCLK 0 0 No Vsync Dealy
[4]	RO	CFSEEDGE	VS and HS edges are too close.
[3]	RO	HS_Polarity	Detected HSync polarity (for Analog RGB raw input)
[2]	RO	VS_Polarity	Detected VSync polarity (for Analog RGB raw input)
[1:0]	RO	Reserved	

3.2.17 ADC Sync Offset Control Register

Address Offset: 40h Access: Read/Write
Default Value: D0h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	En_HsOffset	Set to 1 for enabling ADC HSync Offset.
[6]	R/W	En_VsOffset	Set to 1 for enabling ADC VSync Offset.
[5]	R/W	En_VsOfs_Evn_P1	Set to 1 for enabling ADC VSync Offset delay 1 line for even field.
[4]	R/W	SOY_Odd_Inv_	Set to 0 for inverting SOY Odd field flag.
[3:2]	RO	Reserved	
[1]	R/W	RGB_PowerDown_	Set to 0 for power down RGB related logic. 1 for enabling RGB path.
[0]	R/W	HS_in_SyncSel	Select the sampling edge of HSync pin.

3.2.18 ADC HSync Offset LSB Register

Address Offset: 41h Access: Read/Write
Default Value: 02h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HsOffset[7:0]	Delay ADC HSync by # dots.

3.2.19 ADC HSync Offset MSB Register

Address Offset: 42h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	HsOffset[10:8]	Delay ADC HSync by # dots.

3.2.20 ADC VSync Offset LSB Register

Address Offset: 43h Access: Read/Write
Default Value: 01h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	VsOffset[7:0]	Delay ADC VSync by # lines.

3.2.21 ADC VSync Offset MSB Register

Address Offset: 44h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	VsOffset[10:8]	Delay ADC VSync by # lines.

3.2.22 ADC HSync Offset Pulse Width Register

Address Offset: 45h Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HsPulseWidth[7:0]	Pulse width of the regenerated ADC HSync (# dots).

3.2.23 ADC VSync Offset Pulse Width Register

Address Offset: 46h Access: Read/Write
Default Value: 01h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	RO	Reserved	
[3:0]	R/W	VsPulseWidth[3:0]	Pulse width of the regenerated ADC VSync (# lines).

3.2.24 ADC Capture Control Register

Address Offset: 47h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	Mask_H_Left	Set to 1 for mask left portion when wrap.
[6]	R/W	Mask_H_Right	Set to 1 for mask right portion when wrap.
[5]	R/W	Mask_V_Top	Set to 1 for mask top portion when wrap.
[4]	R/W	Mask_V_Bottom	Set to 1 for mask bottom portion when wrap.
[3:1]	RO	Reserved	
[0]	R/W	Reserved	Reserved for chip test only

3.2.25 ADC Capture HSize LSB Register

Address Offset: 48h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	ADC_HSize[7:0]	ADC Capture window: Horizontal Size (# dots).

3.2.26 ADC Capture HSize MSB Register

Address Offset: 49h Access: Read/Write
Default Value: 02h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	ADC_HSize[10:8]	ADC Capture window: Horizontal Size (# dots).

3.2.27 ADC Capture VSize LSB Register

Address Offset: 4Ah Access: Read/Write
Default Value: E0h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	ADC_VSize[7:0]	ADC Capture window: Vertical Size (# lines).

3.2.28 ADC Capture VSize MSB Register

Address Offset: 4Bh Access: Read/Write
Default Value: 01h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	ADC_VSize[10:8]	ADC Capture window: Vertical Size (# lines).

3.2.29 ADC Capture HSync Back Porch LSB Register

Address Offset: 4Ch Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	ADC_HStart[7:0]	ADC Capture window: Horizontal Start Point (# dots).

3.2.30 ADC Capture HSync Back Porch MSB Register

Address Offset: 4Dh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	ADC_HStart[10:8]	ADC Capture window: Horizontal Start Point (# dots).

3.2.31 ADC Capture VSync Back Porch LSB Register

Address Offset: 4Eh Access: Read/Write
Default Value: 05h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	ADC_VStart[7:0]	ADC Capture window: Vertical Start Point (# linees).

3.2.32 ADC Capture VSync Back Porch MSB Register

Address Offset: 4Fh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	ADC_VStart[10:8]	ADC Capture window: Vertical Start Point (# linees).

3.2.33 VSYNC Timing Measurement Register

Address Offset: 50h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	FreeRun_Sel_cvd	1: Use cvd signal to enter FreeRun; 0: ShortVS
[6]	R/W	HSPMD	Register 0x5c and 0x5d can be HS pulse width or HSync period 1: Period in # of pixel clock. 0: HSync pulse width in # of pixel clock.
[5]	RO	DONE_FRMXCLKCNT	When EN_FRAMEXCLKCNT is enabled, a whole frame time can be obtained through XCLK counting. See registers 0x51, 0x52 and 0x53. After this bit read back as 1, then clear EN_FRAMEXCLKCNT first before reading 0x51~0x53 values.
[4]	R/W	EN_FRAMEXCLKCNT	When input VSync changes, enable this bit to start measurement on VSync using XCLK.
[3]	R/W	Reserved	
[2]	RO	In_ShortVS_FreeRun	Status indicator of whether it is in Free-run which caused by short VS
[1]	R/W	VsPeriod_Rd_SetShort	Register 0x5A and 0x5B read back from: 1: Programmed threshold for VS period 0: VSync period in # of lines
[0]	R/W	ShortVS_Check_En	Set to 1for enabling monitoring VS period

3.2.34 VSync Period Measurement L Register

Address Offset: 51h Access: Read Only
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	FRMXCLK_SUM[7:0]	VSync Period, count by XCLK

3.2.35 VSync Period Measurement M Register

Address Offset: 52h Access: Read Only
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	FRMXCLK_SUM[15:8]	

3.2.36 VSync Period Measurement H Register

Address Offset: 53h Access: Read Only
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	RO	Reserved	
[4:0]	RO	FRMXCLK_SUM[20:16]	

3.2.37 Input HSize LSB Register

Address Offset: 54h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO or R/W	Inp_HSize[7:0]	This register is: Read Only, when P0_30h<3>=0, showing input image HSize Read/Write, when P0_30h<3>=1, over-write HSize.

3.2.38 Input HSize MSB Register

Address Offset: 55h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	RO or R/W	Inp_HSize[10:8]	

3.2.39 Input VSize LSB Register

Address Offset: 56h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO or R/W	Inp_VSize[7:0]	This register is: Read Only, when P0_30h<3>=0, showing input image VSize Read/Write, when P0_30h<3>=1, over-write VSize.

3.2.40 Input VSize MSB Register

Address Offset: 57h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	RO or R/W	Inp_VSize[10:8]	

3.2.41 HSync Period LSB Register

Address Offset: 58h Access: Read Only
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	Hs_Period[7:0]	32x HSync period, counted by XCLK

3.2.42 HSync Period MSB Register

Address Offset: 59h Access: Read Only
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	Hs_Period[15:8]	32x HSync period, counted by XCLK

3.2.43 VSync Period LSB Register

Address Offset: 5Ah Access: Read/Write
Default Value: FFh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO or R/W	Vs_Period[7:0]	This register is: RO, when P0_50h<2>=0, showing input VSync period (by lines) R/W, when P0_50h<2>=1, programmed ShortVS threshold

3.2.44 VSync Period MSB Register

Address Offset: 5Bh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2]	RO	Vs_Period[10]	
[1:0]	RO or R/W	Vs_Period[9:8]	

3.2.45 HSync Pulse Width LSB Register

Address Offset: 5Ch Access: Read Only
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	Hs_Width[7:0]	HSYNC pulse width or period counted by dot clock See HSPMD (P0_50h<6>) for detail.

3.2.46 HSync Pulse Width MSB Register

Address Offset: 5Dh Access: Read Only
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	RO	Hs_Width[10:8]	HSYNC pulse width or period counted by dot clock

3.2.47 VSYNC Pulse Width LSB Register

Address Offset: 5Eh Access: Read Only
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	Vs_Width[7:0]	VSYNC pulse width counted by input HSYNC

3.2.48 VSYNC Pulse Width MSB Register

Address Offset: 5Fh Access: Read Only
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	RO	Vs_Width[10:8]	VSYNC pulse width counted by input HSYNC

3.3 Picture Enhancement Register Set

3.3.1 DCTI Control Register

Address Offset: 60h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2]	R/W	DCTi_Dist_Sel	DCTI distance selection: 1 for longer distance
[1]	RO	Reserved	
[0]	R/W	DLTi_Dist_Sel	DLTI distance selection: 1 for longer distance

3.3.2 Peaking Register

Address Offset: 61h Access:
Default Value: 08h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	Peaking_En	Enable Peaking function
[6]	R/W	Peaking_LR_Disable	Peaking boundary mode
[5:0]	R/W	Peaking_Coring	

3.3.3 Peaking Band-Pass Coefficient Register

Address Offset: 62h Access:
Default Value: 04h Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	RO	Reserved	
[4:0]	R/W	Peaking_BP_Coef	

3.3.4 Peaking High-Pass Coefficient Register

Address Offset: 63h Access:
Default Value: 04h Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	RO	Reserved	
[4:0]	R/W	Peaking_HP_Coef	

3.3.5 Peaking Low-Pass Coefficient Register

Address Offset: 64h Access:
Default Value: 02h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	WLE_Gain[3:0]	
[3]	RO	Reserved	
[1:0]	R/W	Peaking_LP_Coef	

3.3.6 DCTI_0 Gain and Coring Register

Address Offset: 65h Access: Read/Write
Default Value: 08h Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	R/W	DCTI_GAIN_0	
[4:0]	R/W	DCTI_CO_0	

3.3.7 DCTI_1 Gain and Coring Register

Address Offset: 66h Access: Read/Write
Default Value: 08h Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	R/W	DCTI_GAIN_1	
[4:0]	R/W	DCTI_CO_1	

3.3.8 Cb/Cr Delay control

Address Offset: 67h Access: Read/Write
Default Value: 1Eh Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	U_delay	Cb signal delay control. 0: no delay (default) 1: 1 pixel delay
[6:5]	R/W	V_delay	Cr signal delay control. 00: no delay (default) 01: 1 pixel delay 10: 2 pixel delay 11: 3 pixel delay
[4:0]	R/W	DCTI_Threshold	DCTI performing Threshold Limit

3.3.9 Contrast Adjust Register

Address Offset: 68h Access: Read/Write
Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	LumaCON	

3.3.10 Brightness Adjust Register

Address Offset: 69h Access: Read/Write
Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	LumaBRI	

3.3.11 Hue Sin Adjust Register

Address Offset: 6Ah Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HueSin	

3.3.12 Hue Cos Adjust Register

Address Offset: 6Bh Access: Read/Write
Default Value: 7Fh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HueCos	

3.3.13 Chroma Saturation Adjust Register

Address Offset: 6Ch Access: Read/Write
Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	ChomSat	

3.3.14 White Level Expansion Threshold Register

Address Offset: 6Dh Access: Read/Write
Default Value: EBh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	WLE_TH[7:0]	

3.3.15 Black Level Expansion Threshold Register

Address Offset: 6Eh Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	BLE_TH[7:0]	

3.3.16 VIP Black level Expansion Gain / Offset Control Register

Address Offset: 6Fh Access: Read/Write
DefaultValue: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	BLE_GAIN	
[3:2]	R/W	WLE_OFFSET[1:0]	
[1:0]	R/W	BLE_OFFSET[1:0]	

3.4 Scaling Register Set

3.4.1 Scaling General Control Register

Address Offset: 70h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	Reserved	
[5]	R/W	Inv_VideoF	Inv_VideoF: Reverse input odd field control for intra-field scaling, only take action when ITLCPRO set to 1.
[4]	R/W	Dclki_is_Faster	Software need to turn this bit on when the freq of input pixel clock is higher than output pixel clock.
[3]	R/W	V_Half_En	Set to 1 if vertical downscale less than 1/2.
[2:1]	RO	Reserved	
[0]	WO	Coef_Pointer_Reset	Write 1 to reset pointer, must be performed before programming scaling coefficients.

3.4.2 Scaling Coefficient Data Port Register

Address Offset: 71h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Coef_Data_Port	Coefficient Data Port, fill all coefficient of one set in one time.

3.4.3 Horizontal Scale Step LSB Register

Address Offset: 72h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	H_Scale_Step [7:0]	

3.4.4 Horizontal Scale Step MSB Register

Address Offset: 73h Access: Read/Write
Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	H_Scale_Step [15:8]	

3.4.5 Vertical Scale Step LSB Register

Address Offset: 74h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	V_Scale_Step [7:0]	

3.4.6 Vertical Scale Step MSB Register

Address Offset: 75h Access: Read/Write
Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	V_Scale_Step [15:8]	

3.4.7 Horizontal Aspect Ratio LSB Register

Address Offset: 76h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	H_Aspect[7:0]	Horizontal Aspect Ratio [7:0]

3.4.8 Horizontal Aspect Ratio MSB Register

Address Offset: 77h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	H_Aspect_En	Horizontal Aspect Ratio Enable
[6]	R/W	HASP_Center_Enlarge	Horizontal Aspect adjusting effect: 0: Center portion shrink 1: Center portion enlarge
[5]	R/W	H_Aspect_16_Seg	Non-Linear Scaling: 0 for 8 segments; 1 for 16 segments
[4]	RO	Reserved	
[3:0]	R/W	H_Aspect[11:8]	Horizontal Aspect Ratio [11:8]

3.4.9 Low Pass Filter Register

Address Offset: 78h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	En_Half_input	Enable Low pass
[6]	RO	Reserved	
[5:4]	R/W	LP_Average[1:0]	Shift average level in Low Pass enabled
[3]	R/W	LP_Boundary_Dup	Duplicate the first dot or not
[2]	RO	Reserved	
[1:0]	R/W	LP_ShiftDot[1:0]	Shift dot count during Low Pass enabled

3.4.10 High Boost Filter Register

Address Offset: 79h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	HighBoost_Mode[1:0]	Select threshold
[5:4]	R/W	HighBoost_Coef_C[1:0]	Chroma coef. For High Boost scaling
[3:0]	R/W	HighBoost_Coef_Y[3:0]	Lumea coef. For High Boost scaling

3.4.11 High Boost Register

Address Offset: 7Ah Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	HighBoost_Corner_En	
[6]	R/W	HighBoost_MaskBlack	
[5:0]	RO	Reserved	

3.4.12 Motion Register

Address Offset: 7Ch Access: Read/Write
Default Value: 08h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	Motion_En	1: enable motion detection
[6:4]	RO	Reserved	
[3:2]	R/W	H_Continue[1:0]	Qualified thin line: 0~3: 4/8/12/16 dots
[1:0]	R/W	Init_VPhase_Sel[1:0]	2D DI shift option: 00b: 1/2; 01b:1/4; 10b:1/8; 11b:0 lines

3.4.13 Frame Color (Luma-Y) in Scaler Register

Address Offset: 7Dh Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Scale_Frame_Y[7:0]	Background (Frame) Y Color of Scaler.

3.4.14 Frame Color (Chroma-U) in Scaler Register

Address Offset: 7Eh Access: Read/Write
Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Scale_Frame_U[7:0]	Background (Frame) U Color of Scaler.

3.4.15 Frame Color (Chroma-V) in Scaler Register

Address Offset: 7Fh Access: Read/Write
Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Scale_Frame_V[7:0]	Background (Frame) V Color of Scaler.

3.4.16 Line Buffer Configuration LSB Register

Address Offset: 84h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	LBPRFL[7:0]	LBPRFL can cause a time dealy in XCLK count between the leading edge of input Vsync and leading edge of output Vsync.

3.4.17 Line Buffer Configuration MSB Register

Address Offset: 85h Access: Read/Write
Default Value: 01h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	LBPRFL[15:8]	

3.4.18 Output VSync Front Porch Remapping Register

Address Offset: 87h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	VSFPRMP	Output HSync remap amount in vertical front porch period.

3.4.19 Left Display Border Configuration LSB Register

Address Offset: 88h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HLDSPLB[7:0]	When Output pixel's index is less than HRDSPLB, output pixel value is assigned as left display border with Frame color: {FMCLRRED, FMCLRGRN , FMCLRBLU}

3.4.20 Left Display Border Configuration MSB Register

Address Offset: 89h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	HDSPLB_INV	Horizontal border is on if HDSPLB_INV is set as follows 1: HLDSPLB < Horizontal border < HRDSPLB 0: Horizontal border < HLDSPLB or it > HRDSPLB
[6]	R/w	VDSPLB_INV	Vertical border is on if VDSPLB_INV is set as follows 1: VTDSPLB < < VBDSPLB 0: Vertical border < VTDSPLB or it > VBDSPLB
[5]	R/W	HDSPLB_STY	Horizontal Border style 1: mesh 0: solid
[4]	R/W	VDSPLB_STY	Vertical Border style 1: mesh 0: solid
[3]	RO	Reserved	
[2:0]	R/W	HLDSPLB[10:8]	Refer to P0_8Ah

3.4.21 Right Display Border Configuration LSB Register

Address Offset: 8Ah Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HRDSPLB[7:0]	When Output pixel's index is greater than HRDSPLB, output pixel value is assigned as right display border with Frame color

3.4.22 Right Display Border Configuration MSB Register

Address Offset: 8Bh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	HRDSPLB[10:8]	

3.4.23 Top Display Border Configuration LSB Register

Address Offset: 8Ch Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	VTDSPLB[7:0]	

3.4.24 Top Display Border Configuration MSB Register

Address Offset: 8Dh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	HDSPLB_GRID[1:0]	H grip precision, 00b: 1 pixel 01b: 4 pixels 10b: 16 pixels 11b: 32 pixels
[5:4]	R/W	VDSPLB_GRID[1:0]	V grip precision 00b: 1 line 01b: 4 lines 10b: 16 lines 11b: 32 lines
[3:2]	RO	Reserved	
[1:0]	R/W	VTDSPLB[9:8]	

3.4.25 Bottom Display Border Configuration LSB Register

Address Offset: 8Eh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	VBDSPLB[7:0]	

3.4.26 Bottom Display Border Configuration MSB Register

Address Offset: 8Fh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:2]	RO	Reserved	
[1:0]	R/W	VBDSPLB[9:8]	

3.5 Gamma and Pattern Gen. Register Set

3.5.1 Image Function Control Register

Address Offset: 90h Access: Read/Write
Default Value: 08h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	GATS[1:0]	Gamma Table Select. Default=2'b00. 00b: All R/G/B Gamma tables 01b: B Gamma table 10b: G Gamma table 11b: R Gamma table
[5]	R/W	Gamma_BIST_En	Enable Gamma RAM BIST.
[4]	R/W	Tp_dith_en	
[3]	R/W	Sp_dith_2b	
[2]	R/W	ShortVS_Black	
[1]	R/W	EN_GAMMA	Enable Gamma.
[0]	R/W	EN_DITHER	Enable Dithering: 0: Disable Dithering, output full 8 bit 1: 6 bits Dithering

3.5.2 Built-in Pattern Generator Control Register

Address Offset: 91h Access: Read/Write
Default Value: 04h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	EFMCLR	Enable Frame background color Turn on this bit may disable Scaler's color and show user-defined color on LCD panel. See 0x9D, 0x9E and 0x9F for user-defined frame color.
[6]	R/W	ESLDSW	This bit may enable pattern generator shows 9 patterns sequentially. EFMCLR, ESLDSW — Output 2'b0X — Normal Color 2'b10 — Still pattern 2'b11 — Motion patterns
[5]	R/W	EVBAR	Enable Vertical Bar Patterns
[4]	R/W	PLBIT	1: indicate 8-bit patterns 0:indicate 6-bit patterns
[3:0]	R/W	PTN	Show nth pattern on LCD panel when EFMCLR is enabled When Both EFMCLR and ESLDSW are enabled, pattern generator may show 0, 1 ,2 ...up to PTNth. 5: Gray bar pattern, refer to P0_98h 6: Color bar pattern , refer to P0_98h

3.5.3 GAMMA Table Address Port Register

Address Offset: 93h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	GAMMA_ADR	Gamma coefficient table address. The Index range is 00h~FFh

3.5.4 GAMMA Table Write Data Port Register

Address Offset: 94h Access: Write Only
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	WO	GAMMA_WR_D	Gamma coefficient write data port.

3.5.5 Pattern Bar Width Register

Address Offset: 98h Access: Read/Write
Default Value: 3Ch Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Pattern_Bar_Width	This is for generated pattern vertical bar width (for patterns: Color Bar or Gray ramp)

3.5.6 CC/Ext_OSD Mixer Interface Register

Address Offset: 99h Access: Read/Write
Default Value: 02h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	En_CC_SyncOut	Enable output HS/VS/CLK for external CC/TTX decoder or Ext_OSD chip. Some CC/TTX decoder or Ext_OSD needs those controls.
[6]	R/W	CC_CLKo_Polarity	Polarity of output CC_CLKo.
[5]	R/W	CC_VSo_Polarity	Polarity of output CC_VSo.
[4]	R/W	CC_HSo_Polarity	Polarity of output CC_HSo.
[3]	R/W	CC_HV_is_Act	Output HDE/VDE instead of HS/VS
[2]	R/W	CC_Path_Input	Apply CC/Ext_OSD Mixer for: 0: Video Input path (CC/TTX) 1: Panel Output path (Ext_OSD)
[1]	R/W	CC_Clk_Inv	Invert clock to sample CC_BOX and CC_Y/R/G/B inputs
[0]	R/W	CC_CLKo_Half	Output CC_CLKO as half of VideoDecoder operation clock

3.5.7 CC/Ext_OSD Mixer Control Register

Address Offset: 9Ah Access: Read/Write
Default Value: 40h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	CC_En	Enable Mixer for CC/TTX decoder or Ext_OSD chip interface.
[6]	R/W	CC_Color_4bits	Input CC/Ext_OSD Color width: 0: 3 bits only (CC_R/G/B) 1: 4 bits (CC_Y/R/G/B)
[5]	WO	Reset_CC_LUT_Ptr	Write 1 to this bit to reset CC_LUT pointer
[4:3]	R/W	CC_αB_Mode[1:0]	CC Mixer Alpha-Blending Mode: 00b: All CC FG will be alpha blended with original Video source as CC BG; 01b: All CC FG will not be alpha blended with original Video source; 10b: All CC FG will not be alpha blended except its dot color from LUT[1]. 11b: All CC FG will not be alpha blended except its dot color from LUT[1~3]. Note: CC FG = CC_BOX && (CC_Color == 0); CC BG = CC_BOX && (CC_Color != 0);

[2:0]	R/W	CC_αB_Set[2:0]	Alpha Blending percentage (n/8). If set 000b, alpha blending is disabled (0/8 * Original Source + 8/8 * CC display); If set 001b, blending as 1/8 * Original Source + 7/8 * CC display; . . . If set N, blending as N/8 * Original Source + (8-N)/8 * CC display;

3.5.8 CC/Ext_OSD Mixer LUT Data Port Register

Address Offset: 9Bh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	WO	CC_LUT_D[7:0]	Total 32 bytes write. The CC_LUT[0..15] is YUV_4/4/4 bits format.

3.5.9 Pattern Color Gradient & Dithering Mode Register

Address Offset: 9Ch Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	CLRGRDT[3:0]	When EFMCLR are enabled, CLRGRDT may set color gradient at pattern 2, 3 ,4, 5
[3:2]	RO	Reserved	
[1:0]	R/W	Patt_Bar_LSB_Sel[1:0]	Select the gray LSB value in Gray bar ramp

3.5.10 Frame Color Red Configuration Register

Address Offset: 9Dh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	FMCLRRED	8 bits of red color depth for frame color.

3.5.11 Frame Color Green Configuration Register

Address Offset: 9Eh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	FMCLRGRN	8 bits of green color depth for frame color.

3.5.12 Frame Color Blue Configuration Register

Address Offset: 9Fh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	FMCLRBLU	8 bits of blue color depth for frame color.

3.6 OSD1 Register Set

(For detail OSD1 description, please refer to section **2.9_OSD1.**)

3.6.1 OSD1 Configuration Index Port Register

Address Offset: A0h Access: Write Only
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	WO	OSD1_CFG_INDEX	OSD1 Configuration Address Port

3.6.2 OSD1 Configuration Data Port Register

Address Offset: A1h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	OSD1_CFG_DATA	OSD1 Configuration Data Port

3.6.3 OSD1 RAM Address Port Register

Address Offset: A2h Access: Write Only
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	WO	OSD1_RAM_A	OSD1 RAM Address Port, LSB first, then MSB
[1]	RO	OSD1_RAM_Ready	OSD1 RAM is ready for next programming
[0]	RO	OSD1_Cfg_Ready	OSD1 configuration is ready for next programming

3.6.4 OSD1 RAM Data Port Register

Address Offset: A3h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	OSD1_RAM_D	OSD1 RAM Data Port

3.7 OSD2 Register Set

(For detail OSD2 description, please refer to section2.10 OSD2.)

3.7.1 OSD2 Configuration Index Port Register

Address Offset: A8h Access: Write Only
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	WO	OSD2_CFG_INDEX	OSD2 Configuration Address Port

3.7.2 OSD2 Configuration Data Port Register

Address Offset: A9h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	OSD2_CFG_DATA	OSD2 Configuration Data Port

3.7.3 OSD2 RAM Address Port Register

Address Offset: AAh Access: Write Only
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	WO	OSD2_RAM_A	OSD2 RAM Address Port, LSB [7:0] firs, then MSB[15:8]
[1]	RO	OSD2_RAM_Ready	OSD2 RAM is ready for next programming
[0]	RO	OSD2_Cfg_Ready	OSD2 configuration is ready for next programming

3.7.4 OSD2 RAM Data Port Register

Address Offset: ABh Access: Write Only
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	WO	OSD2_RAM_D	OSD2 RAM Data Port

3.8 Central Bus Configuration Port Register Set

3.8.1 Central Bus Configuration Start Address Port LSB Register

Address Offset: ADh Access: Write Only
Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	WO	CBus_Address[7:0]	Start Address Port for configuring Central Bus

3.8.2 Central Bus Configuration Start Address Port MSB Register

Address Offset: AEh Access: Write Only
Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	WO	CBus_Address[15:8]	Start Address Port for configuring Central Bus CBus_addr[15:0] = 8000h: start address of internal i51 cache

3.8.3 Central Bus Configuration Data Port MSB Register

Address Offset: AFh Access: Write Only
Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	WO	CBus_Data[7:0]	Central Bus configuration Data Port

3.9 LCD Output Control Register Set

3.9.1 Display Window Horizontal Start Register

Address Offset: B0h Access: Read/Write
Default Value: 20h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	DWHS_L[7:0]	Horizontal back porch.

3.9.2 Display Window Vertical Start Register

Address Offset: B2h Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	DWVS[7:0]	Vertical back porch

3.9.3 Display Window Horizontal Width LSB Register

Address Offset: B4h Access: Read/Write
Default Value: E0h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	DWHSZ[7:0]	Horizontal Active.

3.9.4 Display Window Horizontal Width MSB Register

Address Offset: B5h Access: Read/Write
Default Value: 01h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	DWHSZ[10:8]	Horizontal Active.

3.9.5 Display Window Vertical Width LSB Register

Address Offset: B6h Access: Read/Write
Default Value: EAh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	DWVSZ[7:0]	Vertical Active.

3.9.6 Display Window Vertical Width MSB Register

Address Offset: B7h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:2]	RO	Reserved	
[1:0]	R/W	DWVSZ[9:8]	

3.9.7 Display Panel Horizontal Total Dots per Scan Line LSB Register

Address Offset: B8h Access: Read/Write
Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	PH_TOT[7:0]	Output horizontal total dots

3.9.8 Display Panel Horizontal Total Dots per Scan Line MSB Register

Address Offset: B9h Access: Read/Write
Default Value: 03h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	PH_TOT[10:8]	

3.9.9 Display Panel Vertical Total Lines per Frame LSB Register

Address Offset: BAh Access: Read/Write
Default Value: 58h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	PV_TOT[7:0]	Output vertical total lines

3.9.10 Display Panel Vertical Total Lines per Frame MSB Register

Address Offset: BBh Access: Read/Write
Default Value: 02h Size: 8 bits

Bit	Access	Symbol	Description
[7:2]	RO	Reserved	
[1:0]	R/W	PV_TOT[9:8]	

3.9.11 Display Panel HSYNC Width Register

Address Offset: BCh Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	PH_PW[7:0]	

3.9.12 Display Panel VSYNC Width Register

Address Offset: BEh Access: Read/Write
Default Value: 02h Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	RO	Reserved	
[4:0]	R/W	PV_PW[4:0]	

3.9.13 Panel Output Signal Control 1 Register

Address Offset: C0h Access: Read/Write
Default Value: 01h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	DAC_3_Phases	Enable DAC data separated by 1/3 clock phases. 0: Same clock phase, all RGB data are aligned to skew of CPH1 rising edge 1: 3 phases, each RGB data are aligned to different CPH1~3 (considered RGB swap by line)
[6]	RO	Reserved	
[5]	R/W	En_sPanel	Enable Serial RGB (sPanel) output. 0: for Analog panel (DAC output with TCON) 1: for Serial RGB panel (sD[7:0] + DCLKO + HS/VS/HDE)
[4]	R/W	sPanel_Dot	Select output RGB components when Serial RGB (sPanel) output. 0: RGB from different cell position, consider swap. 1: RGB from same dot position, no matter swap or not.
[3]	R/W	Data_Neg	Reverse RGB output. 0: No reverse 1: RGB reverse.
[2]	R/W	PHSync_Polarity	PHSYNC Polarity. Default=0. 0: Active Low 1: Active High
[1]	R/W	PVSync_Polarity	PVSYNC Polarity. Default=0. 0: Active Low 1: Active High
[0]	R/W	PHDE_Polarity	PDE polarity. Default=1. 0: Active Low 1: Active High

3.9.14 Panel Output Signal Control 3 Register

Address Offset: C1h Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	R/W	STH_Width[2:0]	Programmable STH output width = (value + 1) clocks
[4]	R/W	STH_NegEdge	Output STH aligned to: 0: the rising edge internal panel clock 1: the falling edge internal panel clock
[3]	R/W	DCLK_INV	CLKO Polarity. Default=0. 0: Non-Invert, CLKO rising aligns to Data transition 1: Inverted, CLKO falling aligns to Data transition
[2:1]	RO	Reserved	
[0]	R/W	Half_CPHn	Half CPHn frequency when set to 1.

3.9.15 Panel VSYNC Frame Delay Control Register

Address Offset: C2h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6:5]	R/W	Hso_2_Vso_Delay	Adjust VSO Transition Edge
[4]	R/W	PSYNC_STR	For Frame lock, input VSync (if exist) will trigger output VSync 0: Allow input vsync to trigger output vsync 1: Block input vsync triggering on output vsync
[3]	R/W	ELASTPHS	Last HSync Line length option: 0: Short line, i.e., last hsync is less than 1.0 line 1: Long line , i.e.,last hsync is greater than 1.0 line
[2]	RO	Reserved	
[1]	R/W	IGNORE_VSYNC	Ignore the input VSYNC. This can be used for output free run when input VSYN is not available
[0]	WO	Reserved	

3.9.16 Panel VSYNC Frame Delay Line Count LSB Register

Address Offset: C3h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	PV_DELAY_L	Delay last stage VSync output, in the unit of output HSync leading edge.

3.9.17 Panel VSYNC Frame Delay Line Count MSB Register

Address Offset: C4h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:2]	RO	Reserved	
[1:0]	R/W	PV_DELAY_H	

3.9.18 Serial RGB HSync Delay Register

Address Offset: C5h Access: Read/Write
Default Value: 60h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	sPanel_HS_Delay[7:0]	Delay output HSync for sPanel. (count in 3x panel clock) Value must >= 02h. This register is used to shift sPanel_HS, and align correct RGB color in sequence, for some sPanel do not have HDE input.

3.9.19 Serial RGB Sync Width Register

Address Offset: C6h Access: Read/Write
Default Value: 85h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	sPanel_VsHs_Align	Enable output VSync align to HSync for sPanel. 0: VSync not aligned to HSync 1: VSync aligned to the leading clock of HSync pulse.
[6]	R/W	sPanel_Vs_1T	Set output VSync width for sPanel. 0: VSync width set by P0_BE (lines) 1: VSync 1T pulse only.
[5]	RO	Reserved	
[4:0]	R/W	sPanel_HS_Width[4:0]	Set output HSync width for sPanel. (count in 3x panel clock) Value must >= 01h

3.9.20 Output RGB Reordering Register

Address Offset: C7h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6:4]	R/W	Reserved	For test only {LnSwap_Sel, LnSwap_Inv, LnSwap_En}
[3]	R/W	BIGENDIANE	Reverse bit [7:0] of RGB: 0: Non-Inverted, Little Endian. 1: Inverted, Big Endian.
[2:0]	R/W	RGBSWAPE	RGB Channel Swapping: 000: RGB, 001: RBG, 010: GRB, 011: GRB, 1X0: BRG, 1X1: BGR;

3.9.21 Output PLL Divider 1 Register

Address Offset: C8h Access: Read/Write
Default Value: 15h Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6:0]	R/W	PLLDIV_F	PLL feedback divider.

3.9.22 Output PLL Divider 2 Register

Address Offset: C9h Access: Read/Write
Default Value: 02h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	SS_Clock_En	Enable Spread Spectrum clock output
[6:5]	R/W	SS_Clock_Deviation[1:0]	Spread Spectrum clock deviation selection
[4:0]	R/W	PLLDIV_I	PLL Input Divider.

3.9.23 Output PLL Divider 3 Register

Address Offset: CAh Access: Read/Write
Default Value: 03h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	PLLMX	PLL MUX Function Select PLLMX: Mode 2'b00: PLLCLK 2'b01: Keep High 2'b10: Bypass PLL 2'b11: Bypass PLL
[5]	R/W	PLLPD	Display PLL power down Control: 0: Display PLL power on 1: Display PLL power down
[4]	R/W	PLL_Div2	Display PLL analog divider, set 1 to half frequency output
[3:2]	R/W	PLL_OUT_SEL	PLL additional divider 0: no divider 1: divided by 2 2: divided by 4 3: divided by 8
[1:0]	R/W	PLLDIV_O	PLL Output Divider. Default=1. output_freq = 27Mhz * (F + 2) / (I+2) / (2^(O+1))

3.9.24 LLCKn Clock Register

Address Offset: CBh Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	LLCK1_Phase[3:0]	CPH1 (LLCK1) phase, 1<= value <= LLCK_DivideN[3:0]
[3:0]	R/W	LLCK_DivideN[3:0]	LLCK pre-divider. 0/1 for no divide;

3.9.25 Output LLCK Control 1 Register

Address Offset: CCh Access: Read/Write
Default Value: 32h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	LLCK3_Phase[3:0]	CPH3 (LLCK3) phase, 1<= value <= LLCK_DivideN[3:0]
[3:0]	R/W	LLCK2_Phase[3:0]	CPH2 (LLCK2) phase, 1<= value <= LLCK_DivideN[3:0]

3.9.26 Output LLCK Control 2 Register

Address Offset: CDh Access: Read/Write
Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	DAC_Clk_Delay[3:0]	DAC Clock skew to CPH1 option
[3:2]	R/W	CPH_Shift[1:0]	0/1/2/3: shift by 0/3, 1/3, 2/3, 2/3 phases
[1]	R/W	Same_CPH	Output all 3 CPH1~CPH3 with same phases
[0]	R/W	Speed_3X	Enable Cell-Base Scaling

3.9.27 Delta Type Panel Control Register

Address Offset: CEh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	Delta_L2_Drop	For Delta-type panel, drop cell or not in even Line
[6:4]	R/W	Delta_L2_Swap[2:0]	For Delta-type panel, RGB swap in even Line
[3]	R/W	Delta_L1_Drop	For Delta-type panel, drop cell or not in odd Line
[2:0]	R/W	Delta_L1_Swap[2:0]	For Delta-type panel, RGB swap in odd Line

3.9.28 Key Stone Step LSB Register

Address Offset: D0h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	KS_Step[7:0]	Keystone slope ratio

3.9.29 Key Stone Step MSB Register

Address Offset: D1h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	KS_Step [15:8]	

3.9.30 Key Stone Maximum Black Dot Register

Address Offset: D2h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	KS_Hmax [7:0]	Maximum Black dot number on each left or right sides

3.9.31 Key Stone Register

Address Offset: D3h Access: Read/Write
Default Value: 58h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	En_KeyStone	Enable Keystone function
[6]	R/W	KS_Pyramid	Keystone shape due to light source - 1: Lower; 2: Top-mounted
[5]	RO	Reserved	
[4]	R/W	En_KsV_Blank	
[3]	R/W	En_Dot1Smooth	
[2:0]	RO	Reserved	

3.9.32 Key Stone Reset Register

Address Offset: D4h Access: Write Only
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:2]	RO	Reserved	
[1]	WO	KS_Coef_Reset	Reload default keystone scaling coefficients
[0]	WO	KS_Coef_Ptr_Reset	Reset pointer of keystone coefficient table

3.9.33 Key Stone Coef Data Port Register

Address Offset: D5h Access: Write Only
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	WO	KS_Coef_Data_Port	

3.9.34 Display Window Horizontal Start Register

Address Offset: D8h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HMDISP_STR[7:0]	

3.9.35 Display Window Vertical Start Register

Address Offset: DAh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	VMDISP_STR	

3.9.36 Display Window Horizontal Size LSB Register

Address Offset: DCh Access: Read/Write
Default Value: E0h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HMDISP_SIZE[7:0]	

3.9.37 Display Window Horizontal Size MSB Register

Address Offset: DDh Access: Read/Write
Default Value: 01h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	HMDISP_SIZE[10:8]	

3.9.38 Display Window Vertical Size LSB Register

Address Offset: DEh Access: Read/Write
Default Value: EAh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	VMDISP_SIZE[7:0]	

3.9.39 Display Window Vertical Size MSB Register

Address Offset: DFh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:2]	RO	Reserved	
[1:0]	R/W	VMDISP_SIZE[9:8]	

3.10 Global Control Register Set

3.10.1 Power Management Control Register

Address Offset: E0h Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	PD_TotalPad_	Set to 0 for Power Down all I/O pads, except I^2C I/F.
[6]	R/W	PD_ADCD_	Set to 0 for Power Down ADC digital portion.
[5]	R/W	PD_VIP_	Power down ITU-R656, L601 interface, active low
[4]	R/W	PD_VD_	Set to 0 for Power Down Comb Video Decoder block.
[3]	R/W	LLCK1_EN	LLCK1 enable
[2]	R/W	LLCK2_EN	LLCK2 enable
[1]	R/W	LLCK3_EN	LLCK3 enable
[0]	R/W	PD_TC_	Set to 0 for Power down TC interface.

3.10.2 Output Pin Configuration

Address Offset: E1h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	RowSTV_Sel	RowSTV_Sel / Mode 2'b00 / Output both 2'b01 / Output both 2'b10 / Output STV1 2'b11 / Output STV2
[5:4]	R/W	ColSTH_Sel	ColSTH_Sel / Mode 2'b00 / Output both 2'b01 / Output both 2'b10 / Output STH1 2'b11 / Output STH2
[3]	R/W	UD_Sel	Set UD output value
[2]	R/W	RL_Sel	Set RL output value
[1:0]	RO	Reserved	

3.10.3 Shadow Control Configuration

Address Offset: E2h Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	RO	Reserved	
[4]	R/W	Shadow_Enable	1: Enable registers shadow control
[3:1]	RO	Reserved	
[0]	WO	Shadow_Sync	Write 1 to sync all shadowed registers

3.10.4 DAC Power Management

Address Offset: E3h Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	PDn_Bias	1: power down Bias circuit 0: power on Bias circuit
[6]	R/W	PDn_VCOM	1: power down Analog VCOM Amp circuit 0: power on Analog VCOM Amp circuit
[5]	RO	Reserved	
[4]	R/W	PDn_DC2DC_	1: power on DC to DC circuit 0: power down DC to DC circuit
[3]	R/W	SL	1: power down 3 channels 0: power on 3 channels
[2]	R/W	SLR	1: power down R channel 0: power on R channel
[1]	R/W	SLG	1: power down G channel 0: power on G channel
[0]	R/W	SLB	1: power down B channel 0: power on B channel

3.10.5 Analog Output Current 1 Register

Address Offset: E4h Access: Read/Write
Default Value: 0Fh Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	R/W	VCOM_DC[2:0]	LSB of VCOM DC setting
[4:0]	R/W	DAC_Amp[4:0]	DAC Amp setting

3.10.6 Analog Output Current 2 Register

Address Offset: E5h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	VCOM_VoltagePeak	VCOM voltage peak setting
[6:5]	R/W	VCOM_DC[4:3]	MSB of VCOM DC setting
[4:0]	R/W	VCOM_Amp[4:0]	VCOM Amp setting

3.10.7 Power Down Register

Address Offset: E6h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	PD_CombLB	1: power down Video Decoder Comb Line Buffers 0: power on Video Decoder Comb Line Buffers
[6]	R/W	PD_XCLK2MC	1: Tri-state XCLK2MC output 0: Allow XCLK2MC output
[5]	R/W	PDn_BackLight_	1: power on BackLight circuit 0: power down BackLight circuit
[4]	RO	ShutDn_BackLight	Shutdown result
[3]	RO	ShutDn_DC2DC	Shutdown result
[2:0]	RO	Reserved	

3.10.8 CCFL/LED Control Register

Address Offset: E7h Access: Read/Write
Default Value: 60h Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6]	R/W	Mask_SAR1_Toggle	Set to 1 for masking interrupt trigger source of SAR1_Toggle
[5:4]	R/W	Mask_SAR0_Toggle	Set to 1 for masking interrupt trigger source of SAR0_Toggle
[4:3]	RO	Reserved	
[2]	RO/W1C	SAR1_Toggle	Read to get SAR1_Toggle interrupt status, Write 1 to clear it
[1]	RO/W1C	SAR0_Toggle	Read to get SAR0_Toggle interrupt status, Write 1 to clear it
[0]	RO	Reserved	

3.10.9 PWM_1 General Control Register

Address Offset: E8h Access: Read/Write
Default Value: 07h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	PWM1_Low[4:3]	
[5]	R/W	PWM1_Alt_Mode	1: Alternative PWM1 mode; 0: Legacy {PWM1_High/256} mode
[4]	R/W	PWM1_En	Enable PWM_1
[3]	RO	Reserved	
[2:0]	R/W	PWM1_Freq_Sel	This register set the PWM1 counter base clock = XCLK / 2^N, N=0, 1, 2, 3, 5, 7, 9, 11. That is, the PWM1 freq = PWM1 base clock freq / 256.

3.10.10 PWM_1 Active High Time Counter Register

Address Offset: E9h Access: Read/Write
Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	R/W	PWM1_High[7:5] / PWM1_Low[2:0]	InPWM1 legacy mode, this register set PWM1 high time (PWM1_High[7:0]/256) counted by PWM1 base clock. In PWM1 Alternative mode, the PWM1 output: PWM1_High[4:0] / (PWM1_Low[4:0] + PWM1_High[4:0]), based clock is divide from XCLK , see P0_E8<2:0>
[4:0]	R/W	PWM1_High[4:0]	This register set PWM1 high time counted by PWM1 base clock. The based clock is divide from XCLK , see P0_E8<2:0>

3.10.11 PWM_4 General Control Register

Address Offset: EAh Access: Read/Write
Default Value: 07h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	PWM4_Low[4:3]	
[5]	R/W	PWM4_Alt_Mode	1: Alternative PWM4 mode; 0: Legacy {PWM4_High/256} mode
[4]	R/W	PWM4_En	Enable PWM_4
[3]	RO	Reserved	
[2:0]	R/W	PWM4_Freq_Sel	This register set the PWM4 counter base clock = XCLK / 2^N, N=0, 1, 2, 3, 5, 7, 9, 11. That is, the PWM4 freq = PWM4 base clock freq / 256.

3.10.12 PWM_4 Active High Time Counter Register

Address Offset: EBh Access: Read/Write
Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	R/W	PWM4_High[7:5] / PWM4_Low[2:0]	InPWM4 legacy mode, this register set PWM4 high time (PWM4_High[7:0]/256) counted by PWM4 base clock. In PWM4 Alternative mode, the PWM4 output: PWM4_High[4:0] / (PWM4_Low[4:0] + PWM4_High[4:0]), based clock is divide from XCLK , see P0_E8<2:0>
[4:0]	R/W	PWM4_High[4:0]	This register set PWM4 high time counted by PWM4 base clock. The based clock is divide from XCLK , see P0_E8<2:0>

3.10.13 DAC Offset Control Register

Address Offset: EDh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	RO	Reserved	
[4:0]	R/W	DAC_Offset[4:0]	DAC Offset setting

3.10.14 GPOD Pin Control Register

Address Offset: EEh Access: Read/Write
Default Value: 66h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	GPOD_oSel3	GPOD3 acts as: 00b~01b: RL/GPOD3
[5:4]	R/W	GPOD_oSel2	GPOD2 acts as: 00b~11b: RL/PWM4/GPOD2/STN_CS#
[3:2]	R/W	GPOD_oSel1	GPOD1 acts as: 00b~1xb: UD/GPOD1/ STN_RST#
[1:0]	R/W	GPOD_oSel0	GPOD0 acts as: 00b~11b: UD/PWM4/GPOD0/STN_RST#

3.10.15 Shutdown Control Register

Address Offset: EFh Access: Read/Write
Default Value: C0h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	XCLK2MC_Div[1:0]	Extra divider for XCLK oscillator to XCLK2MC output: 00b: stop; 01b:1/1; 10b:1/2; 11b:1/4;
[5:1]	RO	Reserved	
[0]	R/W	DRI34_alone	DRI3, DRI4 alternative pins

3.10.16 Serial Bus Slave Device Address Register

Address Offset: F0h Access: Read/Write
Default Value: 40/50h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	R/W	SDADDR	default = 40 if CPUINT is low while reset default = 50 if CPUINT is high while reset
[2:0]	RO	Reserved	

3.10.17 Serial Bus Control Register

Address Offset: F1h Access: Read/Write
Default Value: C4h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	SCL_Out	SCL output value, when i8051 enabled and acts as an I2C master
[6]	RO	SCL_In	SCL input status
[5]	R/W	SDA_Out	SDA output value, when i8051 enabled and acts as an I2C master
[4]	RO	SDA_In	SDA input status
[3]	R/W	Reserved	
[2]	R/W	I2CATINCADR	Set to 1 for enabling 2-wire serial bus automatic address increment in multiple R/W Access mode. Default=1'b1.
[1:0]	RO	Reserved	

3.10.18 Foundry ID Register

Address Offset: F3h Access: Read Only
Default Value: 01h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	FID	Foundry ID

3.10.19 Chip ID Register

Address Offset: F4h Access: Read Only
Default Value: 08h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	CID	Chip ID

3.10.20 Revision ID Register

Address Offset: F5h Access: Read Only
Default Value: B1h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	RID	Revision ID, ECO version

3.10.21 Date Code ID Register

Address Offset: F6h Access: Read Only
Default Value: 8Ah Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	DID_H	Date code ID, Year/Month

3.10.22 Wakeup Control Register 1

Address Offset: FCh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	PwrM_En	1: enable power management function
[6]	RO/W1C	PwrM_Wakeup	Read to get the wake up event trigger; Write 1 to clear
[5]	R/W	SAR1_PwrM_En	
[4]	RO	Reserved	
[3:0]	R/W	PwrM_SAR_Threshold	SAR Threshold for Power management event trigger

3.10.23 Wakeup Control Register 2

Address Offset: FDh Access: Read/Write
Default Value: ACh Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	PwrM_GPIO_Value	Set Wakeup control value on GPIOs
[3:0]	R/W	PwrM_GPIO_Sel	Select which GPIO[n] for Power management

3.10.24 Pin Function Select Register

Address Offset: FEh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	GPOA54_as_UDRL	GPOA[5:4] act as: 0: GPOA[5:4] (controlled by P1_51<5:4>); 1: UD and RL (controlled by P0_E1<3:2>)
[6]	R/W	GPOA321_as_TCON	GPOA[3:1] act as: 0: GPOA[3:1] (controlled by P1_51<3:1>); 1: TCON: STB/CKVB (inverted of some TCON signals)
[5]	R/W	GPIC_from_LVY	GPIC[7:0] input from: 0: GPIC[7:0] mux-ed pins; 1: LVY[7:0] pins
[4]	R/W	Alt_VIP_Pins	VIP input pins: 0: Origianl pins (when DAC/sPanel output); 1: Alternative pins (when TTL output)
[3:2]	R/W	TTL_Output_Mode[1:0]	TTL output mode: 00: Disabled (use DAC or sPanel interface output); 01: RGB666 output 10: RGB777 output 11: RGB888 output
[1:0]	R/W	Reserved	

3.10.25 Page Select Register

Address Offset: FFh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:2]	RO	Reserved	
[1:0]	R/W	PAGE[1:0]	

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3.11 TCON Register Set

3.11.1 Timing Controller (TCON) Control Register

Address Offset: 20h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	GScanInt	Enable interlaced scanning Mode: Type 0: Processive 1: Interlacing
[6]	R/W	DDR_GDRV	Enable DDR gate driver Mode: Type 0: 1 line/GCLK 1: 2 lines/GLK
[5]	R/W	GTOE	Enable gate driver output Mode: Type 0: Shutdown output 1: Enable
[4]	R/W	DbScan_Edge	Clock edge of STV When DbScan_STV_1p is enabled, DbScan_Edge can control STV alignment with the falling edge o rising edge of GCLK Mode: Type 0: Falling edge of GCLK 1: Rising edge of GCLK
[3]	R/W	DbScan_STV_1p5	STV 1.5 lines wide Mode: Type 0: 1 line wide 1: 1.5 lines wide
[2]	R/W	DbScan_En	Gate driver Scanning control Mode: Type 0: 1 GCLK/line 1: 2 GCLKs/line
[1]	R/W	Q1HPL	Q1H polarity Mode: Type 0: Negative 1: Positive
[0]	R/W	PNINV	Enable line-inverted function.

3.11.2 Timing Protocol & Polarity Control Register

Address Offset: 21h Access: Read/Write
Default Value: FFh Size: 8 bits

Bit	Access	Symbol	Description
[7]	RW	DRVRSTPL	This bit may control Source Drive Reset polarity When P0_E1h<7:6> is not 11b, pin STV2 becomes the rese of source driver.
[6]	R/W	GTOEPL	This bit may control GOE polarity Mode Type 0 Low-active 1 Highactive
[5]	R/W	STVPL	Row Driver start pulse polarity Mode Type 0 Negative 1 Positive
[4]	R/W	CLKVPL	Data Inversion Polarity Mode Type 0 Negative 1 Positive
[3]	R/W	FLD1PL	Video Field Polarity Mode Type 0 Inverted field flag 1 Non-inverted field flag
[2]	R/W	POLPL	Column Driver POL inversion polarity Mode Type 0 Negative 1 Positive
[1]	R/W	LPPL	Column Driver Latch Pulse polarity Mode Type 0 Negative 1 Positive
[0]	R/W	STHPL	Column Driver Start Pulse polarity Mode Type 0 Negative 1 Positive

3.11.3 Column Driver Latch Pulse Placement LSB Register

Address Offset: 22h Access: Read/Write
Default Value: 03h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	CDLPPLM[7:0]	This register allows LP to place between 2 DE pulses counted by LLCK dot clock The reference point is the rising edge of DE.

3.11.4 Column Driver Latch Pulse Placement MSB Register

Address Offset: 23h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	CDLPPLM[10:8]	This register allows LP to place between 2 DE pulses counted by LLCK dot clock The reference point is the rising edge of DE.

3.11.5 Column Driver Latch Pulse Duration Control Register

Address Offset: 24h Access: Read/Write
Default Value: 21h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	CDLPDU[7:0]	This register allows LP duration programmable. counted by LLCK dot clock.

3.11.6 POL Placement LSB Register

Address Offset: 25h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	POLPLM[7:0]	The reference point is the leading edge of DE.

3.11.7 POL Placement MSB Register

Address Offset: 26h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	POLPLM[10:8]	The reference point is the leading edge of DE.

3.11.8 CLKV Placement LSB Register

Address Offset: 27h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	CLKVPLM[7:0]	The reference point is the leading edge of DE

3.11.9 CLKV Placement MSB Register

Address Offset: 28h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	CLKVPLM[10:8]	The reference point is the leading edge of DE

3.11.10 CLKV Duration LSB Register

Address Offset: 29h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	CLKVDU[7:0]	The reference point is leading edge of DE

3.11.11 CLKV Duration MSB Register

Address Offset: 2Ah Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	CLKVDU[10:8]	The reference point is the leading edge of DE

3.11.12 STH Position Placement Register

Address Offset: 2Bh Access: Read/Write
Default Value: 01h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	STHPLM[2:0]	STH timing related to HDE. -2 to 5 CLKHs

3.11.13 Gate Driver Pre-Driving Register

Address Offset: 2Dh Access: Read/Write
Default Value: 03h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	GTVLTC	STV2 Duration

3.11.14 Double Scan CLKV Placement LSB Register

Address Offset: 2Eh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	DbS_CLKVPLM[7:0]	

3.11.15 Double Scan CLKV Placement MSB Register

Address Offset: 2Fh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	DbS_CLKVPLM[10:8]	

3.11.16 Row Driver Configuration Register

Address Offset: 30h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:1]	RO	Reserved	
[0]	R/W	ESTVOFFSET	Enable STV Offset

3.11.17 Gate Driver OE Pulse Position Placement LSB Register

Address Offset: 31h Access: Read/Write
Default Value: 0Fh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	GOEPL[7:0]	

3.11.18 Gate Driver OE Pulse Position Placement MSB Register

Address Offset: 32h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	GOEPL[10:8]	

3.11.19 Gate Driver OE Pulse Duration LSB Register

Address Offset: 33h Access: Read/Write
Default Value: 0Fh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	GOEDU[7:0]	

3.11.20 Gate Driver OE Pulse Duration MSB Register

Address Offset: 34h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	GOEDU[10:8]	

3.11.21 STV Offset Register

Address Offset: 35h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	STVOFF[7:0]	

3.12 Infra-Red Register Set

3.12.1 IR Sampling Tick LSB Register

Address Offset: 40h Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	IR_Tick[7:0]	Sampling Tick LSB byte (Unit: XCLK is 27MHz): NEC mode: 560μs (3B10h); Philips RC5 mode: 900μs (5EECh)

3.12.2 IR Sampling Tick MSB Register

Address Offset: 41h Access: Read/Write
Default Value: 3Bh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	IR_Tick[15:8]	Sampling Tick MSB byte.

3.12.3 IR Stream 1~4 Register (when IR_Counter_Mode=0)

Address Offset: 42h~45h Access: Read Only
Default Value: –h Size: 32 bits

Bit	Access	Symbol	Description
[7:0] x4	RO	IR_Stream[0..31]	Decoded IR stream (packet) stored in P1_42h~45h The first received bit is IR_Stream[0], then the next IR_Stream[1], …. and the last available bit is IR_Stream[31] if packet that long. IR_Stream[7:0] in P1_42, IR_Stream[15:8] in P1_43, IR_Stream[23:16] in P1_44, IR_Stream[31:24] in P1_45;

3.12.4 IR Duration 1~3 Register (when IR_Counter_Mode=1)

Address Offset: 42h~44h Access: Read Only
Default Value: –h Size: 24 bits

Bit	Access	Symbol	Description
[7:0] x3	RO	IR_Duration[0..21] (P1_44<7:6> are 00b)	The duration (count in XCLK) of input IR. When IR protocol is not supported, F/W can use this counter result and IR interrupt to decode.

3.12.5 IR Stream 1 Register

Address Offset: 47h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	IR_En	Enable IR Decoder.
[6]	R/W	IR_Counter_Mode	Set to 0 for supported IR protocols; Set to 1 for monitoring IR transition duration (count in XCLK)
[5:4]	R/W	IR_Mode[1:0]	IR Decoder Mode: 00: NEC mode; 01: Philips RC5 mode; 1X: Sony mode
[3]	R/W	IR_Invert	Invert IR1 input to IR Decoder.
[2]	RO	IR_Value	Current IR value (high or low)
[1]	RO	IR_Overflow	IR duration counter overflow if get 1, then the
[0]	RO	IR_Repeat	Getting 1 indicates the current IR packet is Repeat.

3.13 GPIO Register Set

3.13.1 GPOA Output Control Register

Address Offset: 50h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	oe_GPOA[7:0]	Enable GPOA[n] pin begin output drive when set to 1.

3.13.2 GPOA Output Value Register

Address Offset: 51h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	o_GPOA[7:0]	Assign GPOA[7:0] Output Value

3.13.3 GPOA Status Register

Address Offset: 52h Access: Read Only
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	i_GPOA[7:0]	Report GPOA[7:0] Pins current status

3.13.4 GPOB Output Control Register

Address Offset: 54h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	oe_GPOB[7:0]	Enable GPOB[n] pin begin output drive when set to 1.

3.13.5 GPOB Output Value Register

Address Offset: 55h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	o_GPOB[7:0]	Assign GPOB[7:0] Output Value

3.13.6 GPOB Status Register

Address Offset: 56h Access: Read Only
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	i_GPOB[7:0]	Report GPOB[7:0] Pins current status

3.13.7 GPIC Interrupt Trigger 1 Register

Address Offset: 57h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	En_Rise_GPIC[7:0]	Enable GPIC[7:0] rising edge to trigger interrupt.

3.13.8 GPIC Interrupt Trigger 2 Register

Address Offset: 58h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	En_Fall_GPIC[7:0]	Enable GPIC[7:0] falling edge to trigger interrupt.

3.13.9 GPIC Interrupt Register

Address Offset: 59h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO/W1C	Int_GPIC[7:0] / Clr_Int_GPIC[7:0]	Read to get interrupt status triggered by GPIC[7:0] transition. Write 1 to clear.

3.13.10 GPIC Status Register

Address Offset: 5Ah Access: Read Only
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	i_GPIC[7:0]	Report GPIC[7:0] Pins current status

3.13.11 GPIC De-Bounce Register

Address Offset: 5Bh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	En_DeBnc_GPIC[7:0]	Enable GPIC[7:0] input de-bounce filters

3.13.12 GPIO Output Register

Address Offset: 5Ch Access: Read/Write
Default Value: F0h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	o_GPO[7:0]	GPIO[3:0] Output Value
[3:0]	R/W	oe_GPIO[3:0]	Set to 1 for GPIO[3:0] output enable, else acts as input.

3.13.13 GPIO Status and Interrupt Register

Address Offset: 5Dh Access: Read/Write
Default Value: F0h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	RO	i_GPIO[3:0]	Report GPIO[3:0] Pins current status
[3:0]	RO/W1C	Int_GPIO[3:0] / Clr_Int_GPIO[3:0]	Read to get interrupt status triggered by GPIC[7:0] transition. Write 1 to clear.

3.13.14 GPIO Interrupt Trigger Register

Address Offset: 5Eh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	En_Fall_GPIO[3:0]	Enable GPIO[3:0] falling edge to trigger interrupt.
[3:0]	R/W	En_Rise_GPIO[3:0]	Enable GPIO[3:0] rising edge to trigger interrupt.

3.13.15 GPIO Control Register

Address Offset: 5Fh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	En_DeBounce[1:0]	Enable GPIO[3:2] and GPIO[1:0] inputs de-bounce function.
[5:4]	R/W	DeBounce_Sel[1:0]	GPIO[3:0] input de-bounce duration base selection. 00: 1ms 01: 2ms 10: 4ms 11: 8ms
[3:0]	R/W	OD_GPIO[3:0]	Set to 1 for GPIO[n] as Open Drain output, else as Drive output.

3.14 Digital PWM Register Set

3.14.1 PWM23 Limit Register - 1

Address Offset: 60h Access: Read/Write
Default Value: 02h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	CCFL_Half_Bridge	1:Half bridge output; 0: Full bridge output
[6:4]	RO	Reserved	
[3:0]	R/W	PWM2_DeadTimer_sel	When PWM2_DeadTimer[2:1]==00b, shutdown immediately

3.14.2 PWM23 Limit Register - 2

Address Offset: 61h Access: Read/Write
Default Value: 02h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	PWM2_avg_en	Enable PWM2 averaging successive inputs
[6]	R/W	PWM2_avg_mode	PWM2 average mode, 0b: average 2, 1b: average 4
[5]	R/W	PWM3_avg_en	Enable PWM3 averaging successive inputs
[4]	R/W	PWM3_avg_mode	PWM3 average mode, 0b: average 2, 1b: average 4
[3:0]	R/W	PWM3_DeadTimer_sel	When PWM3_DeadTimer[2:1]==00b, shutdown immediately

3.14.3 PWM2 Control Register

Address Offset: 62h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	PWM2_En	Enable PWM2
[6]	R/W	PWM2_Track	0b: Assign mode, 1b: Track mode;
[5:4]	R/W	PWM2_Freq_Sel	00b~11b: divided 1/2/4/8
[3:2]	R/W	PWM2_Step_Sel	00b~11b: slower -> faster tracking
[1]	R/W	PWM2_FTClk_en	Enable Fractional Fine Tune
[0]	R/W	PWM2_4bits_mode	Enable 4 bits mode, 0b: 1 bit, 1b: 4 bit

3.14.4 PWM2 Duty Register

Address Offset: 63h Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	PWM2_High[7:0]	00~FFh means 1/PWM2_Period ~ 256/PWM2_Period; PWM2_En=0 means 0/PWM2_Period;

3.14.5 PWM2 Period Register

Address Offset: 64h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description

[7:0]	R/W	PWM2_Period[7:0]	

3.14.6 PWM3 Control Register

Address Offset: 65h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	PWM3_En	Enable PWM3
[6]	R/W	PWM3_Track	0b: Assign mode, 1b: Track mode;
[5:4]	R/W	PWM3_Freq_Sel	00b~11b: divided 1/2/4/8
[3:2]	R/W	PWM3_Step_Sel	00b~11b: slower -> faster tracking
[1]	R/W	PWM3_FTClk_en	Enable Fractional Fine Tune
[0]	R/W	PWM3_4bits_mode	Enable 4 bits mode, 0b: 1 bit, 1b: 4 bit

3.14.7 PWM3 Duty Register

Address Offset: 66h Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	PWM3_High[7:0]	00~FFh means 1/PWM3_Period ~ 256/PWM3_Period; PWM3_En=0 means 0/PWM3_Period;

3.14.8 PWM3 Period Register

Address Offset: 67h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	PWM32_Period[7:0]	

3.14.9 CCFL Control Register

Address Offset: 68h Access: Read/Write
Default Value: 06h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	PWM3_for_CCFL	Backlight control type: 1b: CCFL; 0b: LED
[6]	R/W	CCFL_ShD_to_Z	Shutdown control option
[5]	R/W	PWM23_Rd_Track	P1_63h/66h read back value as: 1b:tracked value; 0b:programmed PWM2/3_High[7:0]
[4]	R/W	PWM23_ShutDn_En	Enable over current protection
[3:2]	R/W	PWM3_TurnAround	CCFL full bridge skew
[1:0]	R/W	PWM23_Tip_Ahead	

3.14.10 PWM2 Range Register - 1

Address Offset: 69h Access: Read/Write
Default Value: 08h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	PWM2_High_Min	Lower limit of PWM2 duty

3.14.11 PWM2 Range Register - 2

Address Offset: 6Ah Access: Read/Write
Default Value: 60h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	PWM2_High_Max	Upper limit of PWM2 duty

3.14.12 PWM3 Range Register - 1

Address Offset: 6Bh Access: Read/Write
Default Value: 08h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	PWM3_High_Min	Lower limit of PWM3 duty

3.14.13 PWM3 Range Register - 2

Address Offset: 6Ch Access: Read/Write
Default Value: 60h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	PWM3_High_Max	Upper limit of PWM3 duty

3.14.14 PWM2 Trace Register

Address Offset: 6Dh Access: Read/Write
Default Value: 3Ch Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	PWM2_Threshold	Trace threshold
[3:0]	R/W	PWM2_Target	Target of trace level

3.14.15 PWM3 Trace Register

Address Offset: 6Eh Access: Read/Write
Default Value: 3Ch Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	PWM3_Threshold	Trace threshold
[3:0]	R/W	PWM3_Target	Target of trace level

3.14.16 PWM23 Read Value Register

Address Offset: 6Fh Access: Read Only
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	RO	VFB[3:0]	
[3:0]	RO	VFBL[3:0]	

3.15 SAR Register Set

3.15.1 SAR0 Control Register

Address Offset: 70h Access: Read/Write
Default Value: 6Eh Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	R/W	SAR0_Freq_Sel	000b: clock disable, 001b~111b: divided by 2^2~2^8
[4:2]	R/W	SAR0_StableMask	Stable Mask
[1]	R/W	PDn_SAR0	1b: Power down SAR0
[0]	R/W	SAR0_DeBounce	1b: Enable de-bounce function

3.15.2 SAR0 Real-Time Value Register

Address Offset: 71h Access: Read Only
Default Value: FFh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	SAR0_RlTm_Value	SAR0 real-time sampled value

3.15.3 SAR0 Threshold Register

Address Offset: 72h Access: Read/Write
Default Value: 20h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	SAR0_Threshold	Threshold for stable checking

3.15.4 SAR1 Control Register

Address Offset: 73h Access: Read/Write
Default Value: 6Eh Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	R/W	SAR1_Freq_Sel	000b: clock disable, 001b~111b: divided by 2^2~2^8
[4:2]	R/W	SAR1_StableMask	Stable Mask
[1]	R/W	PDn_SAR1	1b: Power down SAR1
[0]	R/W	SAR1_DeBounce	1b: Enable de-bounce function

3.15.5 SAR1 Real-Time Value Register

Address Offset: 74h Access: Read Only
Default Value: FFh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	SAR1_RlTm_Value	SAR1 real-time sampled value

3.15.6 SAR1 Threshold Register

Address Offset: 75h Access: Read/Write
Default Value: 20h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	SAR1_Threshold	Threshold for stable checking

3.15.7 SAR0 Stable Value Register

Address Offset: 76h Access: Read Only
Default Value: FFh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	SAR0_Ltch_Value	SAR0 stable sampled value

3.15.8 SAR1 Stable Value Register

Address Offset: 77h Access: Read Only
Default Value: FFh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	SAR1_Ltch_Value	SAR1 stable sampled value

3.15.9 SAR0/1 Source Selection Register

Address Offset: 78h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	R/W	SAR0_Src_Sel	00b/01/1x: SRA00/SAR01/SAR02
[5:4]	R/W	SAR1_Src_Sel	00b/01/1x: SRA10/SAR11/SAR12
[3:0]	RO	Reserved	

3.16 Touch Panel Register Set

3.16.1 TP Control Register - 1

Address Offset: 7Ch Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	TP_Measure[2:0]	Measure Mode: 000b: Disable 4-wire 100b: Pen Down 001b: Measure X 010b: Measure Y

3.16.2 TP Control Register - 1

Address Offset: 7Dh Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	RO	Reserved	
[4]	R/W	TP_PSEN	1: Enable Touch Panel Power Saving **Note: while using SAR keys, should set it to "0"**
[3]	RO	TP_PDD_Result	Status of Touch Panel Pen-Down-Detected
[2]	RO	TP_Move	Status of Touch Panel coordinate moved
[1]	R/W	TP_PDD_Trig_En	
[0]	R/W	TP_Move_Trig_En	

3.16.3 PWM Tip Selection

Address Offset: 7Fh Access: Read/Write
Default Value: 44h Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6:4]	R/W	PWM2_Tip_Sel	000b~111b: divided by 2^4~2^11
[3]	RO	Reserved	
[2:0]	R/W	PWM3_Tip_Sel	000b~111b: divided by 2^4~2^11

3.17 GPO Register Set

3.17.1 GPOD Register

Address Offset: 8Ch Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	o_GPOD[3:0]	Data output
[3:0]	R/W	oe_GPOD[3:0]	Output enable

3.18 Color Space Convert Register Set

3.18.1 YUV To RGB Convert Register - 1

Address Offset: B0h Access: Read/Write
Default Value: 95h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	YCoef_R[7:0]	Y To R Coefficient

3.18.2 YUV To RGB Convert Register - 2

Address Offset: B1h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5]	R/W	CbCoef_R_Sign	Cb To R Coefficient, Sign bit
[4:0]	R/W	CbCoef_R[4:0]	Cb To R Coefficient

3.18.3 YUV To RGB Convert Register - 3

Address Offset: B2h Access: Read/Write
Default Value: CCh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	CrCoef_R[7:0]	Cr To R Coefficient

3.18.4 YUV To RGB Convert Register - 4

Address Offset: B3h Access: Read/Write
Default Value: 95h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	YCoef_G[7:0]	Y To G Coefficient

3.18.5 YUV To RGB Convert Register - 5

Address Offset: B4h Access: Read/Write
Default Value: 32h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	CbCoef_G[7:0]	Cb To G Coefficient

3.18.6 YUV To RGB Convert Register - 6

Address Offset: B5h Access: Read/Write
Default Value: 68h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	CrCoef_G[7:0]	Cr To G Coefficient

3.18.7 YUV To RGB Convert Register - 7

Address Offset: B6h Access: Read/Write
Default Value: 95h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	YCoef_B[7:0]	Y To B Coefficient

3.18.8 YUV To RGB Convert Register - 8

Address Offset: B7h Access: Read/Write
Default Value: 81h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	CbCoef_B[4:0]	Cb To B Coefficient

3.18.9 YUV To RGB Convert Register - 9

Address Offset: B8h Access: Read/Write
Default Value: C0h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	En_YCbCr2RGB	Set to 1 for enabling YUV (YCbCr) Color space converting to RGB
[6]	R/W	Y_Sub16	Set to 1 for Luma offset 16; 0 for offset 0;
[5]	R/W	CrCoef_B_Sign	Cr To B Coefficient, Sign bit
[4:0]	R/W	CrCoef_B[4:0]	Cr To B Coefficient

3.19 Color Probing Register Set

3.19.1 Color Range and Probing Control Register

Address Offset: C0h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	Show_Sum	Color Range Mode: 0: Show Minimum/Maximum values 1: Show summation of a group dots.
[6]	R/W	Whole_ActRange_	Performing Color in the range of: 0: Whole input active window 1: a group dots window, defined by P1_CA ~ P1_CE
[5]	R/W	En_Hblank_rng	Set to 1 when probing color not only in active region, but also in horizontal blank area
[4]	R/W	HSI_Leading_rng	Horizontal count from input HSync leading or trailing edge
[3]	W1O/RO	FullRange_Probe/Busy	Write-1 to latch current probing results, and latched values will present in P1_C4~C9 after this bit reqd back as 0.
[2]	R/W	FullRange_En	This allow accumulated color probing result, if need clear results, must reset En_Color_Range
[1]	RO	Done_Color_Range	Color Range Probing is finished when read get 1.
[0]	R/W	En_Color_Range	Set to 1 for enabling Color Range Probing; All color range result must be read first before disabling this bit.

3.19.2 Probed R-Channel Color Value Register

Address Offset: C1h Access: Read Only
Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	rbk_R[7:0]	

3.19.3 Probed G-Channel Color Value Register

Address Offset: C2h Access: Read Only
Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	rbk_G[7:0]	

3.19.4 Probed B-Channel Color Value Register

Address Offset: C3h Access: Read Only
Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	rbk_B[7:0]	

3.19.5 Probed R-Channel Color Range LSB Register

Address Offset: C4h Access: Read Only
Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	R_Low[7:0] / R_Sum[7:0]	When Show_Sum=0, get minimum R color value, When Show_Sum=1, get R color summation LSB.

3.19.6 Probed R-Channel Color Range MSB Register

Address Offset: C5h Access: Read Only
Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	R_High[7:0] / R_Sum[15:8]	When Show_Sum=0, get maximum R color value, When Show_Sum=1, get R color summation MSB.

3.19.7 Probed G-Channel Color Range LSB Register

Address Offset: C6h Access: Read Only
Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	G_Low[7:0] / G_Sum[7:0]	When Show_Sum=0, get minimum G color value, When Show_Sum=1, get G color summation LSB.

3.19.8 Probed G-Channel Color Range MSB Register

Address Offset: C7h Access: Read Only
Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	G_High[7:0] / G_Sum[15:8]	When Show_Sum=0, get maximum G color value, When Show_Sum=1, get G color summation MSB.

3.19.9 Probed B-Channel Color Range LSB Register

Address Offset: C8h Access: Read Only
Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	B_Low[7:0] / B_Sum[7:0]	When Show_Sum=0, get minimum B color value, When Show_Sum=1, get B color summation LSB.

3.19.10 Probed B-Channel Color Range MSB Register

Address Offset: C9h Access: Read Only
Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	B_High[7:0] / B_Sum[15:8]	When Show_Sum=0, get maximum B color value, When Show_Sum=1, get B color summation MSB.

3.19.11 Probed Dot Coordinate-X LSB Register

Address Offset: CAh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Rbk_X[7:0]	

3.19.12 Probed Dot Coordinate-X MSB Register

Address Offset: CBh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	Rbk_X[10:8]	

3.19.13 Probed Dot Coordinate-Y LSB Register

Address Offset: CCh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Rbk_Y[7:0]	

3.19.14 Probed Dot Coordinate-Y MSB Register

Address Offset: CDh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:2]	RO	Reserved	
[1:0]	R/W	Rbk_Y[9:8]	

3.19.15 Probed Dot Size Register

Address Offset: CEh Access: Read/Write
Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Pixel_RangeSize[7:0]	Defines the dots group size

3.20 ITU - 656 Decoder Register Set

3.20.1 ITU-656 Decoder HS Delay Register

Address Offset: D0h Access: Read/Write
Default Value: 30h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HS_DELAY656[7:0]	Unit: Cycles of Half VCLK

3.20.2 ITU-656 Decoder HS Pulse Width Register

Address Offset: D2h Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:3]	R/W	HS_WIDTH656[5:3]	Unit: Cycles of Half VCLK, HS_WIDTH656[2:0] = 000b
[2:0]	RO	Reserved	

3.20.3 ITU-656 Decoder VS Delay Register

Address Offset: D3h Access: Read/Write
Default Value: 01h Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	RO	Reserved	
[4:0]	R/W	VS_DELAY656[4:0]	Unit: HS

3.20.4 ITU-656 Decoder VS Pulse Width Register

Address Offset: D4h Access: Read/Write
Default Value: 01h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	VS_in_LineCnt	0: VSync Delay/Width in VCLK count (for those digital video inputs which have no HREF or its codeword during vertical blank) 1: VSync Delay/Width in Line count (for those digital video inputs which keeps sending HREF or its codeword during Vertical Blank)
[6]	R/W	VS_Ex1_Odd	Set to 1 for extra 1 line VSync Offset for Odd field
[5]	R/W	VS_Ex1_Evn	Set to 1 for extra 1 line VSync Offset for Even field
[4:2]	RO	Reserved	
[1:0]	R/W	VS_WIDTH656[1:0]	Unit: HS

3.20.5 ITU-656 Decoder HDE Start Register

Address Offset: D5h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HSTART656[7:0]	Unit: Pixel

3.20.6 ITU-656 Decoder HDE Size LSB Register

Address Offset: D7h Access: Read/Write
Default Value: D0h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W or RO	HSIZE656[7:0]	Unit: Pixel, RO if SIZE_DET=1; else R/W

3.20.7 ITU-656 Decoder HDE Size MSB Register

Address Offset: D8h Access: Read/Write
Default Value: 02h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W or RO	HSIZE656[10:8]	Unit: Pixel

3.20.8 ITU-656 Decoder Odd Field VDE Start Register

Address Offset: D9h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	OVSTART656[7:0]	Odd Filed VDE Start, Unit: HS

3.20.9 ITU-656 Decoder Odd/Even Field VDE Start Register

Address Offset: DAh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	EVPluse1	Even Filed VDE Start 1: EVSTART656=OVSTART + 1 0: EVSTART656=OVSTART
[6:0]	RO	Reserved	

3.20.10 ITU-656 Decoder VDE Size LSB Register

Address Offset: DBh Access: Read/Write
Default Value: F0h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W or RO	VSIZE656[7:0]	Unit: HS, RO if SIZE_DET=1; else R/W

3.20.11 ITU-656 Decoder VDE Size MSB Register

Address Offset: DCh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W or RO	VSIZE656[10:8]	Unit: HS

3.20.12 ITU-656 Decoder VCLK Tuning Register

Address Offset: DEh Access: Read/Write
Default Value: 02h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	One_DE_Only	
[6]	R/W	LHDE_Yes	Enable LHDE input for digital RGB input: 0: Ignore LHDE, then requiring setting capture window 1: Use LHDE to capture active window
[5]	R/W	LODD_INV	Set to 1 for invert LODD/LVSYNC pin
[4]	R/W	LODD_is_VSYNC	Set to 1 if LODD pin acts as VSYNC input
[3]	R/W	LHREF_INV	to 1 for invert LHREF/LHSYNC pin
[2]	R/W	LFIEDLD_in_LHREF	Set to 1 for enabling extract Odd flag from LHREF pin
[1]	R/W	VCLK_INV	VCLK skew: invert
[0]	R/W	VCLK_DLY	VCLK skew: delay

3.20.13 ITU-656 Decoder Format Control Register

Address Offset: DFh Access: Read/Write
Default Value: 40h Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6]	R/W	ODDF_INV	Filed flag indicator 0: 1st field =0, 2nd field=1 1: 1st filed =1, 2nd field=0
[5]	R/W	ReSync_OddF	Set to 1 for re-synchronizing Odd Flag
[4]	R/W	RGB_for_HDTV	Option different color space convert coefficient set
[3]	R/W	A656_V_Align	Chroma_V pixel alignment
[2]	R/W	A656_UV_Intrplt	Interpolate UV pixel values when 422 => 444 converting
[1]	R/W	SIZE_DET	Read back Size of HDE and VDE 0:Disable 1:Enable
[0]	R/W	Detect_Update_	Size detect result update allow, depends on: 0:Update current detection 1:Keep previous detection

3.21 SPI and MCU BIU Register Set

3.21.1 MCU Communication Buffer Register

Address Offset: E0h~EFh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Buffer[0..15][7:0]	Communication Buffers between i8051 and external MCU (through I2C bus)

3.21.2 SPI Instruction Register

Address Offset: F0h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	SPI_Instruction[7:0]	Instruction byte for SPI cycle output

3.21.3 SPI Address Register

Address Offset: F1h~F3h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	F1h: SPI_Address[7:0]	Address lower byte for SPI cycle output
[7:0]	R/W	F2h: SPI_Address[15:8]	Address middle byte for SPI cycle output
[7:0]	R/W	F3h: SPI_Address[23:16]	Address higher byte for SPI cycle output

3.21.4 SPI Single Write Data Register

Address Offset: F4h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	SPI_SingleWr_Data[7:0]	Write Data for SPI single write cycle

3.21.5 SPI Control Register

Address Offset: F5h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	WO/RO	SPI_Issue_Cmd	Write 1 to trigger SPI master to start issuing assigned SPI cycle. Read to check SPI interface is in busy or not.
[6:4]	R/W	SPI_Wr_Length[2:0]	Write byte count (includes Instruction, Address, Data): 0XXb=No Write; 100b=Write-1Byte(P1_F4); 101b=Write-3Bytes(P1_F3~F1); 110b=Write-4-Bytes(P1_F3~F1, F4); 111b=Write-3+N (P1_F3~F1, Buffer)
[3:2]	R/W	SPI_Rd_Length[1:0]	Read Data count: 00b=No Read; 01b=Read-1Byte; 10b=Read-3Bytes; 11b=Repeat Read.

[1]	RO / WO	Check_WIP	Write 1 to auto-attach RDSR instruction, and repeat until WIP = 0. Read to get 1 means WIP already fall. This bit is used when PP/SE/BE/.. need to be applied.
[0]	R/W	SPI_Wait_Done	Set 1 to hold CPU until SPI cycle done. This bit must be set when i8051 initial SPI cycles.

3.21.6 SPI Read Back Data Low Byte Register

Address Offset: F6h Access: Read Only
Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	SPI_ReadBack_Data[7:0]	The first data byte read from SPI ROM. It also could be the SPI_Status[7:0] or SPI_Device_ID[7:0], depends on the instruction.

3.21.7 SPI Read Back Data High Byte Register

Address Offset: F7h Access: Read Only
Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	SPI_Device_ID[15:8]	The 2nd data byte read from SPI ROM: SPI_Device_ID[15:8]

3.21.8 SPI Read Back Data High Byte Register

Address Offset: F8h Access: Read Only
Default Value: XXh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	RO	SPI_Manufacture_ID[7:0]	The 3rd data byte read from SPI ROM: SPI_Manufacture_ID[7:0]

3.21.9 SPI DMA Lower Address Register

Address Offset: F9h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	SPI_DMA_Address[7:0]	DMA Address lower byte for moving data between SPI and T138 chip

3.21.10 SPI DMA High Address Register

Address Offset: FAh Access: Read/Write
Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	SPI_DMA_Address[15:8]	DMA Address high byte for moving data between SPI and T138 chip

3.21.11 SPI DMA Transfer Count LSB Register

Address Offset: FBh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	SPI_DMA_Count[7:0]	DMA transfer count LSB for moving data between SPI and T138 chip

3.21.12 SPI DMA Transfer Control MSB Register

Address Offset: FCh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	WO / RO	SPI_DMA_Go / SPI_DMA_Finish	Write 1 to start DMA transferring; read get 1 means the DMA transfer is finished.
[6]	R/W	SPI_DMA_2_Chip	DMA transfer direction: 0: Read from the SPI buffer in T138 chip to external SPI Flash 1: Read from SPI and write to T138 chip
[5]	R/W	SPI_DMA_Hold_uP	When DMA transferring, to hold MCU (if set to 1) or not (if set o 0)
[4:0]	R/W	SPI_DMA_Count[12:8]	DMA transfer count MSB for moving data between SPI and T138 chip

3.21.13 BIU Cache Control Register

Address Offset: FDh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	Cache_En	Set to 1 enables the Code Cache
[6]	R/W	TimerClk_Sel	0: i8051_Clk, same as i8051 core 1: XCLK, 27MHz
[5]	R/W	TimerClk_Inv	Set to 1 to inverse clock to Timer
[4]	RO	Reserved	
[3:1]	R/W	Cache_BaseAddr[15:13]	Cache Base Address (it may map any 8KB segment in SPI ROM)
[0]	RO	Reserved	

3.21.14 BIU Control Register

Address Offset: FEh Access: Read/Write
Default Value: 05h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W %Strap	i8051_En	This is RSTB reset strap from GPOA6 pin, to default enable built-in 8051 or not. Later, it can be enabled or disabled via setting this bit.
[6]	WO	i8051_Reset	Write 1 to reset the internal 8051 block
[5]	RO	Reserved	
[4:2]	R/W	ORAM_IO_WaitState[1:0]	Extra Wait State for burst accessing OSD RAM when OSD_En=1
[1:0]	R/W	DClk_IO_WaitState[1:0]	Wait State for accessing slow I/O in output clock domain.

3.21.15 Page Select Register

Address Offset: FFh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	I8051_Hold	Set to 1 to hold i8051, should only be set by I2C
[6:2]	RO	Reserved	
[1:0]	R/W	PAGE[1:0]	

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3.22 Y/C Separation and Chroma Decoder Register Set

3.22.1 Video Source Selection of Comb Filter Register

Address Offset: 00h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5]	R/W	PIXEL_CNT	Pixel per scan line. 0: 858 pixels (default) 1: 864 pixels
[4]	R/W	LINE_CNT	Scan lines per frame. 0 = 525 (default) 1 = 625
[3:1]	R/W	TV_MODE	Video standard. 000 = NTSC (default) 001 = PAL (I,B,G,H,D,N) 010 = PAL (M) 011 = PAL (CN) 100 = SECAM
[0]	R/W	INPUT_MODE	Video format. 0 = composite (default) 1 = S-Video (separated Y/C)

3.22.2 Bandwidth Control Register

Address Offset: 01h Access: Read/Write
Default Value: 01h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:4]	R/W	LUMA_FILTER	Luma notch filter bandwidth 00 = none (default) 01 = narrow 10 = medium 11 = wide
[3:2]	R/W	CHROMA_FILTER	Chroma low pass filter bandwidth 0 = narrow (default) 1 = wide 2 = extra wide 3 = extra wide
[1]	R/W	BURST_NUMBER	Burst gate width 0 = 5 subcarrier clock cycles (default) 1 = 10 subcarrier clock cycles
[0]	R/W	PED_ENABLE	Blank-to-black pedestal enable 0 = no pedestal subtraction 1 = pedestal subtraction (default)

3.22.3 Y/C AGC Enable Register

Address Offset: 02h Access: Read/Write
Default Value: 4Fh Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	GAIN_UPDATE	Gain updated mode. 0 = per line (default) 1 = per field
[6]		REVSERVED	
[5:4]	R/W	CLAMP_MODE	DC clamping position 00 = auto (default) 01 = backporch only 10 = synctip only 11 = off
[3]	R/W	DGAIN_EN	Digital AGC enable 0 = off 1 = on (default)
[2]	RO	Reserved	
[1]	R/W	C_AGC_EN	Fixed chroma AGC enable. 0 = off 1 = on (default)
[0]	R/W	L_AGC_EN	Fixed luma/composite AGC enable. 0 = off 1 = on (default)

3.22.4 Comb Filtering Mode Register

Address Offset: 03h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:3]	RO	Reserved	
[2:0]	R/W	COMB_MODE	000 = fully adaptive comb (2-D adaptive comb) (default) 010 = 5-tap adaptive comb filter (PAL mode only) 011 = must be used for S-Video 110 = 5-tap hybrid adaptive comb filter (PAL mode only) others = reserved.

3.22.5 Luma AGC Target Value Register

Address Offset: 04h Access: Read/Write
Default Value: DDh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	AGC_LEVEL	Luma AGC target value.

Standard	Programming Value
NTSC M	DDh (221d) (default)
NTSC J	CDh (205d)
PAL B,D,G,H,I, COMB N, SECAM	DCh (220d)
PAL M,N	DDh (221d)

3.22.6 Y/C Output Control Register

Address Offset: 07h Access: Read/Write
Default Value: 20h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:4]	R/W	BLUE_SCREEN	This bit controls the blue screen mode. 00 = Disabled 01 = Enabled 10 = Auto (Default) 11 = reserved
[3:0]	R/W	YC_DELAY	The range is [-5,7]. Default = 0.

3.22.7 Luma Contrast Register

Address Offset: 08h Access: Read/Write
Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	CONTRAST	*Luma_out* = *Luma_in* * CONTRAST where CONTRAST is a 1.7-bit fixed point value.

3.22.8 Luma Brightness Register

Address Offset: 09h Access: Read/Write
Default Value: 20h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	BRIGHTNESS	*Luma_out* = *Luma_in* + BRIGHTNESS - 32

3.22.9 Chroma Saturation Register

Address Offset: 0Ah Access: Read/Write
Default Value: 80h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	SATURATION	*Chroma_out* = *Chroma_in* * SATURATION where SATURATION is a 1.7-bit fixed point value

3.22.10 Chroma Hue Phase Register

Address Offset: 0Bh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	HUE	*U_out = U_in*cos(*HUE*/256*360) + V_in * sin(*HUE*/256*360)* *V_out = V_in*cos(*HUE*/256*360) - U_in * sin(*HUE*/256*360)*

3.22.11 Chroma AGC Register

Address Offset: 0Ch Access: Read/Write
Default Value: 8ah Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	CHROMA_AGC	Chroma AGC target. Default = 138.

3.22.12 AGC Peak Nominal Register

Address Offset: 10h Access: Read/Write
Default Value: 0ah Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6:0]	R/W	AGC_PEAK	Luma peak value. Default = 10.

3.22.13 Chroma DTO Incremental 0 Register

Address Offset: 18h Access: Read/Write
Default Value: 21h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	CHROMA_FREQ_FIX	Fix chroma frequency. 0: disable (default). 1: enable.
[6]	RO	Reserved	
[5:0]	R/W	C_FREQ[29:24]	Bits 29:24 of the 30-bit-wide chroma frequency increment.

3.22.14 Chroma DTO Incremental 1 Register

Address Offset: 19h Access: Read/Write
Default Value: F0h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	C_FREQ[23:16]	Bits 23:16 of the 30-bit-wide chroma frequency increment.

3.22.15 Chroma DTO Incremental 2 Register

Address Offset: 1Ah Access: Read/Write
Default Value: 7Ch Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	C_FREQ[15:8]	Bits 15:8 of the 30-bit-wide chroma frequency increment.

3.22.16 Chroma DTO Incremental 3 Register

Address Offset: 1Bh Access: Read/Write
Default Value: 0Fh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	C_FREQ[7:0]	Bits 7:0 of the 30-bit-wide chroma frequency increment.

3.22.17 Active Video Horizontal Start Time Register

Address Offset: 2Eh Access: Read/Write
Default Value: 82h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	H_START	Active video horizontal start position. Default = 130.

3.22.18 Active Video Horizontal Width Register

Address Offset: 2Fh Access: Read/Write
Default Value: 50h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	H_WIDTH	Active video horizontal pixel counts. Default = 80 → 640+80 = 720

3.22.19 Active Video Vertical Start Register

Address Offset: 30h Access: Read/Write
Default Value: 22h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	V_START	Active video vertical line start position. Default = 34.

3.22.20 Active Video Vertical Height Register

Address Offset: 31h Access: Read/Write
Default Value: 61h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	V_WIDTH	Active video vertical line counts. Default = 97 (384+97 = 481 half lines

3.22.21 Comb Video Status Register 1

Address Offset: 3Ah Access: Read only
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:5]	RO	mv_colourstripes	Macrovision color stripes detected. The number indicates the number of color stripe lines in each group
[4]	RO	mv_vbi_detected	MacroVision VBI pseudo-sync pulses detection 1 = Detected 0 = Undetected
[3]	RO	chromalock	Chroma PLL locked to color burst 1 = Locked 0 = Unlocked
[2]	RO	vlock	Vertical lock 1 = Locked 0 = Unlocked
[1]	RO	hlock	Horizontal line locked 1 = Locked 0 = Unlocked
[0]	RO	no_signal	No signal detection 1 = No Signal Detected 0 = Signal Detected

3.22.22 Comb Video Status Register 2

Address Offset: 3Bh Access: Read only
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R	Line_Eq_to_625	Slow response to line 625 detection
[6]	R	Line_Close_to_625	Fast response to line 625 detection
[5]	R	Fsc3_Present	
[4]	R	Fsc2_Present	
[3]	R	Fsc1_Present	
[2]	R	CKillON	1:chroma is being killed 0:no chroma is being killed
[1]	R	WeakChroma	1:indicates incoming signal contains weak color burst 0:no weak color burst amplitude is present
[0]	RO	Proscan_detected	Progressive Scan Video Detected

3.22.23 Comb Video Status Register 3

Address Offset: 3Ch Access: Read only
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO	vcr_rew	VCR Rewind Detected
[6]	RO	vcr_ff	VCR Fast-Forward Detected
[5]	RO	vcr_trick	VCR Trick-Mode Detected
[4]	RO	vcr	VCR Detected
[3]	RO	noisy	Noisy Signal Detected. This bit is set when the detected noise value (status register P2_7Fh) is greater than the value programmed into the "noise_thresh" register (P2_05h).
[2]	RO	vline_625_detected	625 Scan Lines Detected
[1]	RO	secam_detected	SECAM Color Mode Detected
[0]	RO	pal_detected	PAL Color Mode Detected

3.22.24 Soft Reset Register

Address Offset: 3Fh Access: Read/Write
Default Value: 01h Size: 8 bits

Bit	Access	Symbol	Description
[7:1]	RO	Reserved	
[0]	R/W	RESET	Soft Reset: Write 1 to reset initial values for comb filter

3.22.25 Luminance Peaking Control Register

Address Offset: 80h Access: Read/Write
Default Value: 04h Size: 8 bits

Bit	Access	Symbol	Description
[7:6]	RO	Reserved	
[5:4]	R/W	PEAK_RANGE	Range of peak_gain. Setting peak_range value 00 1 (default) 01 2 10 4 11 8 Ypeak = Y + YH *(peak_gain/peak_range) where Y is the luma and YH is the high frequency luma only

[3:1]	R/W	PEAK_GAIN	peak_gain. Default = 2.
[0]	R/W	PEAK_EN	Luma horizontal peaking control enable. 0 = Disabled (default) 1 = Enabled

3.22.26 Comb Filter Configuration Register

Address Offset: 82h Access: Read/Write
Default Value: 42h Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6]	R/W	PAL_ERR	PAL error reduced. 0: disable. 1: enable.
[5]	R/W	PAL_AUTO_EN	PAL error detect enable 0: disable. 1: enable.
[4]	R/W	COMB_PAL	PAL comb filter enable. 0: disable. 1: enable.
[3:2]	RO	Reserved	
[1:0]	R/W	PAL_SW_LEVEL	PAL switch level. Default = 2.

3.22.27 Comb Lock Configuration Register

Address Offset: 83h Access: Read/Write
Default Value: 6Fh Size: 8 bits

Bit	Access	Symbol	Description
[7:4]	R/W	lose_chromalock_count	This register is used to tune the chromakill, higher values are more sensitive to losing lock Default = 6.
[3:1]	R/W	lose_chromalock_level	Set the level for chromakill. Default = 7.
[0]	R/W	lose_chromalock_ckill	When set, chroma is killed whenever chromlock is lost. Default = 1.

3.22.28 DDS Fsc1 Frequency

Address Offset: A0h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	DDS_FSC1[31:24]	

3.22.29 DDS Fsc1 Frequency

Address Offset: A1h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	DDS_FSC1[23:16]	

3.22.30 DDS Fsc1 Frequency

Address Offset: A2h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	DDS_FSC1[15:8]	

3.22.31 DDS Fsc1 Frequency

Address Offset: A3h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	DDS_FSC1[7:0]	

3.22.32 DDS Fsc2 Frequency

Address Offset: A4h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	DDS_FSC2[31:24]	

3.22.33 DDS Fsc2 Frequency

Address Offset: A5h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	DDS_FSC2[23:16]	

3.22.34 DDS Fsc2 Frequency

Address Offset: A6h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	DDS_FSC2[15:8]	

3.22.35 DDS Fsc2 Frequency

Address Offset: A7h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	DDS_FSC2[7:0]	

3.22.36 DDS Fsc3 Frequency

Address Offset: A8h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	DDS_FSC3[31:24]	

3.22.37 DDS Fsc3 Frequency

Address Offset: A9h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	DDS_FSC3[23:16]	

3.22.38 DDS Fsc3 Frequency

Address Offset: AAh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	DDS_FSC3[15:8]	

3.22.39 DDS Fsc3 Frequency

Address Offset: ABh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	DDS_FSC3[7:0]	

3.22.40 Start of Fsc Line Coverage

Address Offset: ACh Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Line_Fsc_Start	

3.22.41 End of Fsc Line Coverage

Address Offset: ADh Access: Read/Write
Default Value: 09h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Line_Fsc_End	

3.22.42 Start of Fsc1/2 Detection Window

Address Offset: AEh Access: Read/Write
Default Value: 2Dh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Window_Fsc_Start	

3.22.43 End of Fsc1/2 Detection Window

Address Offset: AFh Access: Read/Write
Default Value: 40h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Window_Fsc_End	

3.22.44 Start of Fsc3 Detection Window

Address Offset: B0h Access: Read/Write
Default Value: 48h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Window_Fsc3_Start	

3.22.45 End of Fsc3 Detection Window

Address Offset: B1h Access: Read/Write
Default Value: 5Bh Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	Window_Fsce_End	

3.22.46 Spectrum Analysis

Address Offset: B2h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:1]	R/W	RESERVED	
[0]	R/W	Freq_Dist	1:Frequency distribution 0:Frequency correlation

3.22.47 Component Chroma LPF

Address Offset: C1h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:1]	R/W	RESERVED	
[0]	R/W	CMPV_CLPF	Used for YPbPr video 1: Enable chroma LPF 0: Disable chroma LPF

4 Electrical Characteristics

4.1 Digital I/O Pad Operation Condition

Table 4-1 Operation Condition

	Parameter	Min	Typ	Max
VDD18	Digital Core Power Supply	1.62V	1.8V	1.98V
VD33	Digital I/O Power Supply	3.0V	3.3V	3.6V
V_{IL}	Input Low Voltage	-0.3V		0.8V
V_{IH}	Input High Voltage	2.0V		5.0V
V_{T+}	Schmitt Trigger Low-to-High Threshold	1.44V	1.58V	1.71V
V_{T+}	Schmitt Trigger High-to-Low Threshold	1.09V	1.19V	1.31V
I_I	Input Leakage Current@ V_I=3.3V or 0V			±1μA
I_{OZ}	Tri-state Output Leakage Current@ V_O=3.3V or 0V			±1μA
I_{OL}	Low level Output Current@ V_{OL}=0.4V			
	2mA	2.1mA	3.4mA	4.2mA
	4mA	4.2mA	6.9mA	8.6mA
	8mA	8.4mA	13.9mA	17.2mA
	12mA	12.5mA	20.8mA	25.8mA
I_{OH}	High level Output Current@ V_{OH}=2.4V			
	2mA	3.0mA	6.2mA	10.0mA
	4mA	5.7mA	11.6mA	18.6mA
	8mA	9.5mA	19.4mA	30.9mA
	12mA	13.3mA	27.1mA	43.3mA
R_{PU}	Pull-up resistor	74KΩ	104KΩ	177KΩ
R_{PD}	Pull-down resistor	62KΩ	90KΩ	176KΩ

Note: R_{PU} and R_{PD} are always present no matter normal operation or power down mode is enabled. A typical 30~40μA false leakage current is resulted from R_{PU} and R_{PD} when a tester forces I/O to 3.3V or 0.0 V.

4.2 DC Characteristics

(VDD18=1.8V; VD33=3.3V; AVDDR=AVDDG=AVDDB=AVDDP=AVDDAC=3.3V; VREF=1.235V; RL=37.5ohm, CL=10pF; RSET=386ohm; Temp=75oC, unless otherwise noted)

Table 4-2 DC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Operating voltage range	AVDDR/G/B AVDDP AVDDAC VD33	3.0	3.3	3.6	V	
Operating voltage range	VDD18	1.62	1.8	1.98	V	
Operating voltage range	VD5A	4.2	4.5	4.7	V	
AVDDR supply current	IAVDDR	--	15	20	mA	SL=0, SLR=0
AVDDG supply current	IAVDDG	--	15	20	mA	SL=0, SLG=0
AVDDB supply current	IAVDDB	--	15	20	mA	SL=0, SLB=0
VD33 supply current	IVD33	--	30	35	mA	SL=0
VDD18 supply current	IVDD18	--	40	44	mA	
VD5A supply current	IVD5A	--	30	33	mA	
Full scale current	IOFS	2.00	34.08	--	mA	Full-Scale adjust resistor. A resistor should be connected between this pin and AVS33 to control the magnitude of the full-scale video signal. RSET(ohm)=VREFIN(V)*10.66/IOFS(A) ,where IOFS is full-scale output current.
Output voltage range	V(IO)	--	4.0	--	V	.
DAC resolution	--	--	8	--	bits	.
Integral non-linearity error	INL	--	0.5	+-2	LSB	.
Differential non-linearity error	DNL	--	0.5	+-1	LSB	.

4.3 AC Characteristics

(VDD18=1.8V; VD33=3.3V; AVDDR=AVDDG=AVDDB=AVDDP=AVDDAC =3.3V; VREF=1.235V; RL=37.5ohm; CL=10pF; RSET=386ohm; Temp=75oC, unless otherwise noted)

Table 4-3 AC Characteristics

Parameter	Sym	Min	Typ	Max	Unit	Condition
CK period	Tck	5	--	--	Ns	
CK to valid output	Tdelay	--	--	0.5*Tck+2	Ns	
Output rise time	Tr	--	--	4	Ns	10% to 90% IOFS; assume no package inductance.
Output fall time	Tf	--	--	4	Ns	90% to 10% IOFS; assume no package inductance.
Output settling time	Tsettle	--	--	TBD	Ns	assume no package inductance
Glitch energy	--	--	--	--	pvs	assume no package inductance
DAC to DAC crosstalk	--	--	TBD	--	Db	.

4.4 Analog Processing and A/D Converters

Table 4-4 Analog Characteristics

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Zi	Input impedance, analog video inputs	By design	500			kΩ
Ci	Input capacitance, analog video inputs	By design		10		pF
Vi(pp)	Input voltage range†	Ccoupling = 0.1µF	0.7	1.0	1.3	V
△G	Gain control range		0		12	dB
DNL	DC differential nonlinearity	A/D only		±0.5		LSB
INL	DC integral nonlinearity	A/D only		±1		LSB
Fr	Frequency response	6 MHz		−0.9		dB
			−3			
SNR	Signal-to-noise ratio	6 MHz, 1.0 Vp-p		50		dB
NS	Noise spectrum	50% flat field		50		dB
DP	Differential phase		1.5			
DG	Differential gain			0.5%		

4.5 I²C Host Interface Timing

Table 4-5 I²C Host Interface Timing

	Parameter	Min	Typ	Max
t1	Bus free time between a Stop and Start condition	4.7us		
t2	Hold time (repeated) Start condition	4.0us		
t3	Rise time of both SDA and SCL			1000ns
t4	Data hold time	5.0us		
t5	Data setup time	250ns		
t6	Fall time of both SDA and SCL			300ns
t7	Setup time for a repeated Start condition	4.7us		
t8	Setup time for Stop condition	4.0us		
tLow	Low period of the SCL	4.7us		
tHigh	High period of the SCL	4.0us		
fSCL	SCL clock frequency			1Mhz
Cb	Capacitive load for each bus line			400pF

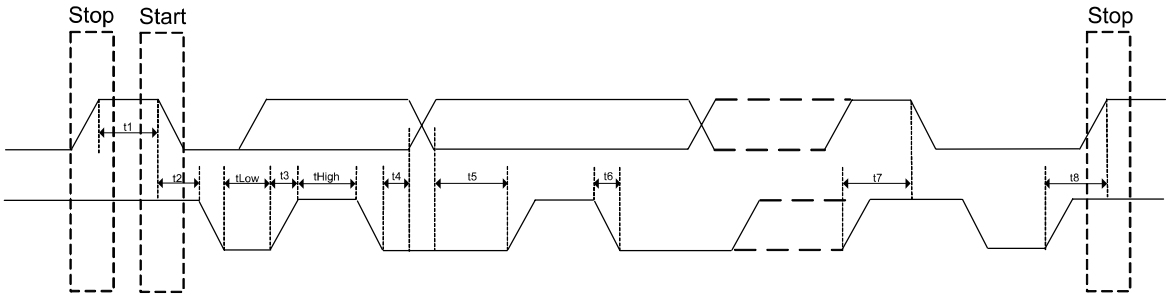
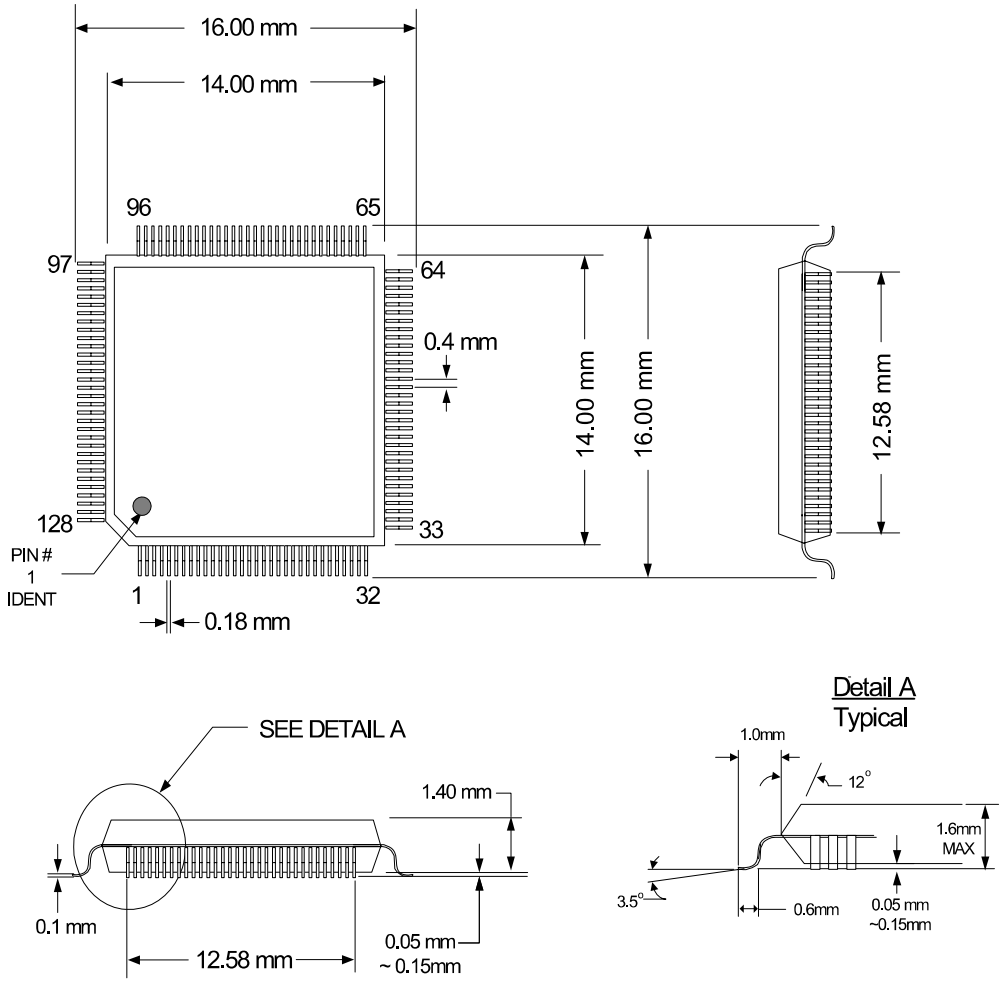


Figure 4-1 I²C Timing

5 Package Dimensions



128 LQFP 14 X 14 X 1.4 mm

Figure 5-1 128-Pin LQFP Dimensions

6 Ordering Information

Table 6-1 Ordering Information

Part No.	Package
T138AF	128 LQFP

7 Revisions Note

Table 7-1 Revision Note

Revisions	Description of changes	Date	Note
0.1	First draft	November 28, 2008	
1.00	First release	January 10, 2009	
1.01	Add OS2_0Eh; Pin description revise.	January 12, 2009	
1.03	Specified for T138AF	May 7, 2009	

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9 Contact Information

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