International
IOR Rectifier

ADVANCED INFORMATION **Data Sheet No. PD60166B**

IR2136/IR21362

3-PHASE BRIDGE DRIVER

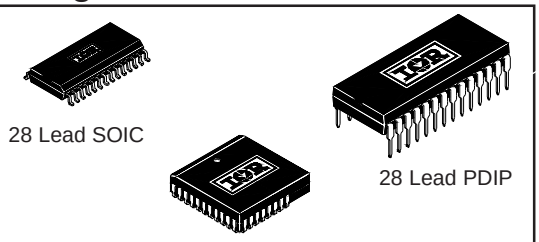
Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V (IR2136) or 12 to 20V (IR21362)
- Undervoltage lockout for all channels
- Over-current shutdown turns off all six drivers
- Independent 3 half-bridge drivers
- Matched propagation delay for all channels
- Lowside outputs out of phase with inputs. High side outputs out of phase (IR2136) or in phase (IR21362) with inputs.
- 5V Schmitt-triggered input logic
- Cross-conduction prevention logic
- Lower di/dt gate driver for better noise immunity
- Externally programmable delay for automatic fault clear

Product Summary

V_{OFFSET}	600V max.
I_O+/-	120 mA / 250 mA
V_{OUT}	10 - 20V or 12V - 20V
Deadtime (typ.)	200 nsec
$t_{on/off}$ (typ.)	400 nsec

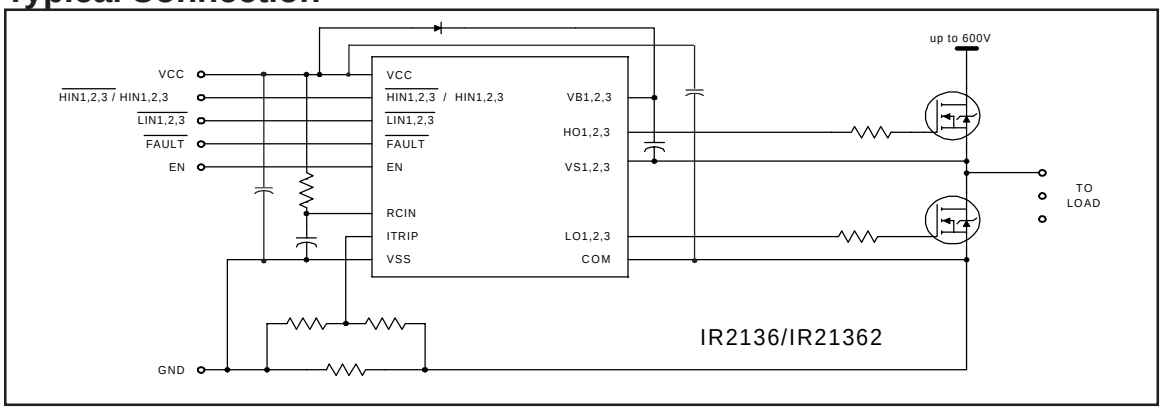
Packages



Description

The IR2136/IR21362 are high votage, high speed power MOSFET and IGBT drivers with three independent high and low side referenced output channels for 3-phase applications. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with 5V CMOS or LSTTL outputs. A current trip function which terminates all six outputs can be derived from an external current sense resistor. An enable function is available to terminate all six outputs simultaneously. An open-drain FAULT signal is provided to indicate that an overcurrent or undervoltage shutdown has occurred. Overcurrent fault conditions are cleared automatically after a delay programmed externally via an RC network connected to the RCIN input. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operates up to 600 volts.

Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_S	High side offset voltage		-0.3	600	V
V_{BS}	High side floating supply voltage		-0.3	25	
V_{HO}	High side floating output voltage		$V_{S1,2,3}$ - 0.3	$V_{B1,2,3}$ + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{SS}	Logic ground		V_{CC} - 25	V_{CC} + 0.3	
$V_{LO1,2,3}$	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Input voltage $\overline{LIN}$,$\overline{HIN}$(IR2136),HIN (IR21362) ITRIP, EN, RCIN		V_{SS} - 0.3	V_{CC} + 0.3	
V_{FLT}	$\overline{FAULT}$ output voltage		V_{SS} - 0.3	V_{CC} + 0.3	
dV/dt	Allowable offset voltage slew rate		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(28 lead PDIP)	—	1.5	W
		(28 lead SOIC)	—	1.6	
		(44 lead PLCC)	—	2.0	
Rth_{JA}	Thermal resistance, junction to ambient	(28 lead PDIP)	—	83	°C/W
		(28 lead SOIC)	—	78	
		(44 lead PLCC)	—	63	
T_J	Junction temperature		—	125	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute referenced to COM. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High side floating supply voltage	$V_{S1,2,3}$ + 10	$V_{S1,2,3}$ + 20	V
$V_{S1,2,3}$	High side floating supply offset voltage	Note 1	600	
$V_{HO1,2,3}$	High side output voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	
$V_{LO1,2,3}$	Low side output voltage	0	V_{CC}	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{SS}	Logic ground	-5	5	
V_{FLT}	$\overline{FAULT}$ output voltage	V_{SS}	V_{CC}	
V_{RCIN}	RCIN input voltage	V_{SS}	V_{CC}	
V_{ITRIP}	ITRIP input voltage	V_{SS}	V_{SS} +5	
V_{IN}	Logic input voltage $\overline{LIN}$, $\overline{HIN}$ (IR2136), HIN(IR21362), EN	V_{SS}	V_{SS} +5	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of COM -5 to COM +600V. Logic state held for V_S of COM -5V to -COM -V_{BS}.

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}1,2,3) = 15V unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels (H_S1,2,3 and L_S1,2,3). The V_O and I_O parameters are referenced to COM and V_S1,2,3 and are applicable to the respective output leads: $H_{O1,2,3}$ and $L_{O1,2,3}$.

Symbol	Definition		Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "0" input voltage $\overline{LIN1,2,3}$, $\overline{HIN1,2,3}$ Logic "1" input voltage HIN1,2,3		2.7	—	—	V	
V_{IL}	Logic "1" input voltage $\overline{LIN1,2,3}$, $\overline{HIN1,2,3}$ Logic "0" input voltage HIN1,2,3		—	—	0.8	V	
$V_{EN,TH+}$	EN positive going threshold		—	—	2.7	V	
$V_{EN,TH-}$	EN negative going threshold		0.8	—	—	V	
$V_{IT,TH+}$	ITRIP positive going threshold		—	480	—	mV	
$V_{IT,HYS}$	ITRIPinput hysteresis		—	80	—	mV	
$V_{RCIN,TH+}$	RCIN positive going threshold		—	8	—	V	
$V_{RCIN,HYS}$	RCIN input hysteresis		—	3	—	V	
V_{OH}	High level output voltage, V_{BIAS} - V_O		—	0.8	1.4	V	I_O = 20 mA
V_{OL}	Low level output voltage, V_O		—	0.3	0.6	V	I_O = 20 mA
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	IR2136 IR21362	8.0 9.6	8.9 10.4	9.8 11.2	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	IR2136 IR21362	7.4 8.6	8.2 9.4	9.0 10.2	V	
V_{CCUVH} V_{BSUVH}	V_{CC} and V_{BS} supply undervoltage lockout hysteresis	IR2136 IR21362	0.3 0.5	0.7 1.0	— —	V	
I_{LK}	Offset supply leakage current		—	—	50	µA	$V_{B1,2,3}$=$V_{S1,2,3}$ =600V
I_{QBS}	Quiescent V_{BS} supply current		20	60	150	µA	V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} supply current		—	1	2	mA	V_{IN} = 0V or 5V
I_{IN+}	Input bias current (OUT = HI or OUT = LO)		—	120	—	µA	V_{IN} = 0V or 5V
I_{ITRIP+}	"high" ITRIP input bias current		—	100	—	µA	V_{ITRIP} = 5V
I_{ITRIP-}	"low" ITRIP input bias current		—	0	1	µA	V_{ITRIP} = 0V
I_{EN+}	"high" ENABLE input bias current		—	100	—	µA	V_{ENABLE}= 5V
I_{EN-}	"low" ENABLE input bias current		—	0	1	µA	V_{ENABLE} = 0V
I_{RCIN}	RCIN input bias current		—	0	1	µA	V_{RCIN} = 0V or 15V
I_{O+}	Output high short circuit pulsed current		120	200	—	mA	V_O= 0V, PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current		250	350	—	mA	V_O= 15V, PW ≤ 10 µs
$R_{ON,RCIN}$	RCIN low on resistance		—	60	—	Ω	
$R_{ON,FLT}$	FAULT low on resistance		—	60	—	Ω	

Dynamic Electrical Characteristics

V_{CC} = V_{BS} = V_{BIAS} = 15V, $V_{S1,2,3}$ = V_{SS} = COM and C_L = 1000 pF unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	400	—	nS	V_{IN} = 0 & 5V $V_{S1,2,3}$ = 0 to 600V
t_{off}	Turn-off propagation delay	—	380	—		
t_r	Turn-on rise time	—	110	—		
t_f	Turn-off fall time	—	50	—		
t_{EN}	ENABLE low to output shutdown propagation delay	—	400	—		V_{IN}, V_{EN} = 0V or 5V
t_{ITRIP}	ITRIP to output shutdown propagation delay	—	700	—		V_{ITRIP} = 5V
t_{bl}	ITRIP blanking time	100	150	—		V_{IN} = 0V or 5V V_{ITRIP} = 5V
t_{FLT}	ITRIP to FAULT propagation delay	—	500	—		V_{IN} = 0V or 5V V_{ITRIP} = 5V
t_{FILIN}	Input filter time (HIN, LIN, EN)	100	200	—		V_{IN} = 0 & 5V
t_{FLTCLR}	FAULT clear time RCIN: R=2meg, C=1nF	—	1.8	—	mS	V_{IN} = 0V or 5V V_{ITRIP} = 0V
DT	Deadtime	—	250	—	nS	V_{IN} = 0 & 5V
MT	Matching delay ON and OFF	—	0	80		
MDT	Matching delay, max (t_{on},t_{off}) - min (t_{on},t_{off}), (ton,toff are applicable to all 3 channels)	—	0	75		External dead time >400nsec
PM	Output pulse width matching, PWin - PWout (fig.2)	—	0	75		

NOTE: For high side PWM, HIN pulse width must be ≥ 1μsec

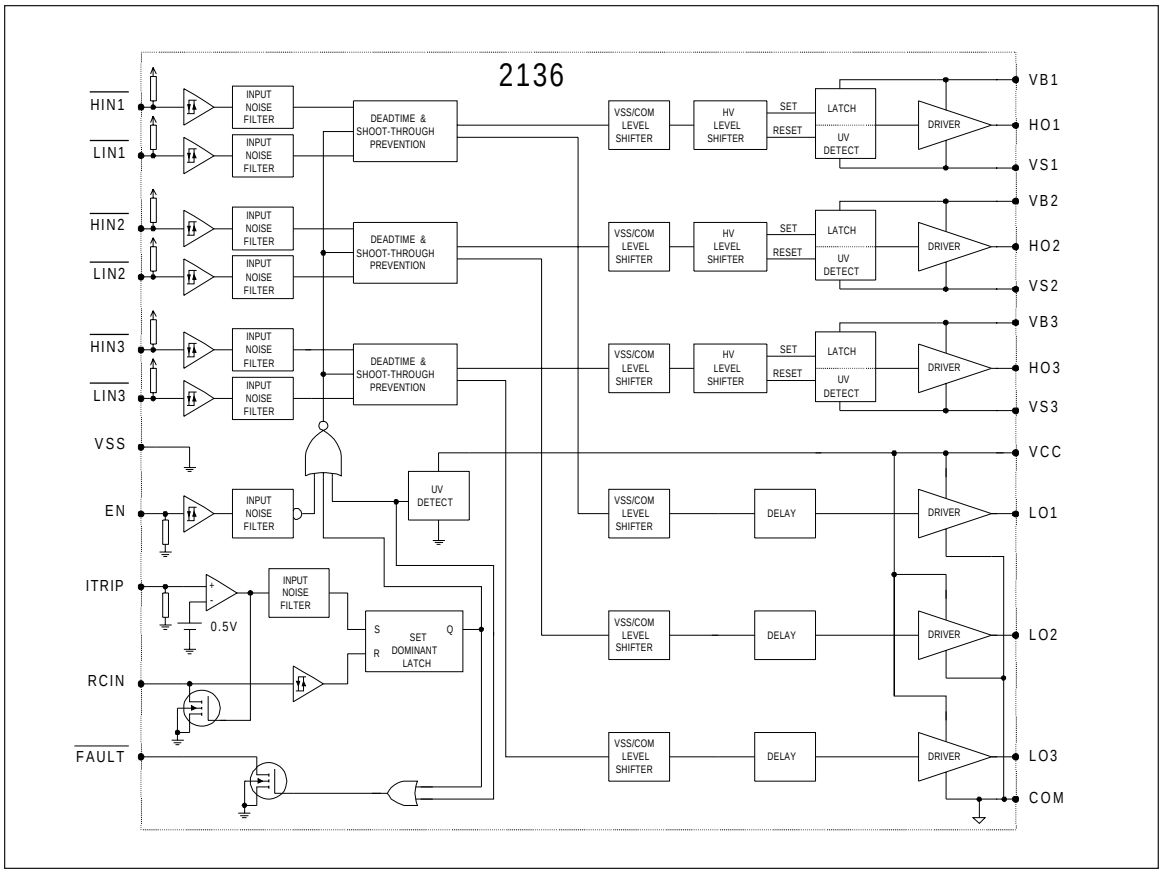
VCC	VBS	ITRIP	ENABLE	FAULT	LO1,2,3	HO1,2,3
<UVCC	X	X	X	0 (note 1)	0	0
15V	<UVBS	0V	5V	high imp	LIN1,2,3	0
15V	15V	0V	5V	high imp	LIN1,2,3	HIN1,2,3
15V	15V	>VITRIP	5V	0 (note 2)	0	0
15V	15V	0V	0V	high imp	0	0

Note: A shoot-through prevention logic prevents LO1,2,3 and HO1,2,3 for each channel from turning on simultaneously.

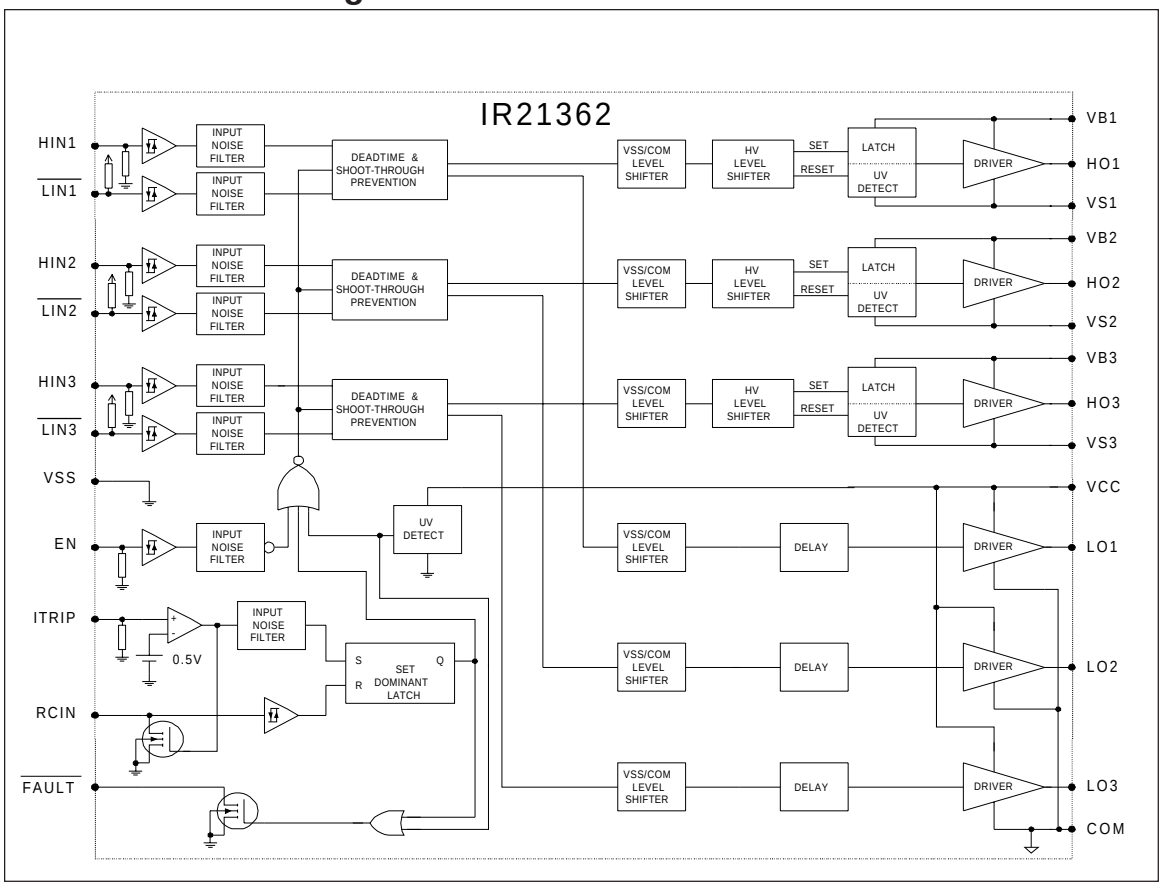
Note 1: UVCC is not latched, when VCC>UVCC, FAULT returns to high impedance.

Note 2: When ITRIP <V_{ITRIP}, FAULT returns to high-impedance after RCIN pin becomes greater than 8V (@ VCC = 15V)

Functional Block Diagram

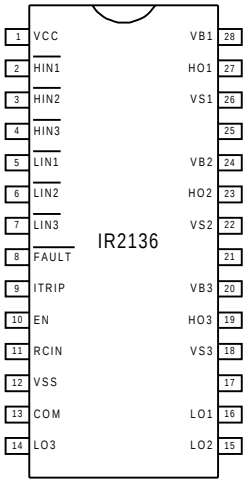


Functional Block Diagram



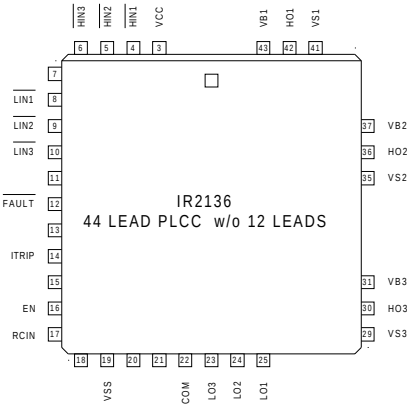
Lead Definitions

Symbol	Description
V_{CC}	Low side and logic fixed supply
VSS	Logic Ground
$\overline{HIN1,2,3}$ HIN1,2,3	Logic inputs for high side gate driver outputs (HO1,2,3), out of phase (IR2136) Logic inputs for high side gate driver outputs (HO1,2,3), in phase (IR21362)
$\overline{LIN1,2,3}$	Logic inputs for low side gate driver outputs (LO1,2,3), out of phase
FAULT	Indicates over-current (ITRIP) or low-side undervoltage lockout has occured. Negative logic, open-drain output
EN	Logic input to enable I/O functionality. Positive logic, i.e. I/O logic functions when ENABLE is high. No effect on FAULT and not latched
ITRIP	Analog input for overcurrent shutdown. When active, ITRIP shuts down outputs and activates FAULT and RCIN low. When ITRIP becomes inactive, FAULT stays active low for an externally set time T_{FLTCLR}, then automatically becomes inactive (open-drain high impedance).
RCIN	External RC network input used to define FAULT CLEAR delay, T_{FLTCLR}, approximately equal to R*C. When RCIN>8V, the FAULT pin goes back into open-drain high-impedance
COM	Low side gate driver return
V_B1,2,3	High side floating supply
HO1,2,3	High side gate driver outputs
$V_{S1,2,3}$	High voltage floating supply returns
LO1,2,3	Low side gate driver output



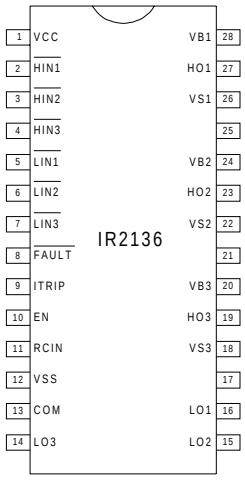
28 Lead PDIP

IR2136



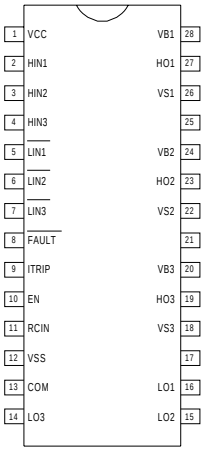
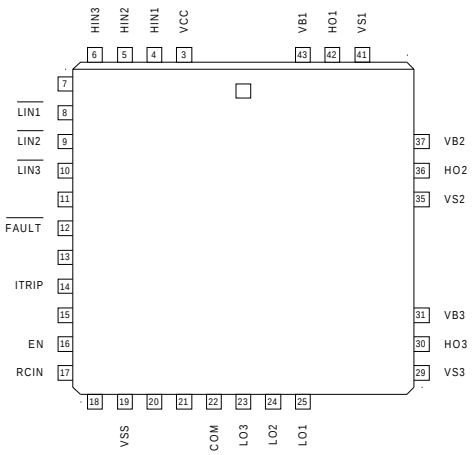
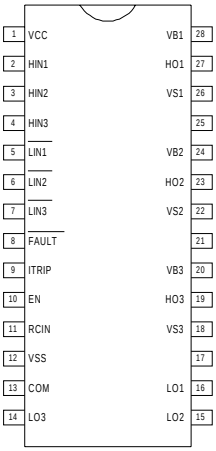
44 Lead PLCC w/o 12 leads

IR2136J

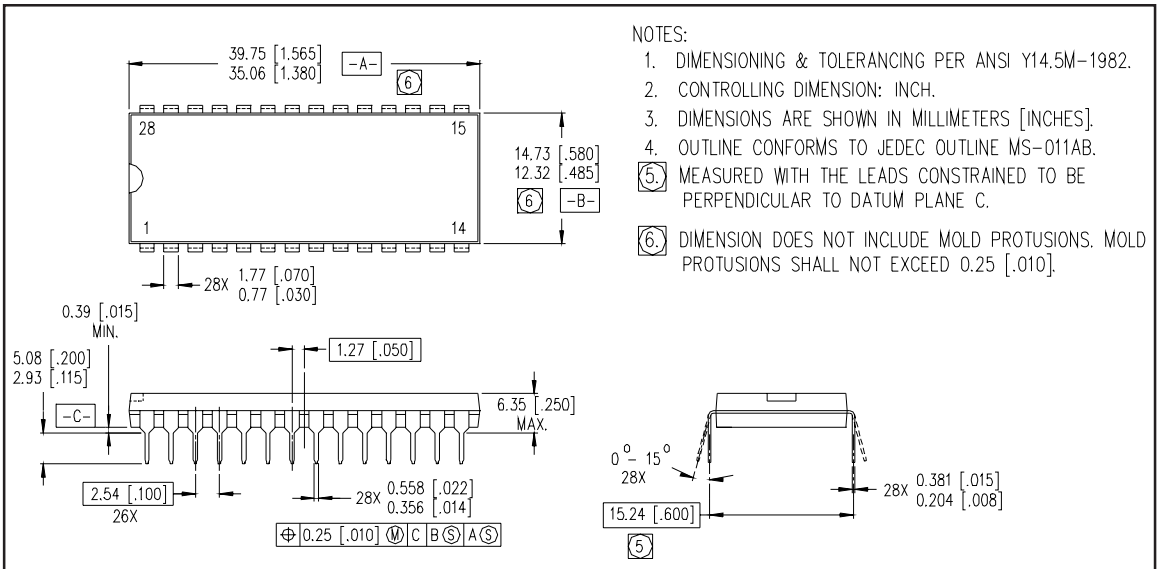


28 lead SOIC (wide body)

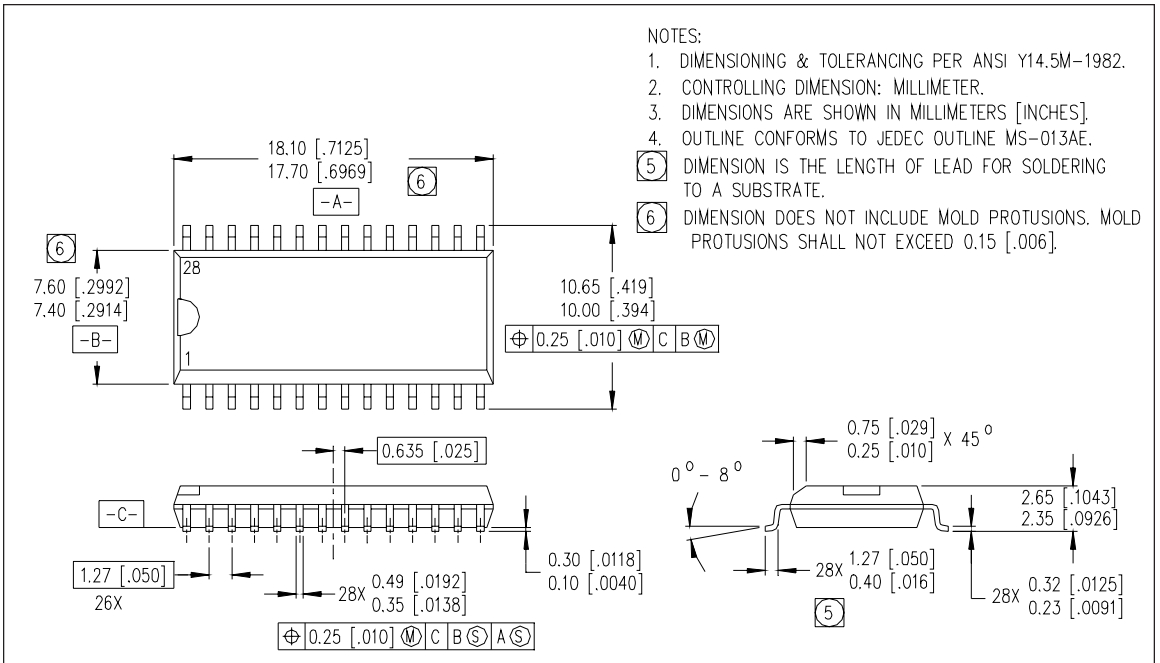
IR2136S

		
28 Lead PDIP	44 Lead PLCC w/o 12 leads	28 lead SOIC (wide body)
IR21362	**IR21362J**	**IR21362S**

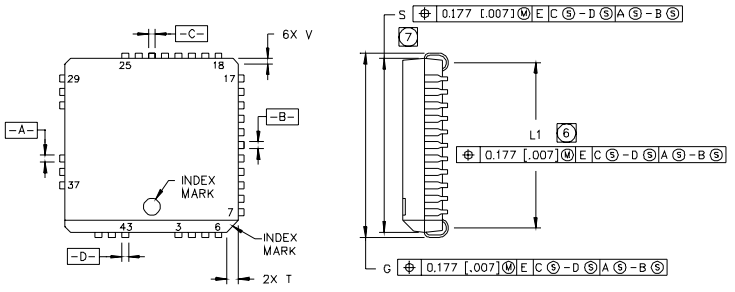
Package Dimensions



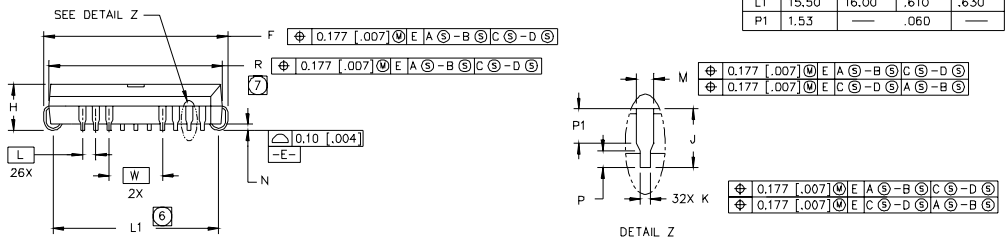
28 Lead PDIP (wide body) 01-3024 02



28 Lead SOIC (wide body) 01-3040 01



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F	17.40	17.65	.685	.695
G	17.40	17.65	.685	.695
H	4.20	4.57	.165	.180
J	2.29	3.04	.090	.120
K	0.33	0.48	.013	.019
L	1.27 BSC		.050 BSC	
M	0.66	0.81	.026	.032
N	0.51	—	.020	—
P	0.64	—	.025	—
R	16.51	16.66	.650	.656
S	16.51	16.66	.650	.656
T	1.07	1.21	.042	.048
V	—	0.50	—	.020
W	5.08 BSC		.200 BSC	
L1	15.50	16.00	.610	.630
P1	1.53	—	.060	—



NOTES:

1. DIMENSIONING & TOLERENCING PER ANSI Y14.5M-1982.
2. DIMENSIONS SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE MS-018AC.
5. DATUMS -A-, -B-, -C-, & -D- ARE DETERMINED BY WHERE THE TOP OF THE LEADS EXIT PLASTIC BODY AT MOLD PARTING LINE.
6. TO BE MEASURED AT -E- SEATING PLANE.
7. DIMENSIONS DO NOT INCLUDE MOLD FLASH, ALLOWABLE FLASH IS 0.254 [.010].

44 Lead PLCC w/o 12 Leads

01-3004 02

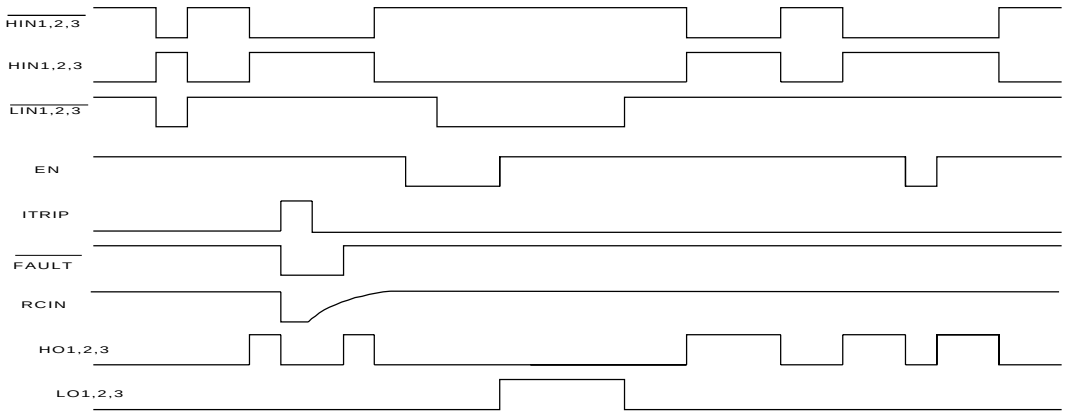


Figure 1. Input/Output Timing Diagram

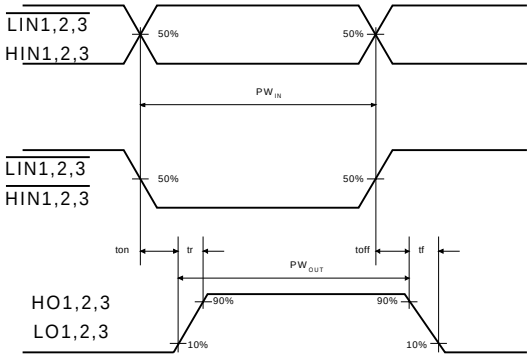


Figure 2. Switching Time Waveforms

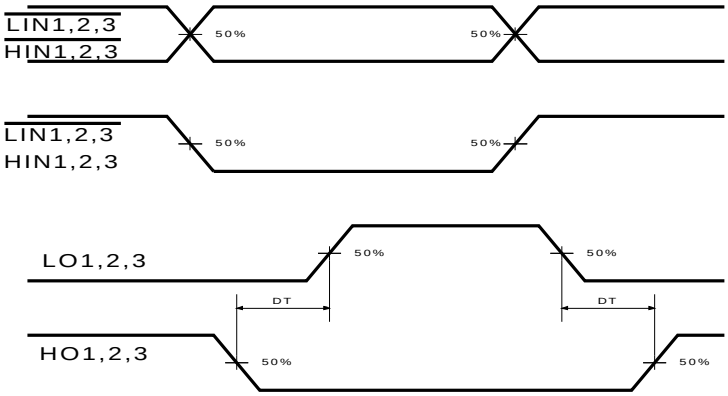


Figure 3. Internal Deadtime Timing Waveforms

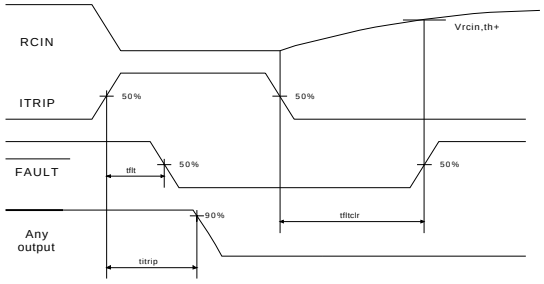


Figure 4. ITRIP/RCIN Timing Waveforms

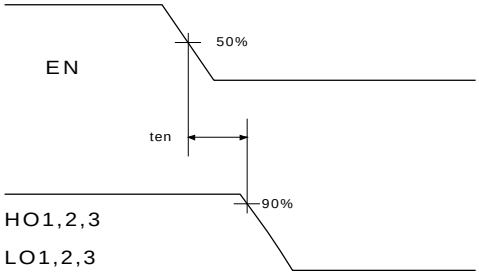


Figure 5. Output Enable Timing Waveform

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IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
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