

## MAX232x Dual EIA-232 Drivers/Receivers

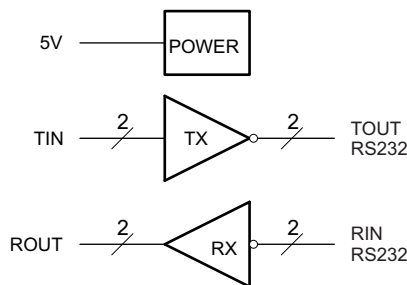
### 1 Features

- Meets or Exceeds TIA/EIA-232-F and ITU Recommendation V.28
- Operates From a Single 5-V Power Supply With 1.0- $\mu$ F Charge-Pump Capacitors
- Operates up to 120 kbit/s
- Two Drivers and Two Receivers
- $\pm 30$ -V Input Levels
- Low Supply Current: 8 mA Typical
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
- Upgrade With Improved ESD (15-kV HBM) and 0.1- $\mu$ F Charge-Pump Capacitors is Available With the MAX202 Device

### 2 Applications

- TIA/EIA-232-F
- Battery-Powered Systems
- Terminals
- Modems
- Computers

### 4 Simplified Schematic



### 3 Description

The MAX232 device is a dual driver/receiver that includes a capacitive voltage generator to supply TIA/EIA-232-F voltage levels from a single 5-V supply. Each receiver converts TIA/EIA-232-F inputs to 5-V TTL/CMOS levels. These receivers have a typical threshold of 1.3 V, a typical hysteresis of 0.5 V, and can accept  $\pm 30$ -V inputs. Each driver converts TTL/CMOS input levels into TIA/EIA-232-F levels.

#### Device Information<sup>(1)</sup>

| ORDER NUMBER | PACKAGE (PIN) | BODY SIZE          |
|--------------|---------------|--------------------|
| MAX232x      | SOIC (16)     | 9.90 mm x 3.91 mm  |
|              | SOIC (16)     | 10.30 mm x 7.50 mm |
|              | PDIP (16)     | 19.30 mm x 6.35 mm |
|              | SOP (16)      | 10.3 mm x 5.30 mm  |

(1) For all available packages, see the orderable addendum at the end of the datasheet.



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## 5 Revision History

### Changes from Revision L (March 2004) to Revision M

Page

|   |          |
|---|----------|
| • Removed Ordering Information table. ....  | <b>1</b> |
| • Added Handling Rating table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. .... | <b>1</b> |
| • Moved $T_{stg}$ to Handling Ratings table. ....   | <b>4</b> |

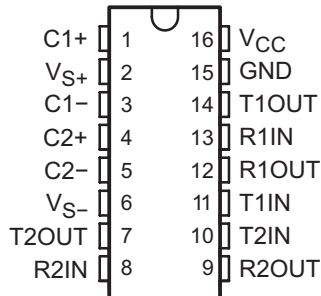
## 6 Pin Configuration and Functions

### Top View

MAX232 . . . D, DW, N, OR NS PACKAGE

MAX232I . . . D, DW, OR N PACKAGE

(TOP VIEW)



### Pin Functions

| PIN             |        | TYPE | DESCRIPTION  |
|-----------------|--------|------|--|
| NAME            | NO.    |      |  |
| C1+             | 1      | —    | Positive lead of C1 capacitor                          |
| VS+             | 2      | O    | Positive charge pump output for storage capacitor only |
| C1-             | 3      | —    | Negative lead of C1 capacitor                          |
| C2+             | 4      | —    | Positive lead of C2 capacitor                          |
| C2-             | 5      | —    | Negative lead of C2 capacitor                          |
| VS-             | 6      | O    | Negative charge pump output for storage capacitor only |
| T2OUT, T1OUT    | 7, 14  | O    | RS232 line data output (to remote RS232 system)        |
| R2IN, R1IN      | 8, 13  | I    | RS232 line data input (from remote RS232 system)       |
| R2OUT, R1OUT    | 9, 12  | O    | Logic data output (to UART)                            |
| T2IN, T1IN      | 10, 11 | I    | Logic data input (from UART)                           |
| GND             | 15     | —    | Ground   |
| V <sub>CC</sub> | 16     | —    | Supply Voltage, Connect to external 5V power supply    |

## 7 Specifications

### 7.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|                 |   |              | MIN                   | MAX                   | UNIT |
|-----------------|---|--------------|-----------------------|-----------------------|------|
| V <sub>CC</sub> | Input Supply voltage range <sup>(2)</sup> |              | -0.3                  | 6                     | V    |
| V <sub>S+</sub> | Positive output supply voltage range      |              | V <sub>CC</sub> - 0.3 | 15                    | V    |
| V <sub>S-</sub> | Negative output supply voltage range      |              | -0.3                  | -15                   | V    |
| V <sub>I</sub>  | Input voltage range                       | T1IN, T2IN   | -0.3                  | V <sub>CC</sub> + 0.3 | V    |
|                 |   | R1IN, R2IN   |                       | ±30                   |      |
| V <sub>O</sub>  | Output voltage range                      | T1OUT, T2OUT | V <sub>S-</sub> - 0.3 | V <sub>S+</sub> + 0.3 | V    |
|                 |   | R1OUT, R2OUT | -0.3                  | V <sub>CC</sub> + 0.3 |      |
|                 | Short-circuit duration                    | T1OUT, T2OUT | Unlimited             |                       |      |
| T <sub>J</sub>  | Operating virtual junction temperature    |              |                       | 150                   | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.

### 7.2 Handling Ratings

|                    |                           |  | MIN | MAX  | UNIT |
|--------------------|---------------------------|--|-----|------|------|
| T <sub>stg</sub>   | Storage temperature range |  | -65 | 150  | °C   |
| V <sub>(ESD)</sub> | Electrostatic discharge   | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>              | 0   | 2000 | V    |
|                    |                           | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> | 0   | 1000 |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

|                 |                                       |         | MIN | NOM | MAX | UNIT |
|-----------------|---------------------------------------|---------|-----|-----|-----|------|
| V <sub>CC</sub> | Supply voltage                        |         | 4.5 | 5   | 5.5 | V    |
| V <sub>IH</sub> | High-level input voltage (T1IN, T2IN) |         | 2   |     |     | V    |
| V <sub>IL</sub> | Low-level input voltage (T1IN, T2IN)  |         |     |     | 0.8 | V    |
| R1IN, R2IN      | Receiver input voltage                |         |     |     | ±30 | V    |
| T <sub>A</sub>  | Operating free-air temperature        | MAX232  | 0   |     | 70  | °C   |
|                 |                                       | MAX232I | -40 |     | 85  |      |

### 7.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> | MAX232xD                               | MAX232xDW | MAX232xN | MAX232xNS | UNIT |      |
|-------------------------------|--|-----------|----------|-----------|------|------|
|                               | SOIC                                   | SOIC wide | PDIP     | SOP       |      |      |
|                               | 16 PINS                                | 16 PINS   | 16 PINS  | 16 PINS   |      |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance | 73        | 57       | 67        | 64   | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report ([SPRA953](#)).

### 7.5 Electrical Characteristics — Device

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 6](#))

| PARAMETER       | TEST CONDITIONS <sup>(1)</sup> | MIN   | TYP <sup>(2)</sup> | MAX | UNIT |    |
|-----------------|--------------------------------|---|--------------------|-----|------|----|
| I <sub>CC</sub> | Supply current                 | V <sub>CC</sub> = 5.5V, all outputs open, T <sub>A</sub> = 25°C |                    | 8   | 10   | mA |

- (1) Test conditions are C1–C4 = 1 μF at V<sub>CC</sub> = 5 V ± 0.5 V
- (2) All typical values are at V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

## 7.6 Electrical Characteristics — Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                      |   | TEST CONDITIONS <sup>(1)</sup> |  | MIN | TYP <sup>(2)</sup> | MAX | UNIT |
|--------------------------------|---|--------------------------------|--|-----|--------------------|-----|------|
| V <sub>OH</sub>                | High-level output voltage               | T1OUT, T2OUT                   | R <sub>L</sub> = 3 kΩ to GND                                 | 5   | 7                  |     | V    |
| V <sub>OL</sub>                | Low-level output voltage <sup>(3)</sup> | T1OUT, T2OUT                   | R <sub>L</sub> = 3 kΩ to GND                                 |     | -7                 | -5  | V    |
| r <sub>O</sub>                 | Output resistance                       | T1OUT, T2OUT                   | V <sub>S+</sub> = V <sub>S-</sub> = 0, V <sub>O</sub> = ±2 V | 300 |                    |     | Ω    |
| I <sub>OS</sub> <sup>(4)</sup> | Short-circuit output current            | T1OUT, T2OUT                   | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0 V                |     | ±10                |     | mA   |
| I <sub>IS</sub>                | Short-circuit input current             | T1IN, T2IN                     | V <sub>I</sub> = 0   |     |                    | 200 | μA   |

(1) Test conditions are C1–C4 = 1 μF at V<sub>CC</sub> = 5 V ± 0.5 V

(2) All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

(3) The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.

(4) Not more than one output should be shorted at a time.

## 7.7 Electrical Characteristics — Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER        |   | TEST CONDITIONS <sup>(1)</sup> |  | MIN | TYP <sup>(2)</sup> | MAX | UNIT |
|------------------|---|--------------------------------|--|-----|--------------------|-----|------|
| V <sub>OH</sub>  | High-level output voltage                       | R1OUT, R2OUT                   | I <sub>OH</sub> = -1 mA                      | 3.5 |                    |     | V    |
| V <sub>OL</sub>  | Low-level output voltage <sup>(3)</sup>         | R1OUT, R2OUT                   | I <sub>OL</sub> = 3.2 mA                     |     |                    | 0.4 | V    |
| V <sub>IT+</sub> | Receiver positive-going input threshold voltage | R1IN, R2IN                     | V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C |     | 1.7                | 2.4 | V    |
| V <sub>IT-</sub> | Receiver negative-going input threshold voltage | R1IN, R2IN                     | V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C | 0.8 | 1.2                |     | V    |
| V <sub>hys</sub> | Input hysteresis voltage                        | R1IN, R2IN                     | V <sub>CC</sub> = 5 V                        | 0.2 | 0.5                | 1   | V    |
| r <sub>I</sub>   | Receiver input resistance                       | R1IN, R2IN                     | V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C | 3   | 5                  | 7   | kΩ   |

(1) Test conditions are C1–C4 = 1 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

(3) The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.

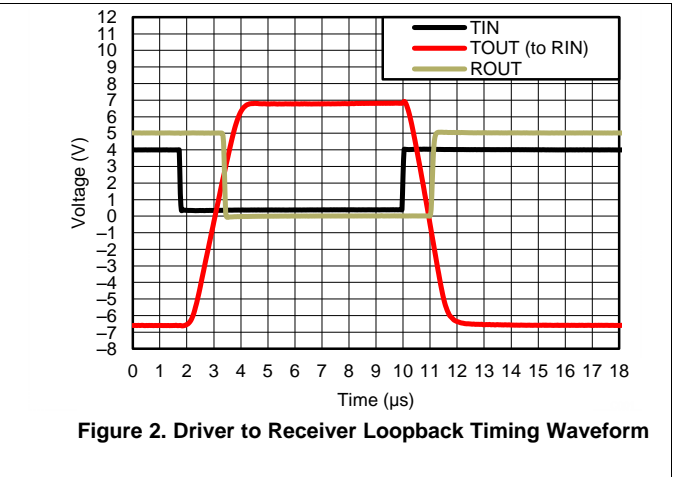
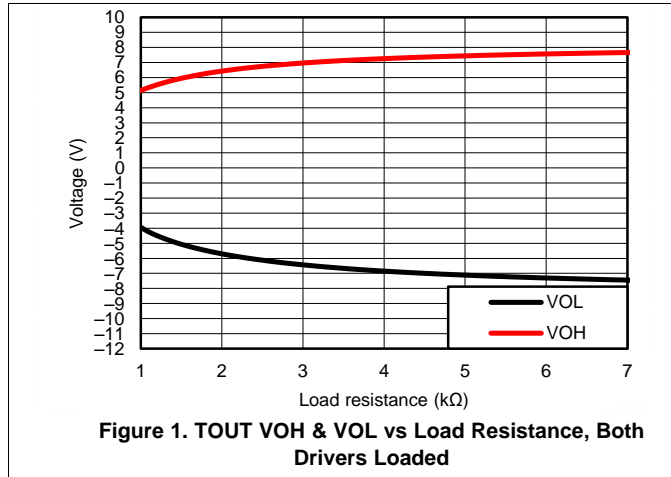
## 7.8 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

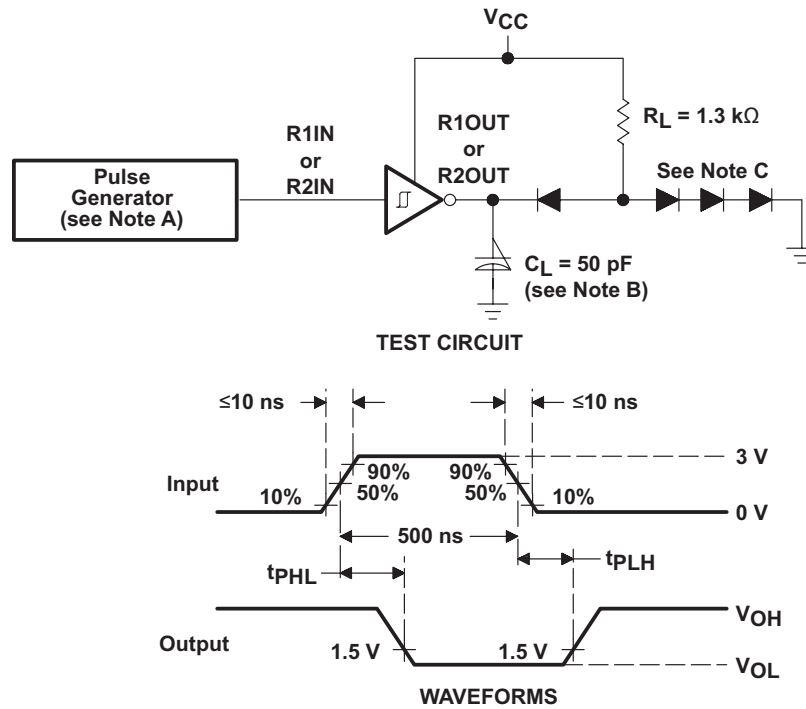
| PARAMETER          |  | TEST CONDITIONS <sup>(1)</sup>                  |  | MIN | TYP <sup>(1)</sup> | MAX | UNIT   |
|--------------------|--|---|--|-----|--------------------|-----|--------|
| SR                 | Driver slew rate   | RL = 3 kΩ to 7 kΩ, see <a href="#">Figure 4</a> |  |     |                    | 30  | V/μs   |
| SR(t)              | Driver transition region slew rate                         | see <a href="#">Figure 5</a>                    |  |     | 3                  |     | V/μs   |
|                    | Data rate  | One TOUT switching                              |  |     | 120                |     | kbit/s |
| t <sub>PLH</sub> ® | Receiver propagation delay time, low- to high-level output | TTL load, see <a href="#">Figure 3</a>          |  |     | 500                |     | ns     |
| t <sub>PHL</sub> ® | Receiver propagation delay time, high- to low-level output | TTL load, see <a href="#">Figure 3</a>          |  |     | 500                |     | ns     |

(1) Test conditions are C1–C4 = 1 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

## 7.9 Typical Characteristics

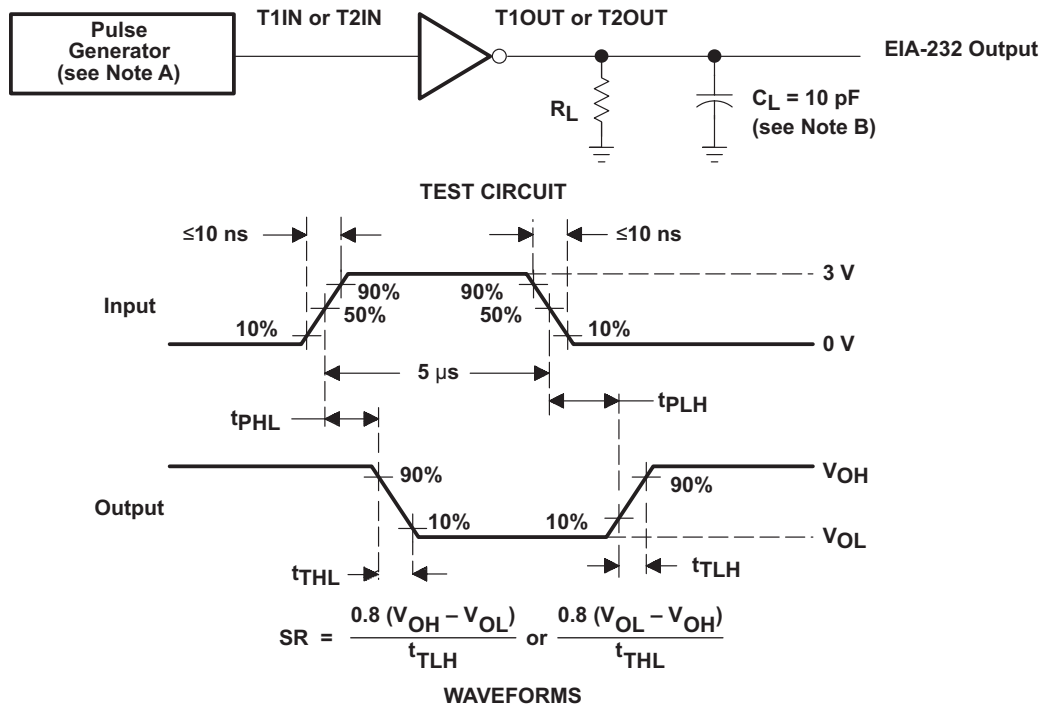


## 8 Parameter Measurement Information

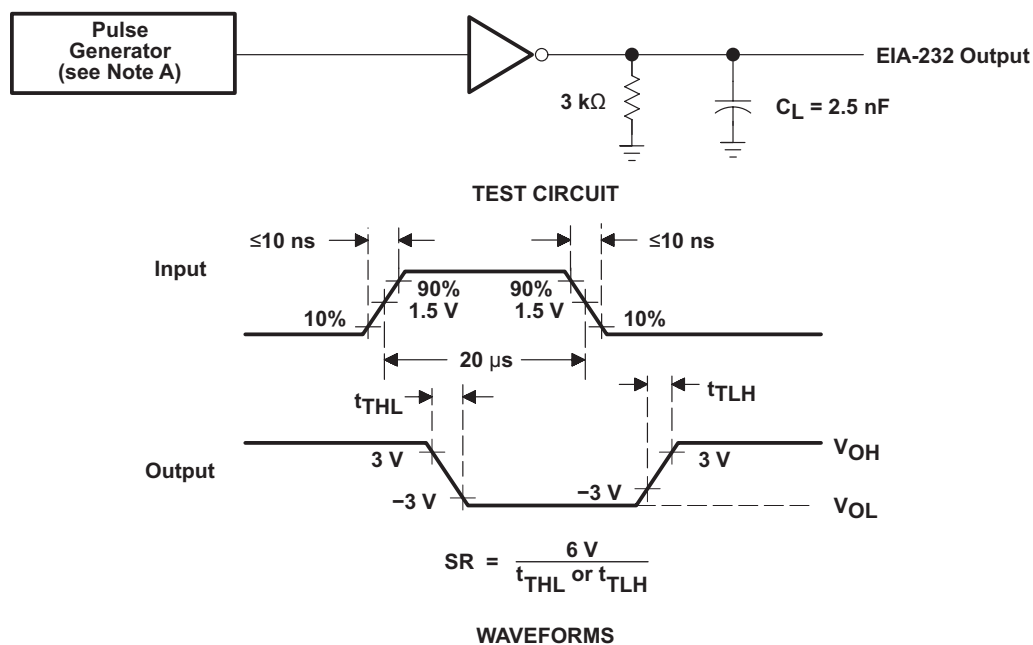


- A. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , duty cycle  $\leq 50\%$ .
- B.  $C_L$  includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.

**Figure 3. Receiver Test Circuit and Waveforms for  $t_{PHL}$  and  $t_{PLH}$  Measurements**

**Parameter Measurement Information (continued)**


- A. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , duty cycle  $\leq 50\%$ .
- B.  $C_L$  includes probe and jig capacitance.

**Figure 4. Driver Test Circuit and Waveforms for  $t_{PHL}$  and  $t_{PLH}$  Measurements (5- $\mu$ s Input)**


- A. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , duty cycle  $\leq 50\%$ .

**Figure 5. Test Circuit and Waveforms for  $t_{THL}$  and  $t_{TLH}$  Measurements (20- $\mu$ s Input)**

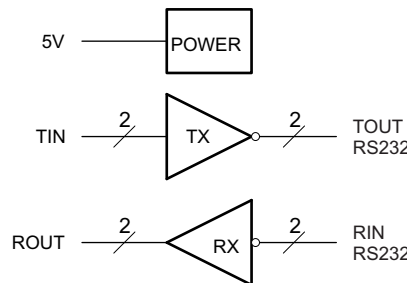


## 9 Detailed Description

### 9.1 Overview

The MAX232 device is a dual driver/receiver that includes a capacitive voltage generator using four capacitors to supply TIA/EIA-232-F voltage levels from a single 5-V supply. Each receiver converts TIA/EIA-232-F inputs to 5-V TTL/CMOS levels. These receivers have a typical threshold of 1.3 V, a typical hysteresis of 0.5 V, and can accept  $\pm 30$ -V inputs. Each driver converts TTL/CMOS input levels into TIA/EIA-232-F levels. The driver, receiver, and voltage-generator functions are available as cells in the Texas Instruments LinASIC™ library. Outputs are protected against shorts to ground.

### 9.2 Functional Block Diagram



### 9.3 Feature Description

#### 9.3.1 Power

The power block increases and inverts the 5V supply for the RS232 driver using a charge pump that requires four 1- $\mu$ F external capacitors.

#### 9.3.2 RS232 Driver

Two drivers interface standard logic level to RS232 levels. Internal pull up resistors on TIN inputs ensures a high input when the line is high impedance.

#### 9.3.3 RS232 Receiver

Two receivers interface RS232 levels to standard logic levels. An open input will result in a high output on ROUT.

### 9.4 Device Functional Modes

#### 9.4.1 $V_{CC}$ powered by 5V

The device will be in normal operation.

#### 9.4.2 $V_{CC}$ unpowered

When MAX232 is unpowered, it can be safely connected to an active remote RS232 device.

**Table 1. Function Table Each Driver<sup>(1)</sup>**

| INPUT<br>TIN | OUTPUT<br>TOUT |
|--------------|----------------|
| L            | H              |
| H            | L              |

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

**Table 2. Function Table Each Receiver<sup>(1)</sup>**

| INPUTS<br>RIN | OUTPUT<br>ROUT |
|---------------|----------------|
| L             | H              |
| H             | L              |
| Open          | H              |

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off),  
Open = disconnected input or connected driver off

## 10 Application and Implementation

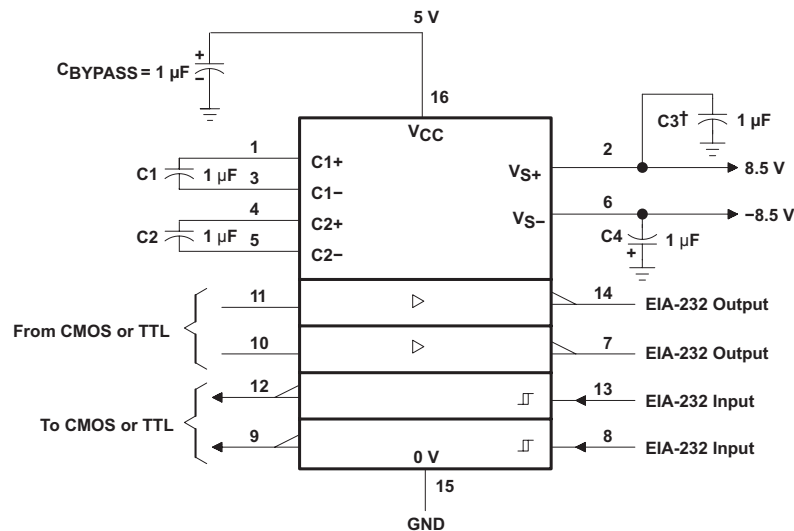
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

For proper operation add capacitors as shown in [Figure 6](#). Pins 9 through 12 connect to UART or general purpose logic lines. EIA-232 lines will connect to a connector or cable.

### 10.2 Typical Application



† C3 can be connected to V<sub>CC</sub> or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown. In addition to the 1-µF capacitors shown, the MAX202 can operate with 0.1-µF capacitors.

**Figure 6. Typical Operating Circuit**

#### 10.2.1 Design Requirements

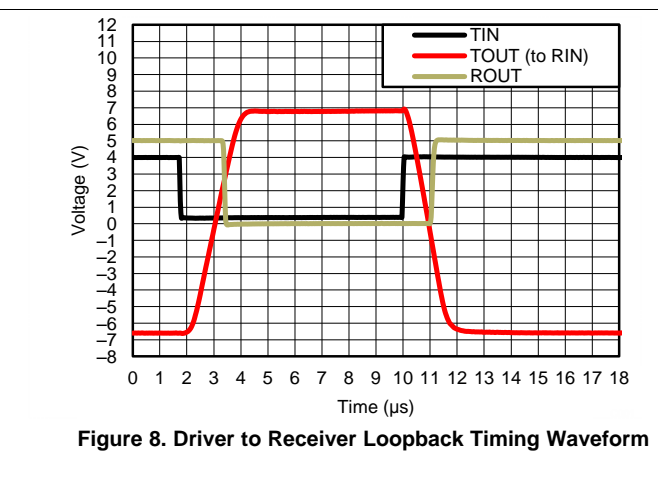
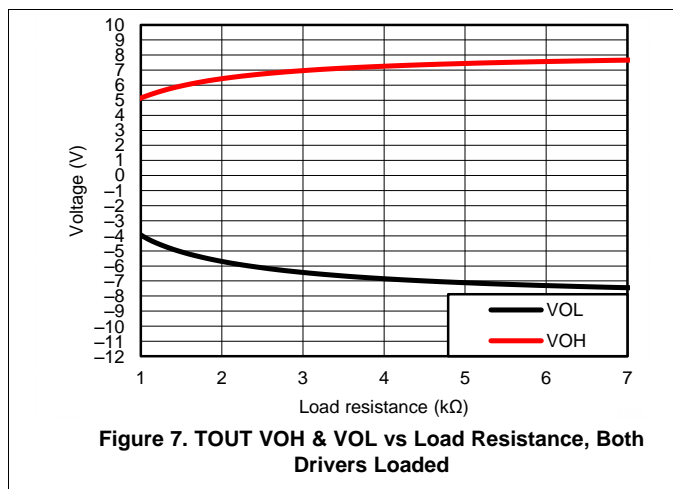
- V<sub>CC</sub> minimum is 4.5 V and maximum is 5.5 V.
- Maximum recommended bit rate is 120 kbps.

#### 10.2.2 Detailed Design Procedure

Use 1 µF tantalum or ceramic capacitors.

## Typical Application (continued)

### 10.2.3 Application Curves



## 11 Power Supply Recommendations

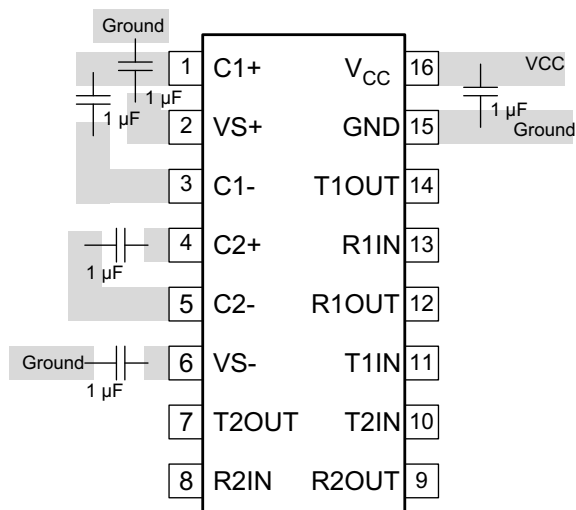
The  $V_{CC}$  voltage should be connected to the same power source used for logic device connected to TIN pins.  $V_{CC}$  should be between 4.5V and 5.5V.

## 12 Layout

### 12.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times.

### 12.2 Layout Example



## 13 Device and Documentation Support

### 13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

| PARTS   | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|---------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| MAX232  | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| MAX232I | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 13.2 Trademarks

All trademarks are the property of their respective owners.

### 13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| MAX232D          | ACTIVE        | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | MAX232                  | <a href="#">Samples</a> |
| MAX232DE4        | ACTIVE        | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | MAX232                  | <a href="#">Samples</a> |
| MAX232DG4        | ACTIVE        | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | MAX232                  | <a href="#">Samples</a> |
| MAX232DR         | ACTIVE        | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU   CU SN       | Level-1-260C-UNLIM   | 0 to 70      | MAX232                  | <a href="#">Samples</a> |
| MAX232DRE4       | ACTIVE        | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | MAX232                  | <a href="#">Samples</a> |
| MAX232DRG4       | ACTIVE        | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | MAX232                  | <a href="#">Samples</a> |
| MAX232DW         | ACTIVE        | SOIC         | DW              | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | MAX232                  | <a href="#">Samples</a> |
| MAX232DWE4       | ACTIVE        | SOIC         | DW              | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | MAX232                  | <a href="#">Samples</a> |
| MAX232DWG4       | ACTIVE        | SOIC         | DW              | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | MAX232                  | <a href="#">Samples</a> |
| MAX232DWR        | ACTIVE        | SOIC         | DW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | MAX232                  | <a href="#">Samples</a> |
| MAX232DWRE4      | ACTIVE        | SOIC         | DW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | MAX232                  | <a href="#">Samples</a> |
| MAX232DWRG4      | ACTIVE        | SOIC         | DW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | MAX232                  | <a href="#">Samples</a> |
| MAX232ID         | ACTIVE        | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | MAX232I                 | <a href="#">Samples</a> |
| MAX232IDG4       | ACTIVE        | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | MAX232I                 | <a href="#">Samples</a> |
| MAX232IDR        | ACTIVE        | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | MAX232I                 | <a href="#">Samples</a> |
| MAX232IDW        | ACTIVE        | SOIC         | DW              | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | MAX232I                 | <a href="#">Samples</a> |
| MAX232IDWG4      | ACTIVE        | SOIC         | DW              | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | MAX232I                 | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| MAX232IDWR       | ACTIVE        | SOIC         | DW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | MAX232I                 | <a href="#">Samples</a> |
| MAX232IDWRE4     | ACTIVE        | SOIC         | DW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | MAX232I                 | <a href="#">Samples</a> |
| MAX232IDWRG4     | ACTIVE        | SOIC         | DW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | MAX232I                 | <a href="#">Samples</a> |
| MAX232IN         | ACTIVE        | PDIP         | N               | 16   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU               | N / A for Pkg Type   | -40 to 85    | MAX232IN                | <a href="#">Samples</a> |
| MAX232INE4       | ACTIVE        | PDIP         | N               | 16   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU               | N / A for Pkg Type   | -40 to 85    | MAX232IN                | <a href="#">Samples</a> |
| MAX232N          | ACTIVE        | PDIP         | N               | 16   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU               | N / A for Pkg Type   | 0 to 70      | MAX232N                 | <a href="#">Samples</a> |
| MAX232NE4        | ACTIVE        | PDIP         | N               | 16   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU               | N / A for Pkg Type   | 0 to 70      | MAX232N                 | <a href="#">Samples</a> |
| MAX232NSR        | ACTIVE        | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | MAX232                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MAX232DR     | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| MAX232DR     | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| MAX232DRG4   | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| MAX232DRG4   | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| MAX232DWR    | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| MAX232DWRG4  | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| MAX232IDR    | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| MAX232IDWR   | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| MAX232IDWRG4 | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MAX232DR     | SOIC         | D               | 16   | 2500 | 333.2       | 345.9      | 28.6        |
| MAX232DR     | SOIC         | D               | 16   | 2500 | 367.0       | 367.0      | 38.0        |
| MAX232DRG4   | SOIC         | D               | 16   | 2500 | 333.2       | 345.9      | 28.6        |
| MAX232DRG4   | SOIC         | D               | 16   | 2500 | 367.0       | 367.0      | 38.0        |
| MAX232DWR    | SOIC         | DW              | 16   | 2000 | 367.0       | 367.0      | 38.0        |
| MAX232DWRG4  | SOIC         | DW              | 16   | 2000 | 367.0       | 367.0      | 38.0        |
| MAX232IDR    | SOIC         | D               | 16   | 2500 | 333.2       | 345.9      | 28.6        |
| MAX232IDWR   | SOIC         | DW              | 16   | 2000 | 367.0       | 367.0      | 38.0        |
| MAX232IDWRG4 | SOIC         | DW              | 16   | 2000 | 367.0       | 367.0      | 38.0        |

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN





- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



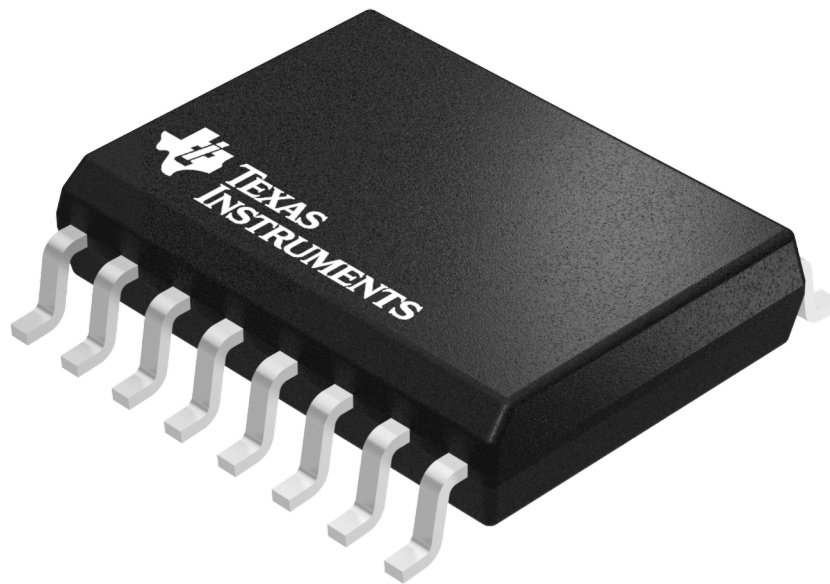
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## GENERIC PACKAGE VIEW

DW 16

**SOIC - 2.65 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

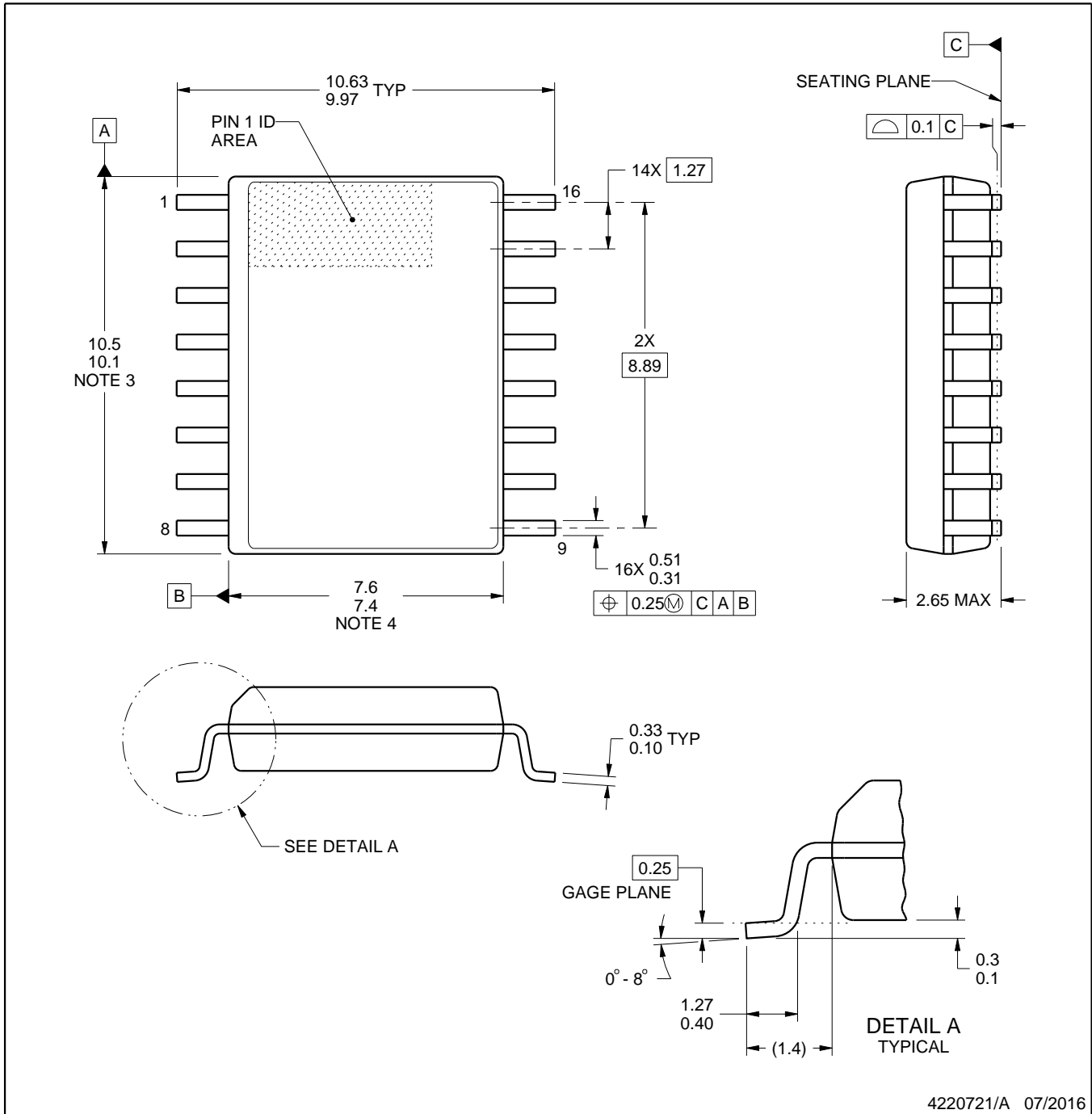
4040000-2/H



# DW0016A

# PACKAGE OUTLINE SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

### NOTES:

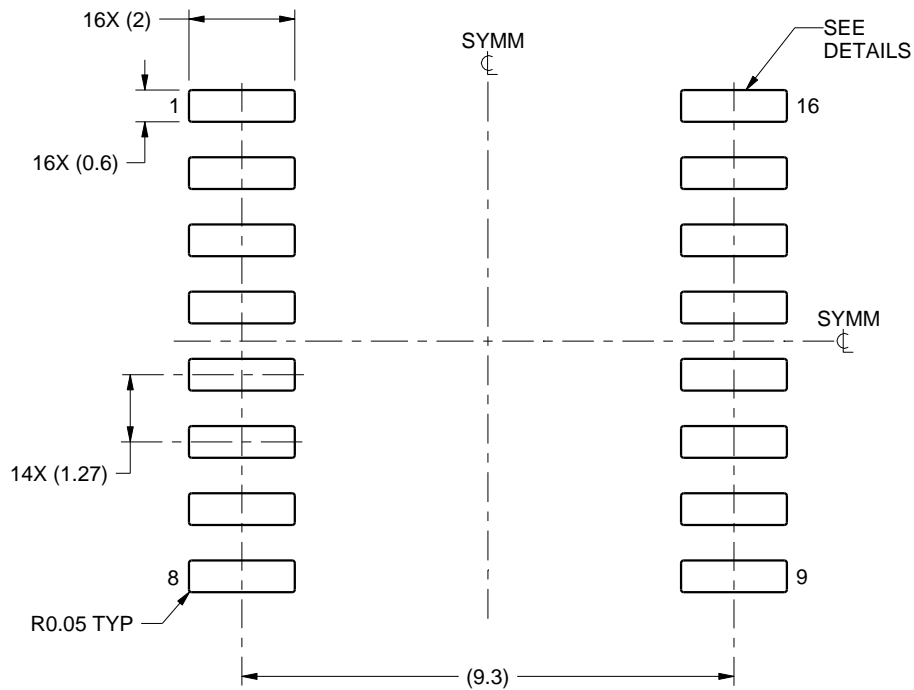
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

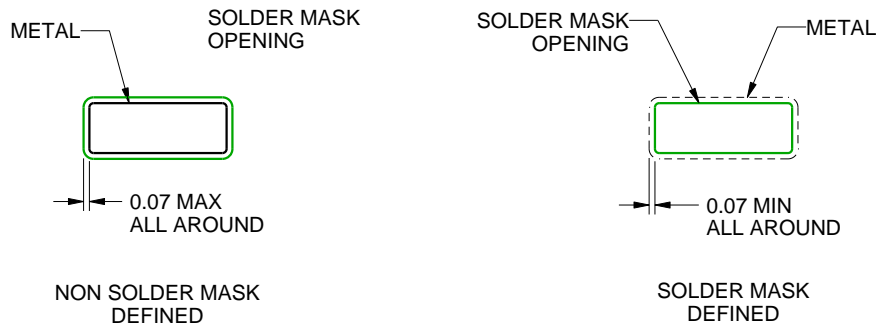
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

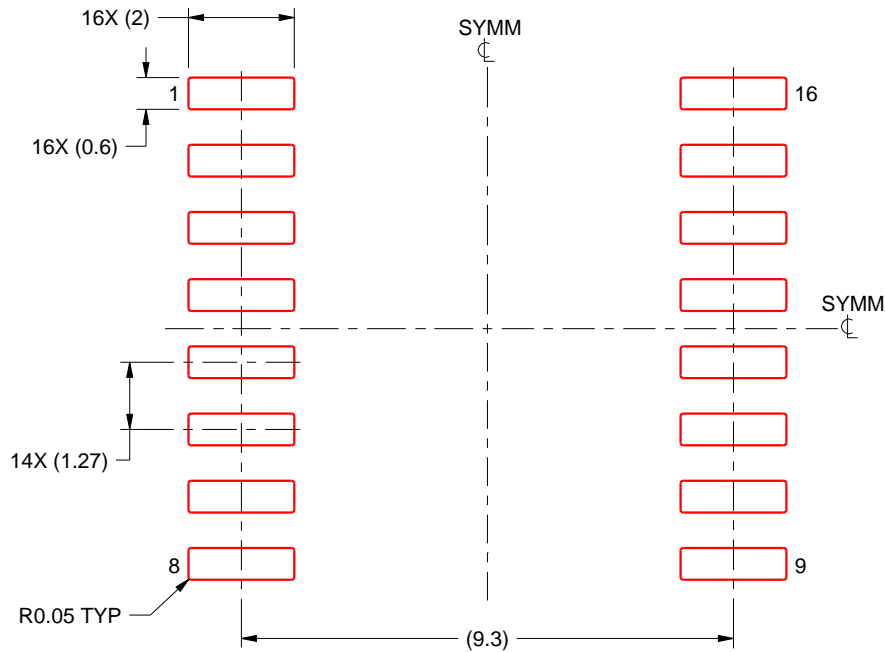


# EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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