# SYNAPTICAD

*Tools for the Thinking Mind*

**Timing Diagram Software, Verilog Simulator, Verilog Compiler, & Testbench Creation**




**Translate between Vhdl and Verilog**
V2V: do-it-yourself translation tools
Full-service VHDL & Verilog translation: we do it for you

**Simulate and debug VHDL and Verilog designs**
VeriLogger Extreme: high-performance Verilog 2001 simulator
BugHunter Pro: graphical debugger for all HDL simulators
Gigawave Viewer: VCD/SPICE waveform viewer
Gates-on-the-Fly: netlist analyzer

**Create and Navigate Verilog and VHDL Code**
EASE: state diagram and block diagram editor
HDL Companion: explore and create VHDL and Verilog designs
IO Checker: verify hundreds of pins between FPGA and PCB

**View and export waveforms to:**

Agilent test equipment, Tektronix test equipment,
Analog and digital simulators

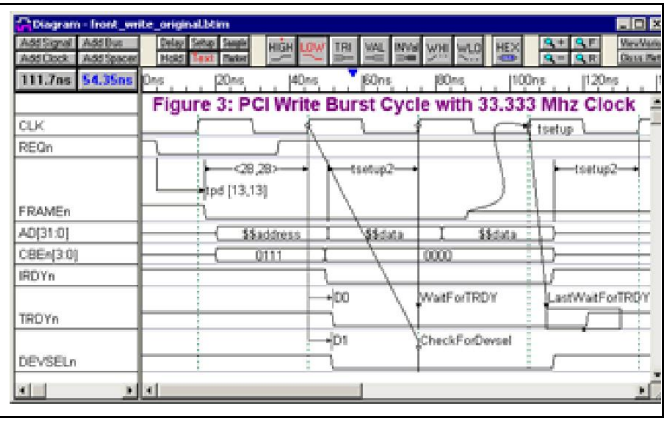
**Draw and Analyze Timing Diagrams**
DataSheet Pro: professional data sheet editor
WaveFormer Pro: timing diagram editor + waveform translator
Timing Diagrammer Pro: timing diagram editor

**Latest News**
SynaptiCAD's WaveFormer supports Agilent & Tektronix equipment and Hyperlynx
Timing Diagram Editors Simplify FPGA Synthesis
VHDL/Verilog Converters upgraded for Verilog 2005

WaveFormer Lite Generates Mixed Signal Test Benches for all FPGA design flows
VeriLogger supports encrypted models from Actel, Altera, and Xilinx
Timing Diagram Editors offer Editable Analog Equations
SynaptiCAD's 64-Bit Verilog Simulator is 30% Faster

**Graphically generate VHDL, Verilog, & SPICE test benches**

WaveFormer Pro for stimulus-only test benches
WaveFormer Pro with reactive test bench generation
TestBencher Pro creates transaction-based test benches
SPICE test bench stimulus (analog and digital)





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## SynaptiCAD Products

Founded by electrical engineers that were looking for ways to make tools that helped their fellow engineers, SynaptiCAD aims to help engineers create perfect designs. Since 1992, we have strived to become a company that creates "tools for the thinking mind". This drives all of the interfaces of our tools.

- **VeriLogger Extreme and BugHunter Pro**
  Created to help you simulate and debug your Verilog and VHDL designs, VeriLogger Pro and BugHunter Pro will help any engineer verify their design. Our tools are proven to reduce simulation debug time, and our unique timing diagram interface makes unit level testing a breeze.
- **Timing Diagrammer Pro, WaveFormer Pro, and DataSheet Pro**
  Need a timing diagram editor that will help you analyze timing, create professional documentation, and generate Verilog and VHDL test benches? Then pick from one of our three timing diagram editors for the feature set that meets your needs.
- **TestBencher Pro**
  Having trouble visualizing complicated verification models? Try TestBencher Pro! You can graphically model bus transactions and then apply them dynamically based on on-going simulation results.

Contact our team to learn more about our time-saving products.