Chitlesh GOORAH

Design & Verification Club Bristol 2010

[Free Electronic Lab]

(formerly Fedora Electronic Lab)

An opensource Design and Simulation platform
for Micro-Electronics

A one-stop linux distribution for hardware design

Marketing means for opensource EDA developers (Networking)

From SPEC, Model, Frontend Design, Backend,
Development boards to embedded software.

Electronic Designers Problems

Approx. 6 month design development cycle

Tackling Design Complexity

Lower Power, Lower Cost and Smaller Space

Semiconductor Industry's neck squeezed in 2008

Management (digital/analog) IP Portfolio

OVERVIEW : FEL'S SOLUTIONS TO THE DESIGN CENTER

Providing EDA solutions for the real world requires a clear overview on the targetted users.

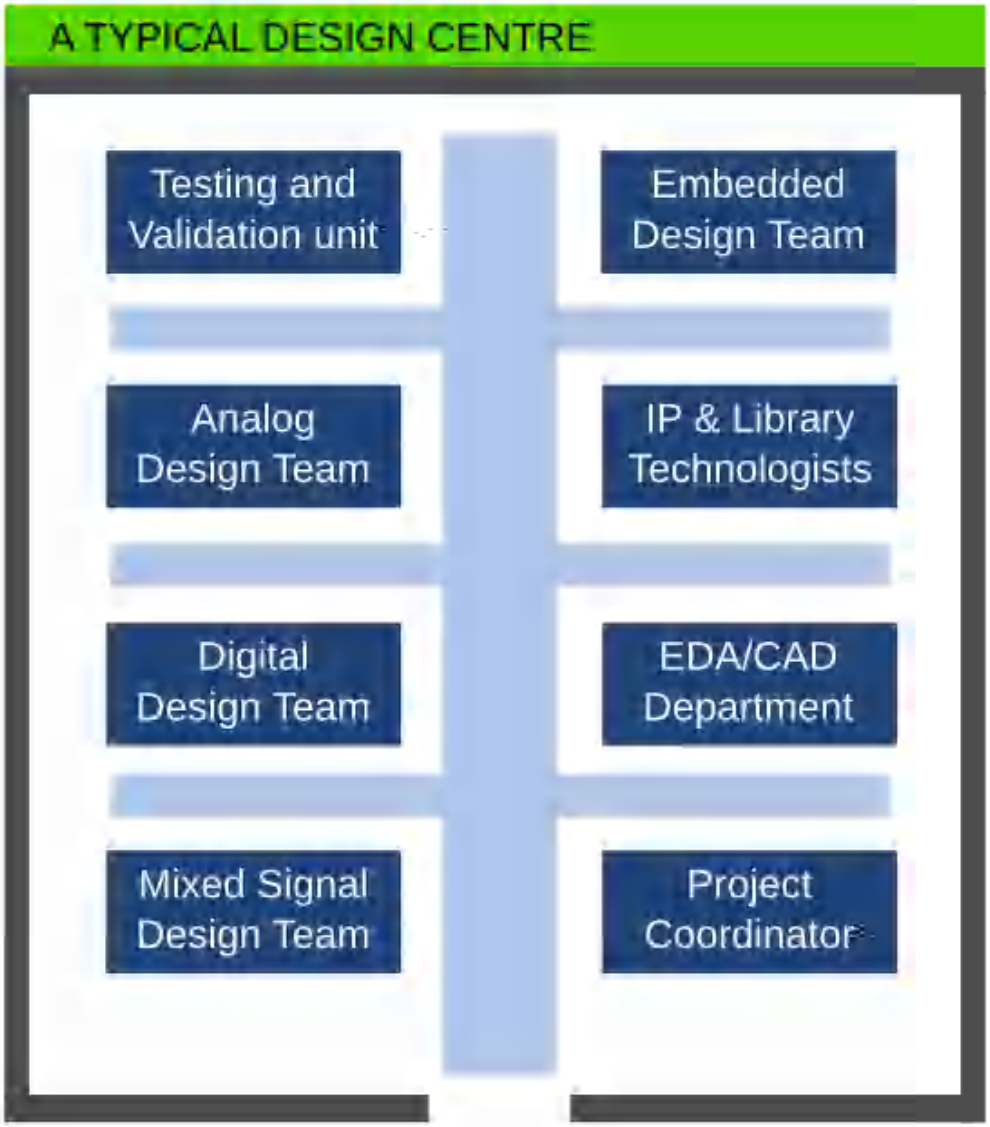
Free Electronic Lab strives to fulfill all the needs of each stage of the design flow .

FEL's Applications

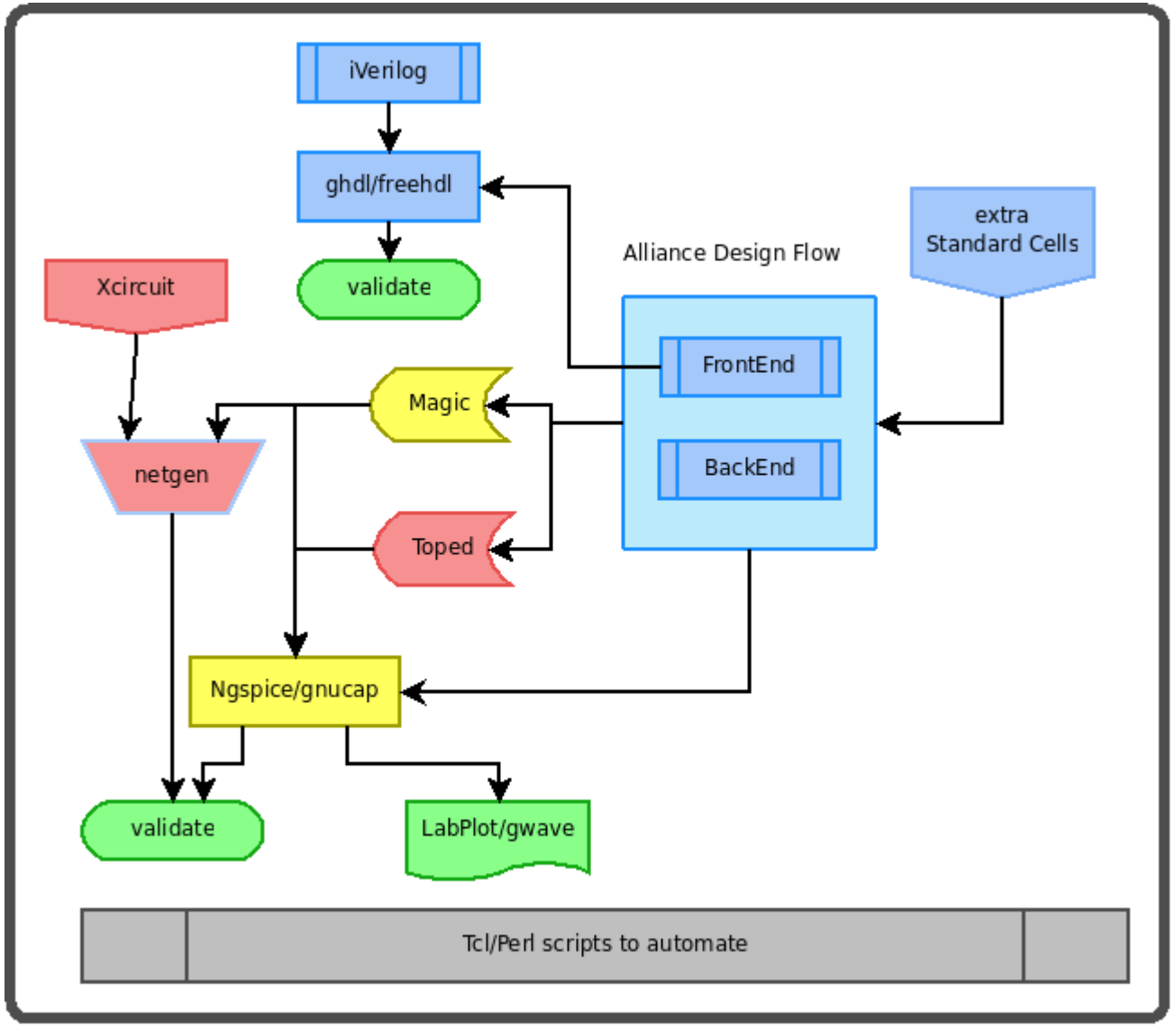
Free Electronic Lab

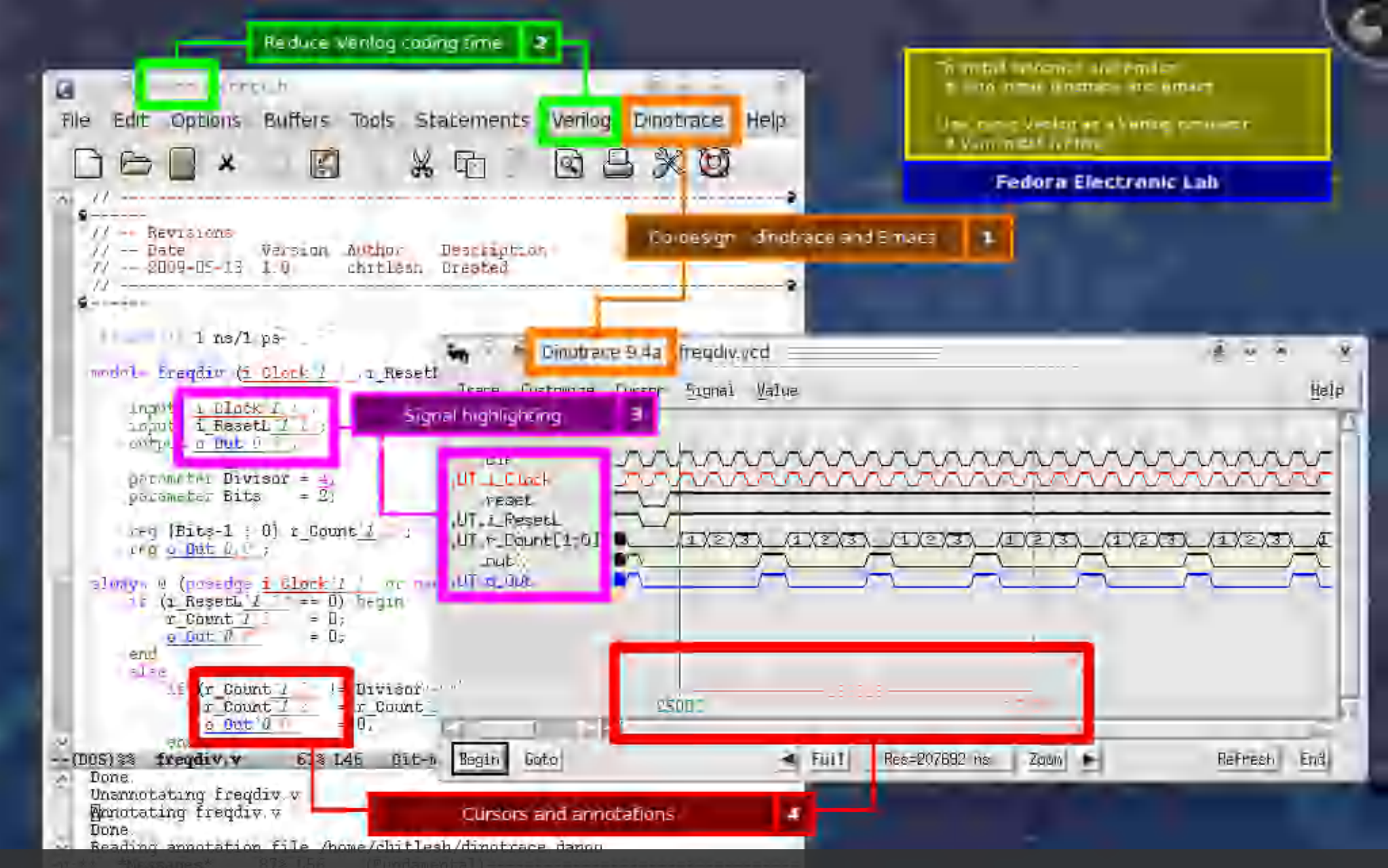
Free Electronic Lab improves hardware design experience with opensource software.

http://chitlesh.fedorapeople.org/FEL



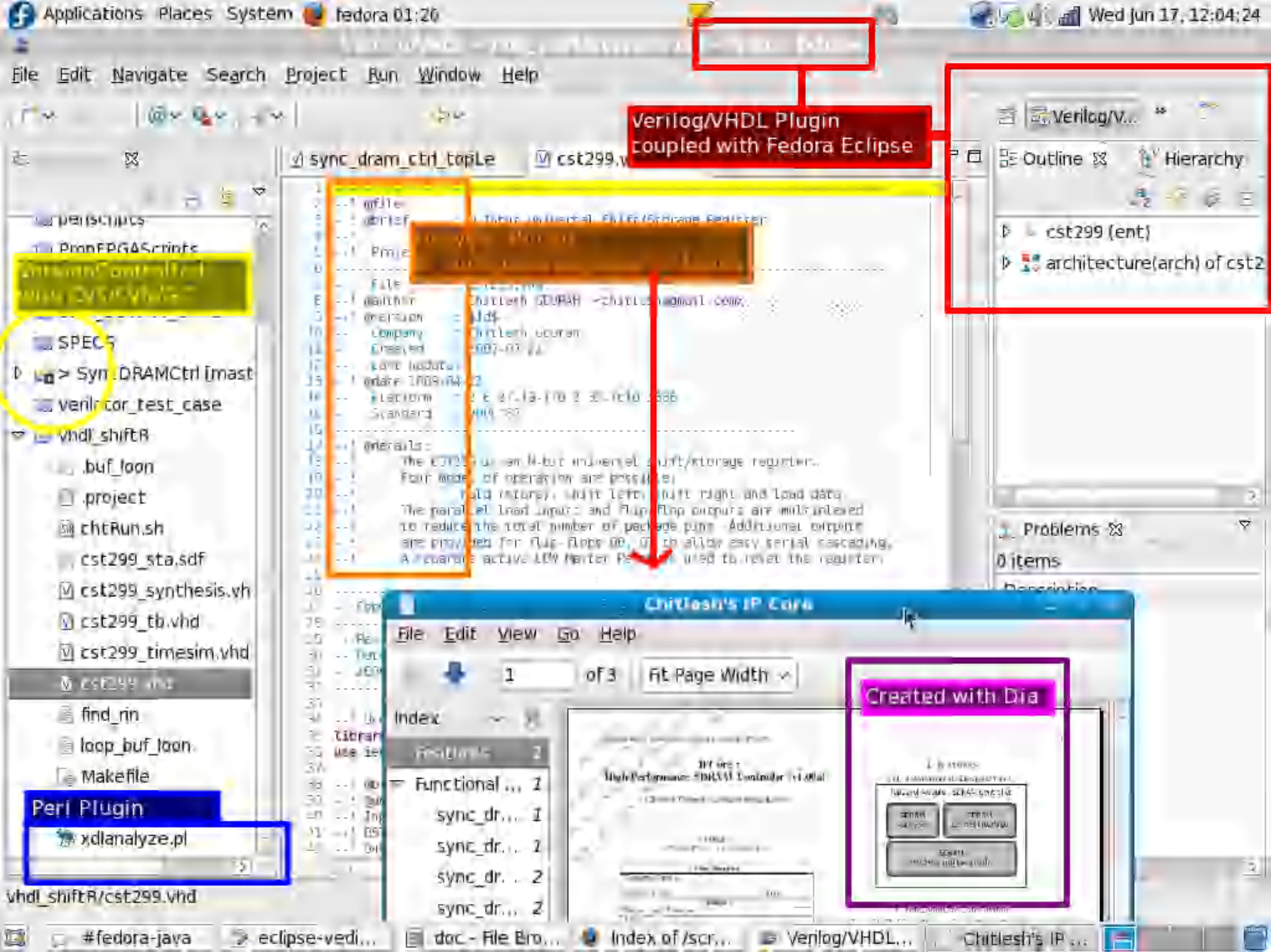
A basic Design Flow

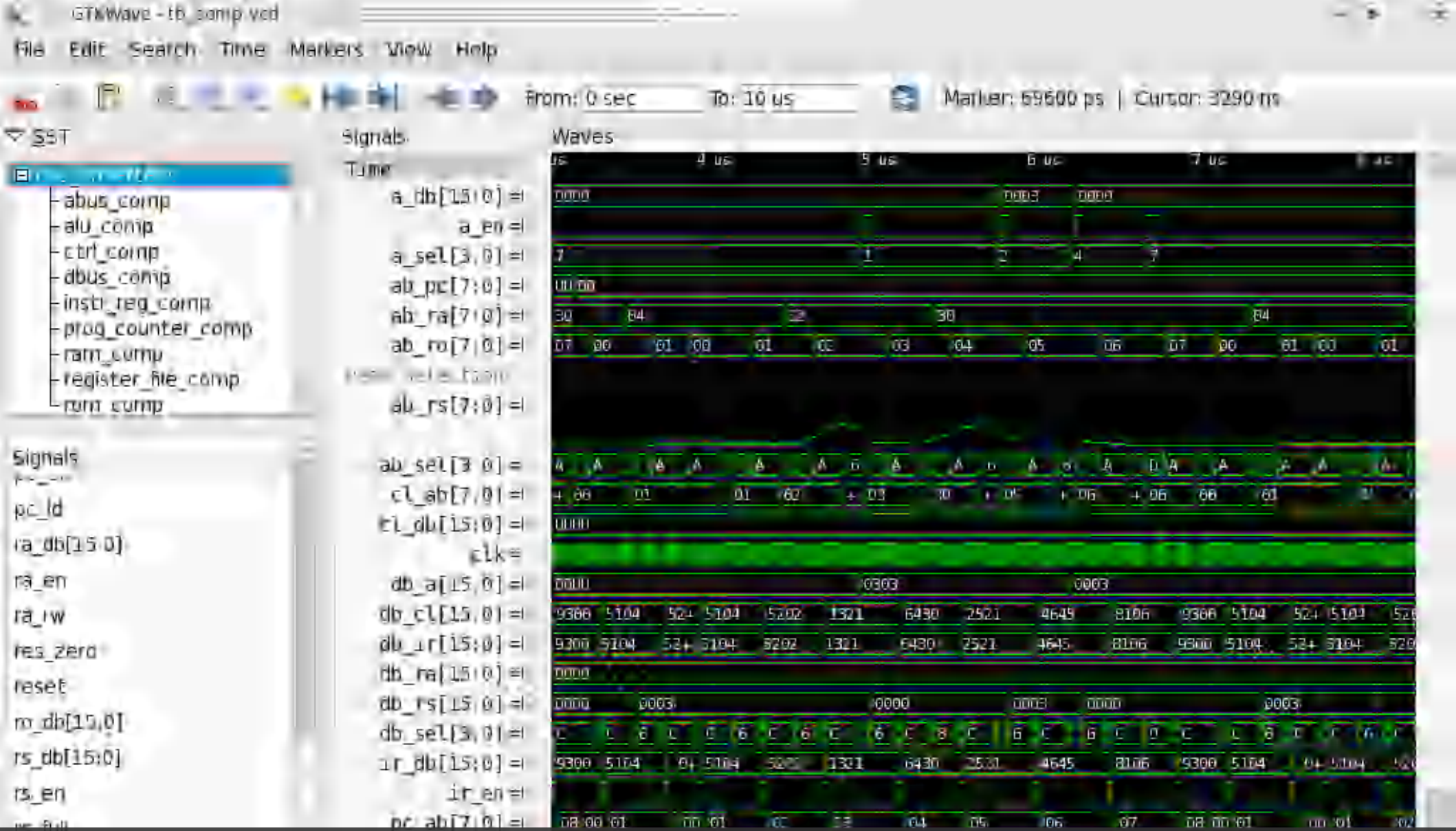




TIP: Use verilator to lint your verilog files.

Most of the Veripool tools are available under FEL.
They are in sync with Wilson Snyder's releases.


Applications Places System
fedora 01:26
Wed Jun 17, 12:04:24
File Edit Navigate Search Project Run Window Help
Verilog/VHDL Plugin
coupled with Fedora Eclipse
Verilog/V...
Outline
Hierarchy
cst299 (ent)
architecture(arch) of cst2
sync_dram_ctrl_topLe
cst299.v
SPEC5
> Syn DRAMCtrl [mast
verilator_test_case
vhdl_shiftR
.buf_loop
.project
chtRun.sh
cst299_sta.sdf
cst299_synthesis.vh
cst299_tb.vhd
cst299_timesim.vhd
find_rin
loop_buf_loop
Makefile
Perl Plugin
xdlanalyze.pl
Problems
0 items
Description
Chitlesh's IP Core
File Edit View Go Help
1
of 3
Fit Page Width
Index
Functional ... 1
sync_dr... 1
sync_dr... 1
sync_dr... 2
sync_dr... 2
Created with Dia
vhdl_shiftR/cst299.vhd
#fedora-java
eclipse-vedi...
doc - File Bro...
Index of /scr...
Verilog/VHDL...
Chitlesh's IP ...



GTKWave

Don't forget its TCL backend

Widely used together with SystemC

Tools

Standard Cell libraries

xooi21 standard cell family

2-I/P exclusive NOR gate with 2-OR input

NEXT | PREV | UP

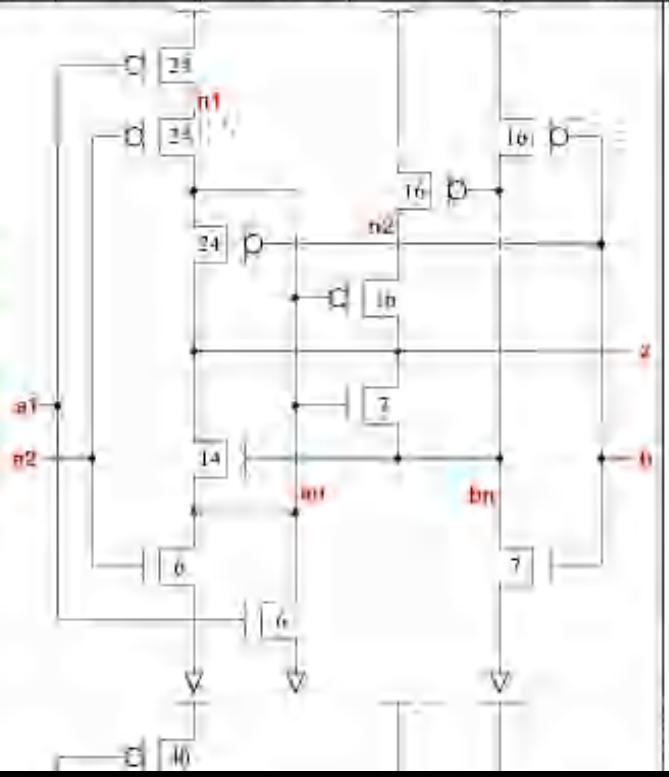
3 XNOR gates with OR gate input designed for minimum transistor count and hence smallest size. The OR gate is made by changing the inverter on the a input of a 2-XNOR gate into a 2-NOR gate. The Prop and Ramp delays below are the average of the inverting and non-inverting delays. The Synopsys Liberty format .LIB file has the correct delays for each case.

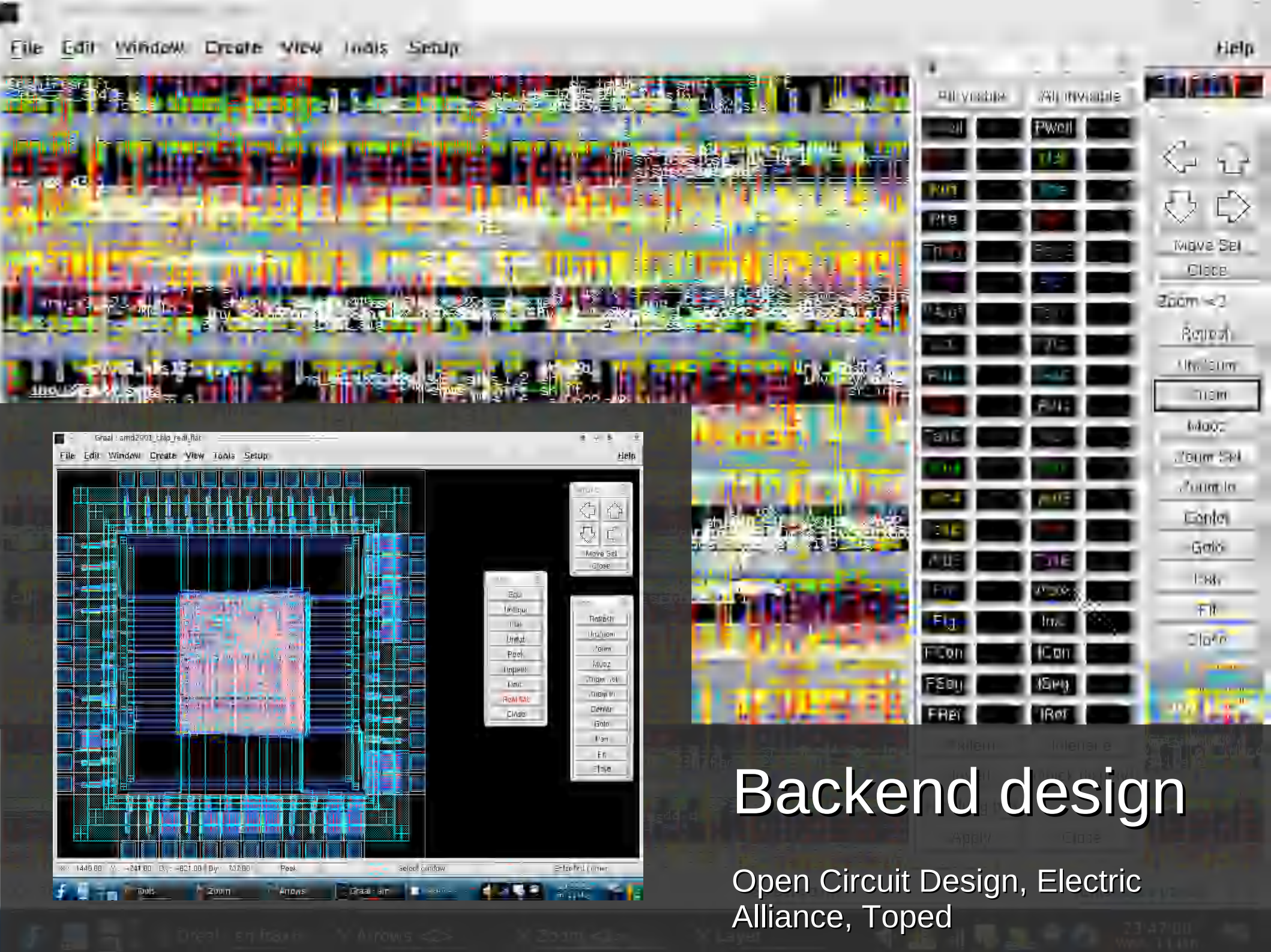
z = ((a1+a2)*b)'

	cell width			power		Generic 0.13um typical timing (ps & ps/fF), on a2.				
				leakage	dynamic	tR=PropR+RampR*Load(fF), tF=PropF+RampF*Load(fF)				
vsclib013	gates	lambda	0.13um	nW	nW/MHz	PinCap	PropR	RampR	PropF	RampF
xooi21v0x05	3.0	72	3,96	0,87	19.7	3.7f	104	6,34	105	4,76
xooi21v0x1	4.0	96	5,28	1,52	29.6	6.0f	94	3,76	94	2,52
xooi21v0x2	6.7	160	8,80	2.73	56.8	11.2f	32	1,96	33	1,27

xooi21v0x05

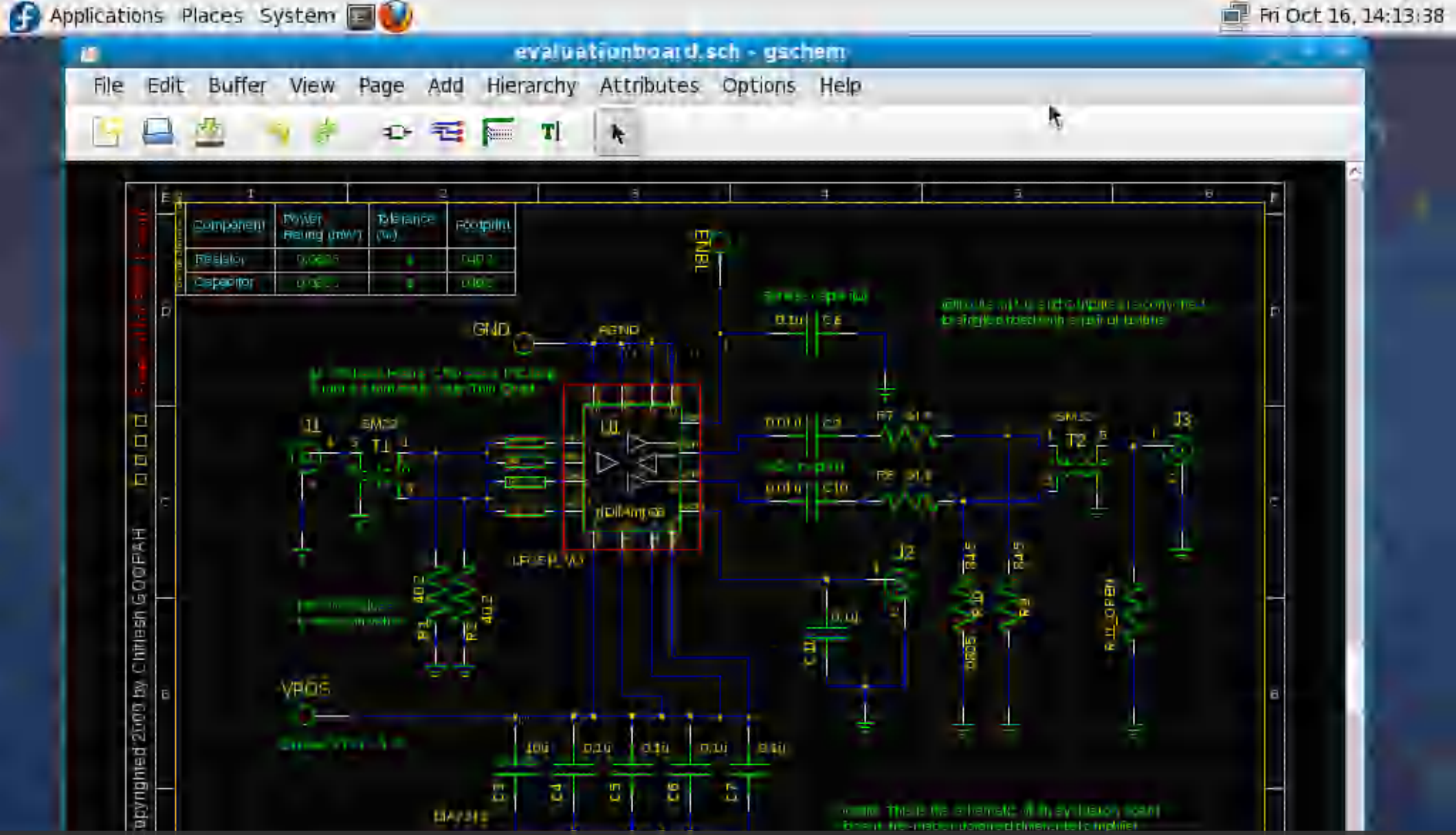
	Effort	
	FO4	Log
a1	2.35	1.97
	3.22	
a2	2.21	1.95
	3.13	
b	2.41	3.08
	2.74	





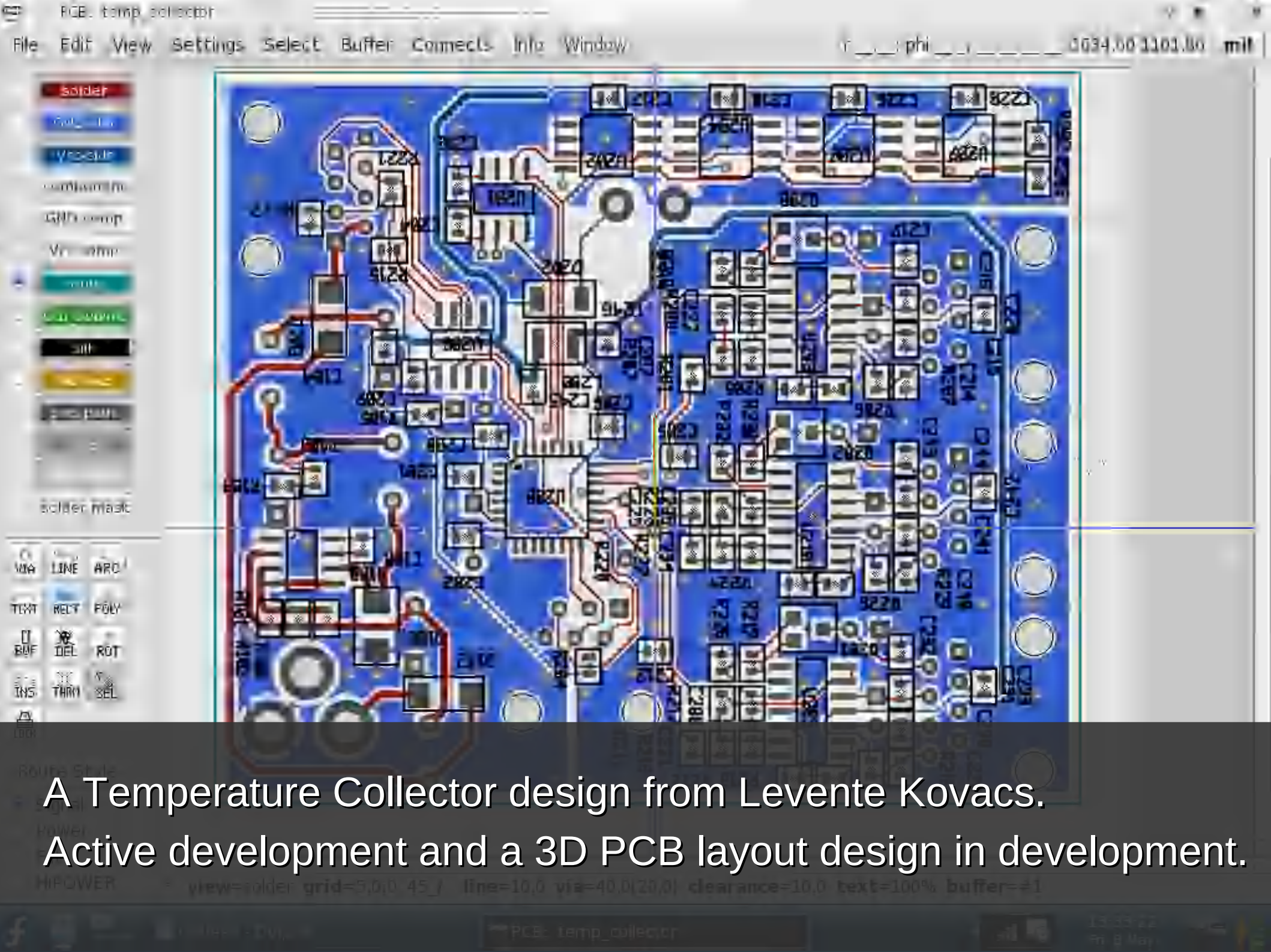
Backend design

Open Circuit Design, Electric
Alliance, Toped



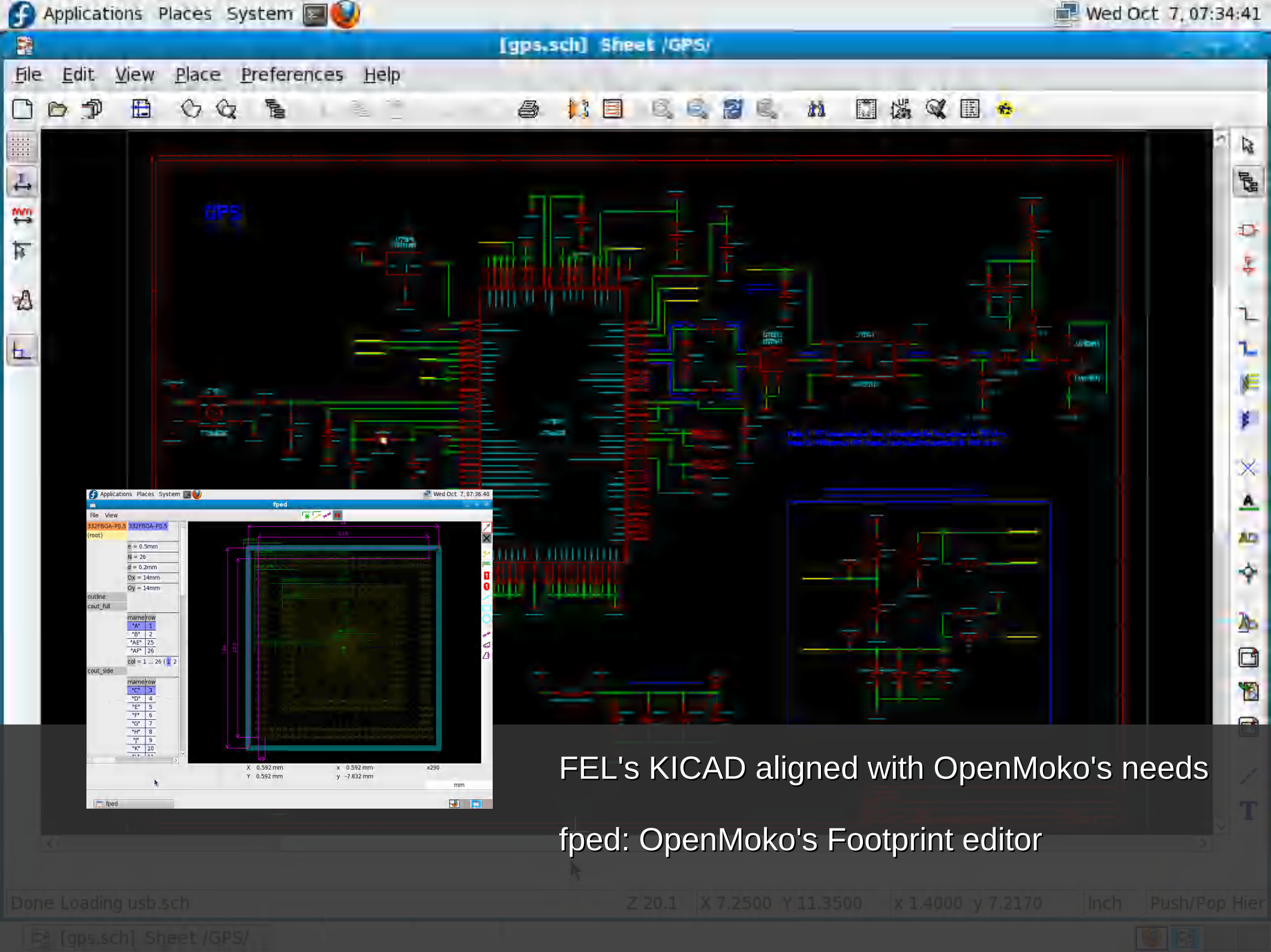
gEDA/gaf

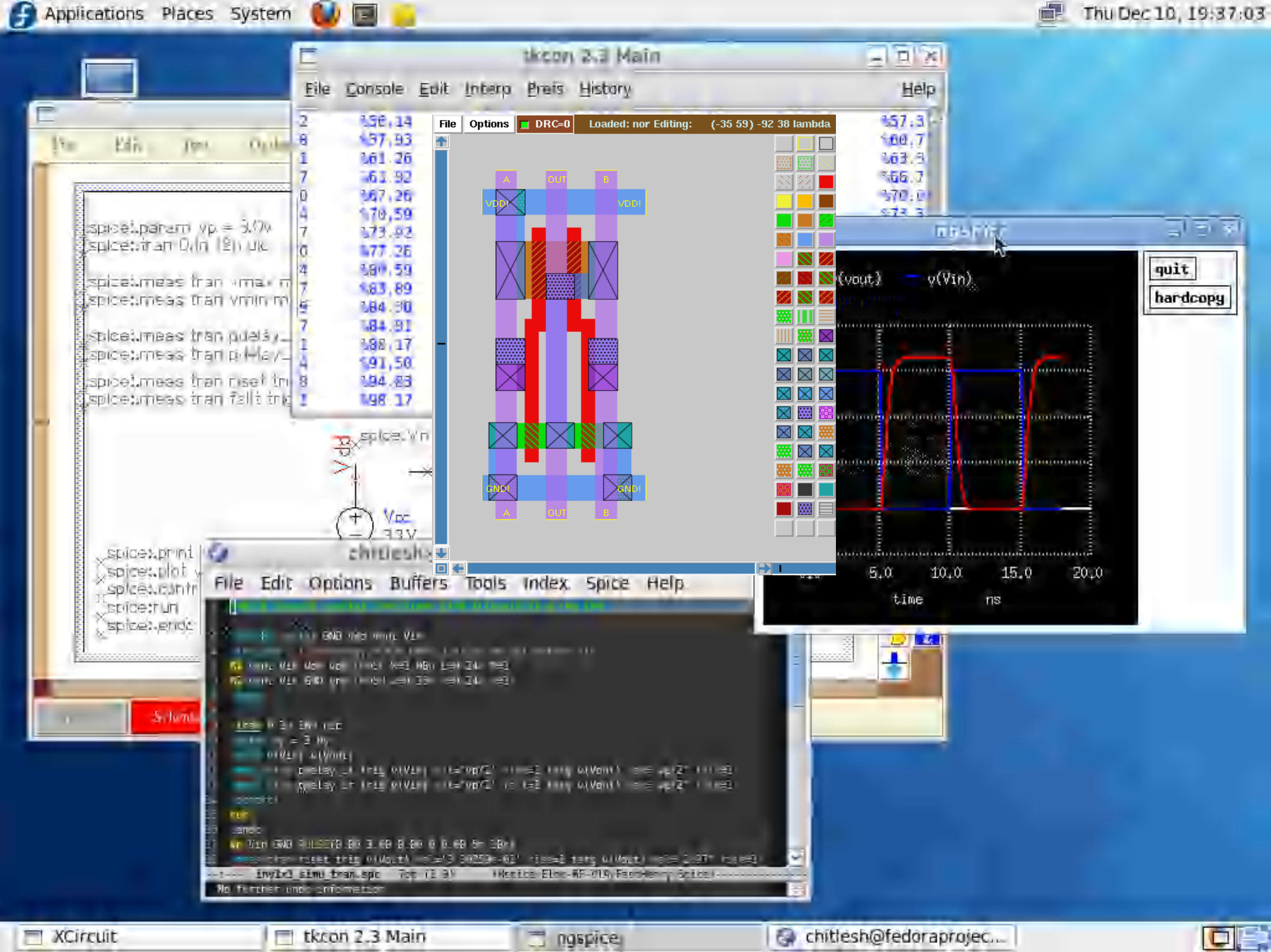
Well known and famous.
A very good example of opensource EDA tool.

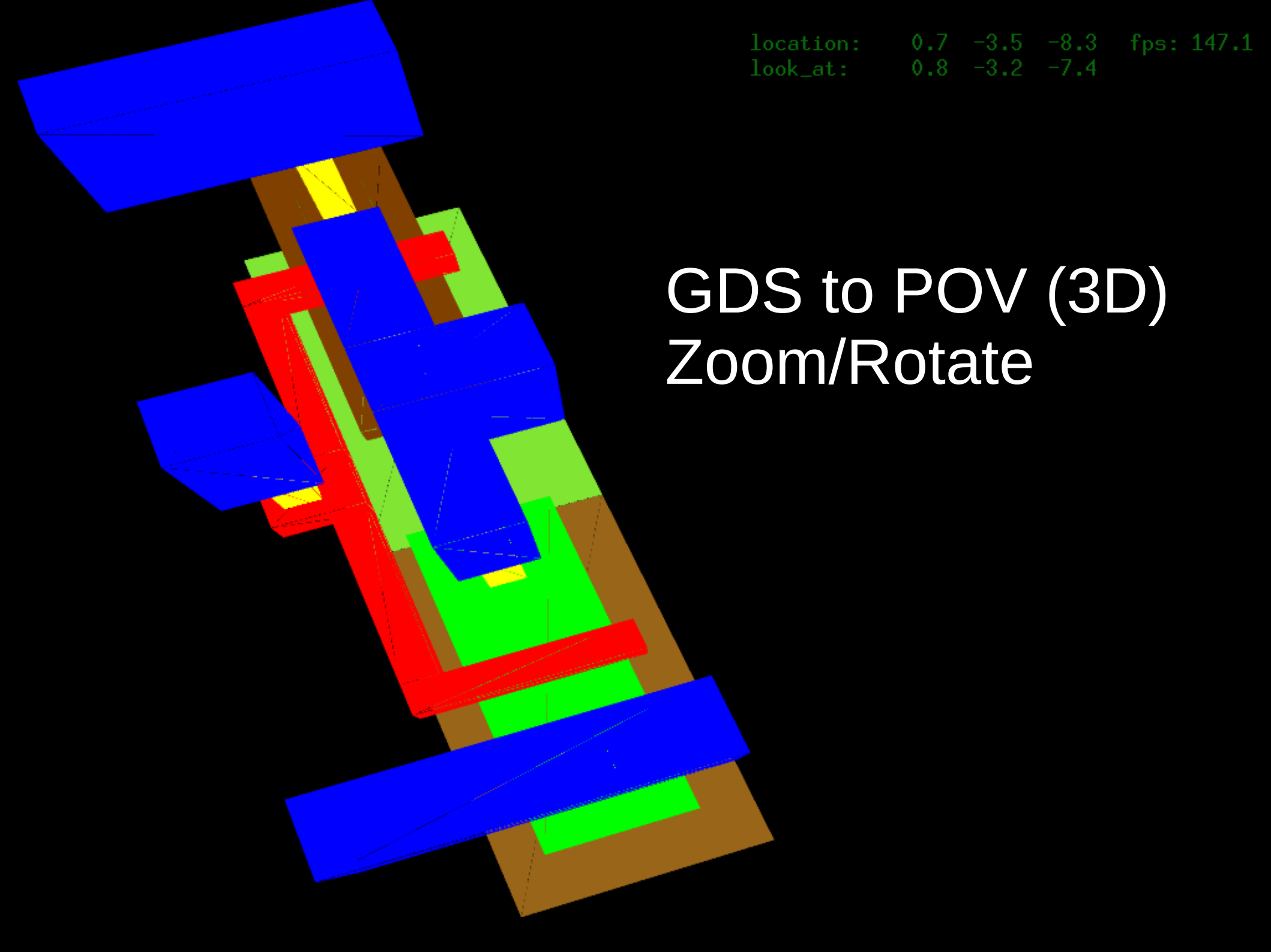


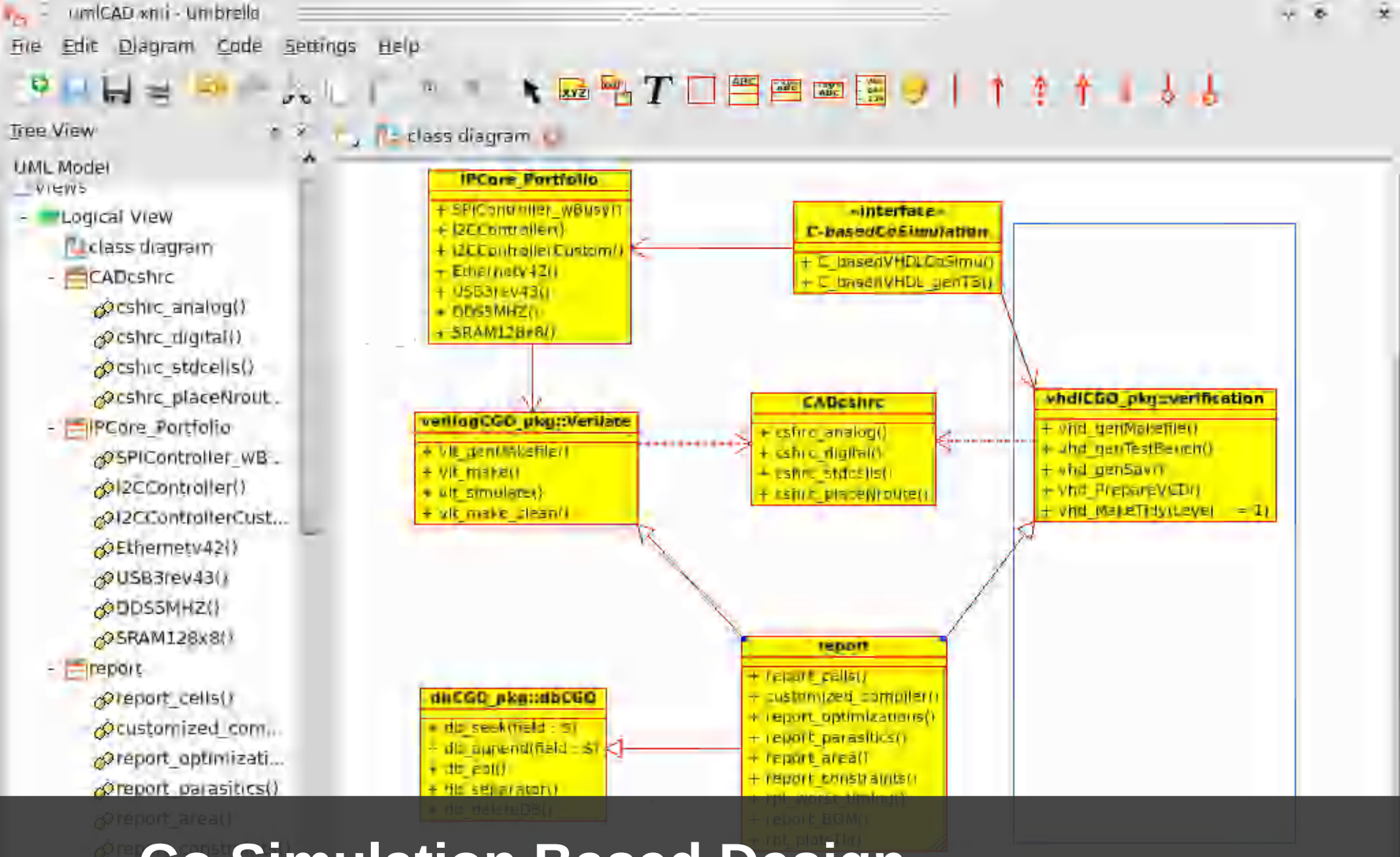
A Temperature Collector design from Levente Kovacs.

Active development and a 3D PCB layout design in development.


Applications Places System
Wed Oct 7, 07:34:41
[gps.sch] Sheet /GPS/
File Edit View Place Preferences Help
GPS
fped
FEL's KICAD aligned with OpenMoko's needs
fped: OpenMoko's Footprint editor
Done Loading usb.sch
[gps.sch] Sheet /GPS/


Applications Places System
Thu Dec 10, 19:37:03
tkcon 2.3 Main
File Console Edit Interp Preis History Help
File Options DRC=0 Loaded: nor Editing: (-35 59) -92 38 lambda
A OUT B
VDD! VDD!
GND! GND!
A OUT B
quit
hardcopy
v(vout) v(Vin)
5.0 10.0 15.0 20.0
time ns
chitlesh
File Edit Options Buffers Tools Index Spice Help
spice:param vp = 3.0v
spice:tran 0.1n 10n uic
spice:meas tran vmax m
spice:meas tran vmin m
spice:meas tran pdelay_
spice:meas tran plhay_
spice:meas tran rise1 tri
spice:meas tran fall1 trig
spice:print
spice:plot
spice:control
spice:run
spice:endc
Vpc
3.3V
XCircuit
tkcon 2.3 Main
ngspice
chitlesh@fedoraprojec...


location: 0.7 -3.5 -8.3 fps: 147.1
look_at: 0.8 -3.2 -7.4
GDS to POV (3D)
Zoom/Rotate



Co Simulation Based Design

UML to Perl, TCL or C++ exports.
TIP: Heaven, when coupled with Truss & Teal tools.

OVERVIEW : A FREE HIGH END HARDWARE DESIGN PLATFORM

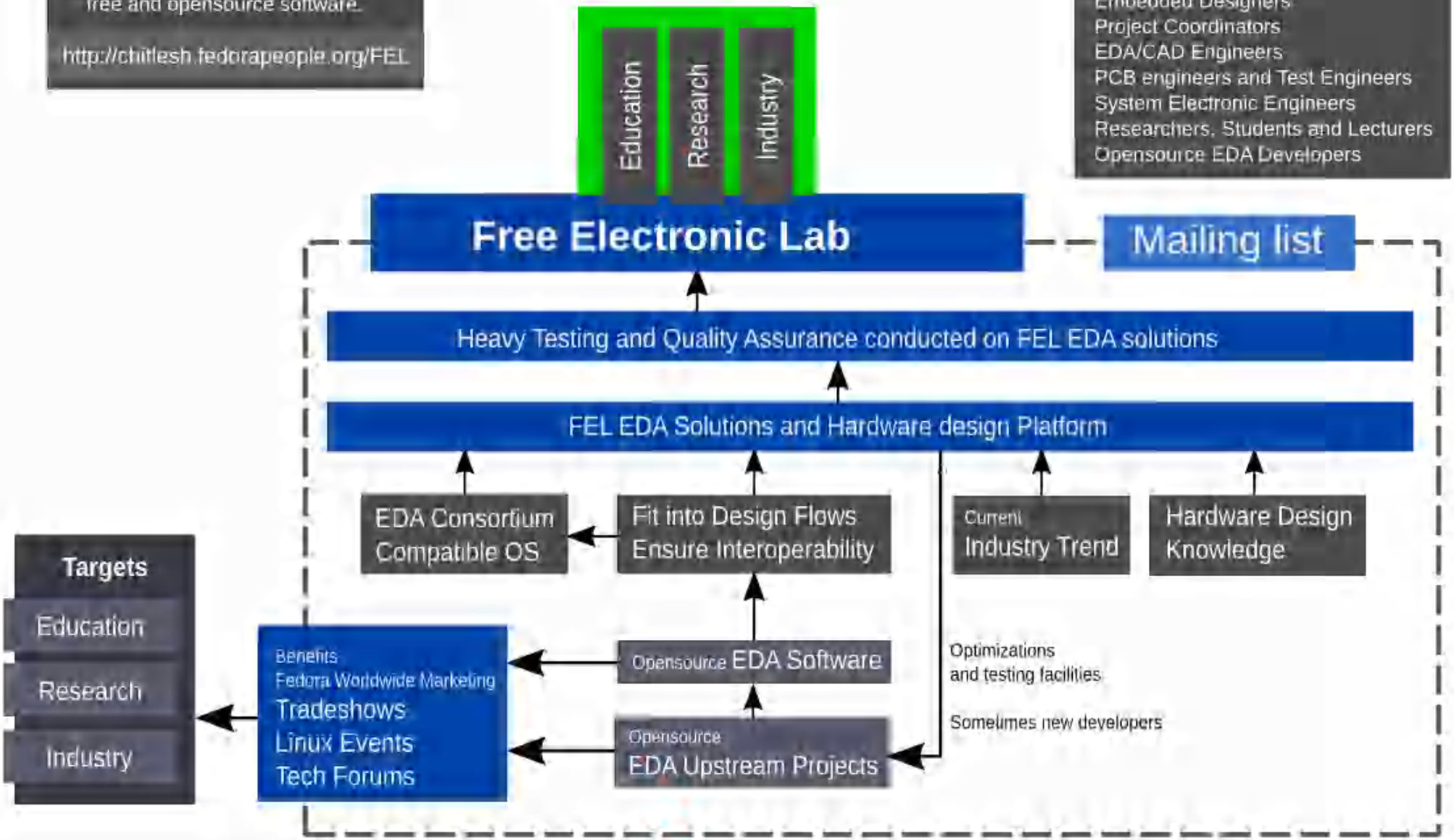
Free Electronic Lab

Free Electronic Lab improves hardware design experience with free and opensource software.

http://chitlesh.fedorapeople.org/FEL

Benefits

Analog/Digital/Mixed Designers
Verification solutions
Embedded Designers
Project Coordinators
EDA/CAD Engineers
PCB engineers and Test Engineers
System Electronic Engineers
Researchers, Students and Lecturers
Opensource EDA Developers



Simple Installation

Trial:

Fedora Electronic Lab LiveDVD

Production Environment:

On Fedora > 12 or upcoming RHEL / CentOS 6

```
# yum groupinstall 'Electronic Lab'
```

Who are using FEL ?

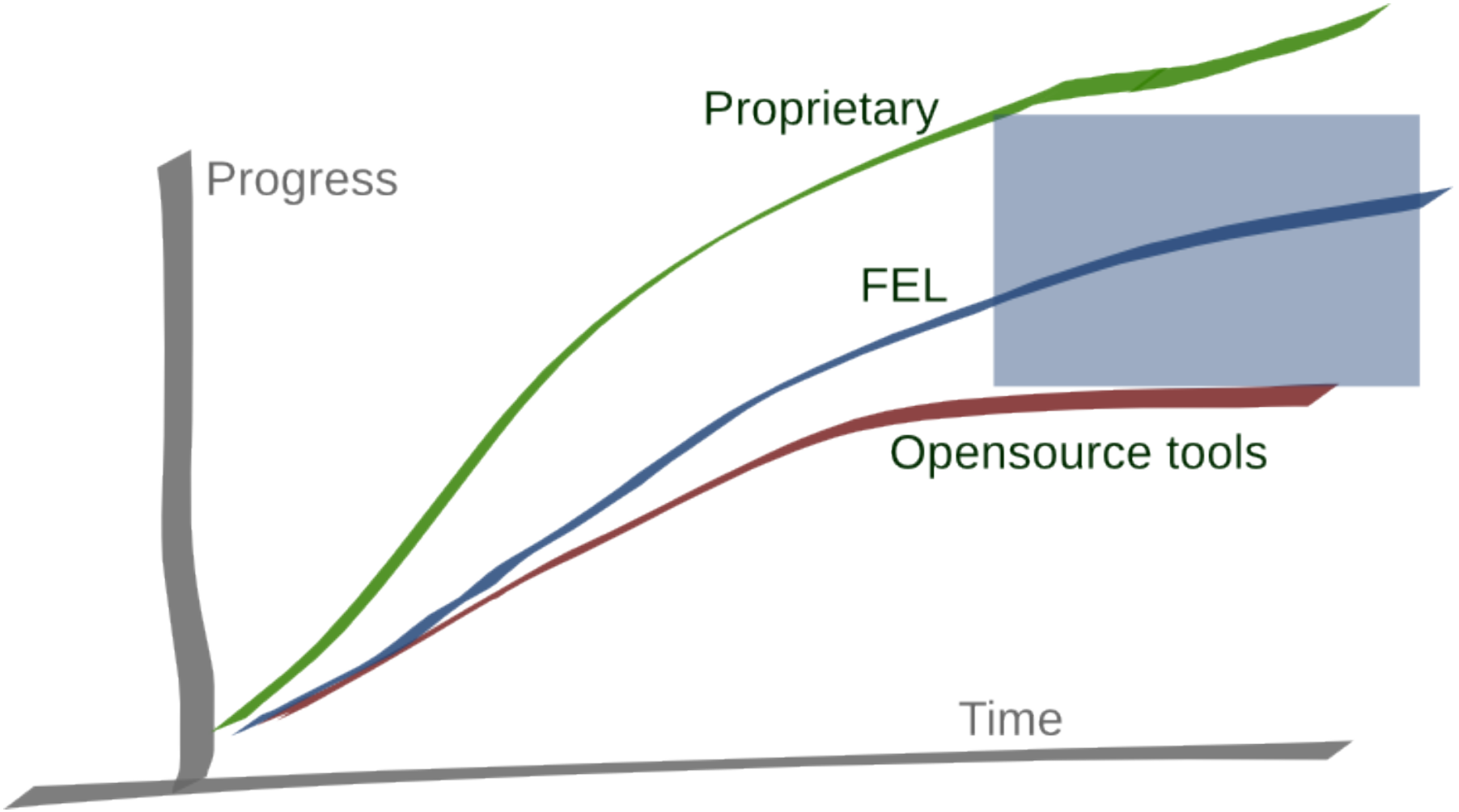
Universities around the world
- US, UK, France, India, Mexico, Brazil, Italy

Small companies & consulting companies

Linux For You magazine
Published twice (Jan 08, Jan 09)

Basic opensource EDA tools
Sun Microsystems, IBM, ST Microelectronics, Analog Devices, On Semi conductors

FEL User and Developer benefits



Free Electronic Lab 6.0 ?

Satisfy User “ME”

Strengthening the Backbone

Ensuring Interchangeability

FrontEnd design experience

Port to the Entreprise Class OS

Step into the opensource IP env

Questions & Answers

Thank you,

The Free Electronic Lab team

http://spins.fedoraproject.org/fel/
electronic-lab@lists.fedoraproject.org