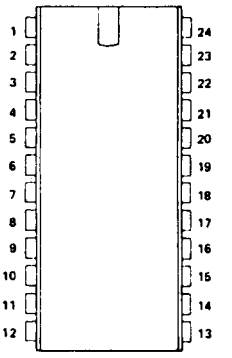
EXPANDABLE 12-INPUT, 6-OUTPUT, 32-TERM, SEQUENTIAL FIELD-PROGRAMMABLE LOGIC ARRAYS

- Field Programmable (Ti:W fuses)
- 12 Input Variables
- 6 Output Functions
- 32 Product Terms
- 4-Bit State Register ('LS333 & 'LS335 only)
- 6-Bit Output Register ('LS333 & 'LS335 only)
- Output Polarity Select ('LS334 & 'LS336 only)
- Choice of 3-State ('LS333 & 'LS334) or Open-Collector ('LS335 & 'LS336) Outputs
- Choice of Sequential ('LS333 & 'LS335) or Combinatorial ('LS334 & 'LS336) Logic

24-PIN CERAMIC AND PLASTIC DUAL IN-LINE PACKAGES (TOP VIEW)



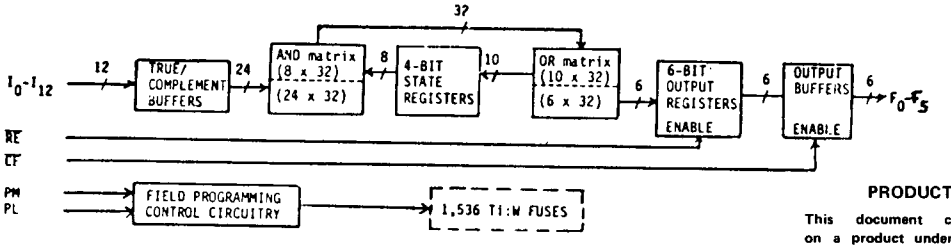
description

These low power Schottky 12-input, 6-output, 32-term logic arrays can be field programmed to provide summations of the 32 product terms onto the six output lines. They feature an option which permits the FPLA outputs to be automatically enabled by a true product term, or, to dedicate during programming, input (L/$\overline{OE}$) to serve as an output enable ($\overline{OE}$). Either option makes the FPLA expandable with respect to product terms.

For every product term, 12 input variables can be programmed as high or low. The 'LS333 and 'LS335 FPLAs contain four J-K flip-flops in the feedback path between the OR and AND matrices. These sequential FPLAs are ideally suited for state machine problems. The 'LS334 and 'LS336 FPLAs are purely combinatorial logic blocks.

Each of these FPLAs contain a 32 by 32 AND matrix and a 16 by 32 OR matrix. Every intersection in both matrices contains a Ti:W fuse link which can be independently addressed and programmed using commercially available PROM type programmers.

FUNCTIONAL BLOCK DIAGRAM FOR THE 'LS333



PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

PIN	PIN NAME	FUNCTIONAL DESCRIPTION
1	I	INPUT One of twelve inputs to the AND matrix
2	H	INPUT One of twelve inputs to the AND matrix
3	G	INPUT One of twelve inputs to the AND matrix
4	F	INPUT One of twelve inputs to the AND matrix
5	E	INPUT One of twelve inputs to the AND matrix
6	D	INPUT One of twelve inputs to the AND matrix
7	C	INPUT One of twelve inputs to the AND matrix
8	B	INPUT One of twelve inputs to the AND matrix
9	A	INPUT One of twelve inputs to the AND matrix
10	F0	OUTPUT One of six outputs from the OR matrix
11	F1	OUTPUT One of six outputs from the OR matrix
12	GND	GROUND Device and substrate ground
13	F2	OUTPUT One of six outputs from the OR matrix
14	F3	OUTPUT One of six outputs from the OR matrix
15	F4	OUTPUT One of six outputs from the OR matrix
16	F5	OUTPUT One of six outputs from the OR matrix
17	$\overline{CS}$	INPUT Chip select; when low, outputs are active; when high, outputs are in high impedance ('LS333,'LS335)
17	PS	INPUT Polarity select for the six outputs, F0 thru F5 ('LS334, 'LS336)
18	$\overline{LE}$	INPUT Latch enable; when low, output latches are enabled; when high, output latches are disabled ('LS333,'LS335)
18	$\overline{CS}$	INPUT Chip select; when low, outputs are active; when high, outputs are in high impedance ('LS334, 'LS336)
19	PM	INPUT Programming mode; when low, the AND matrix is selected for programming; when high (10.5V), the OR matrix is selected for programming
20	PL	INPUT Programming latch; causes the AND/OR term address to be latched for fusing (AND = 0V→10.5V) (OR = 0V→5V)
21	L/$\overline{OE}$	INPUT One of twelve inputs to the AND matrix or outpt enable. User defined via fusing. When used as an output enable, the input is ORed with $\overline{CE}$ for output 3-state control
22	K	INPUT One of twelve inputs to the AND matrix
23	J	INPUT One of twelve inputs to the AND matrix
24	V_{CC}	V_{CC} +5V power supply pin

programming the FPLA

The 'LS333 thru 'LS336 FPLAs are fabricated to include reliable low-voltage programmable Ti:W fuse links which have identical fusing characteristics with those used for most of TI's PROMs. The AND and OR matrices and the data/enable input, L/$\overline{OE}$, can be programmed independently. This means the commercially available PROM programmers can be used to program the low power Schottky FPLAs.

recommended conditions for programming

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (see Note 1)		4.75	5	5.25	V
Program pulse voltage, $V_{(pr)}$		10	10.5	11†	V
Program pulse rise time			100		ns
Input voltage (see Note 1)	High level, V_{IH}	2.4		5	V
	Low level, V_{IL}	0		0.5	V
Duration of programming pulse Y (see Figures and Note 2)		98	100	1000	μs
Programming duty cycle			25	35	%
Free-air temperature, T_A		0		50	°C

†Absolute maximum ratings.

NOTES: 1. Voltage values are with respect to the GND terminal, pin 12.
2. Programming is guaranteed if the pulse applied is 98 μs in duration.

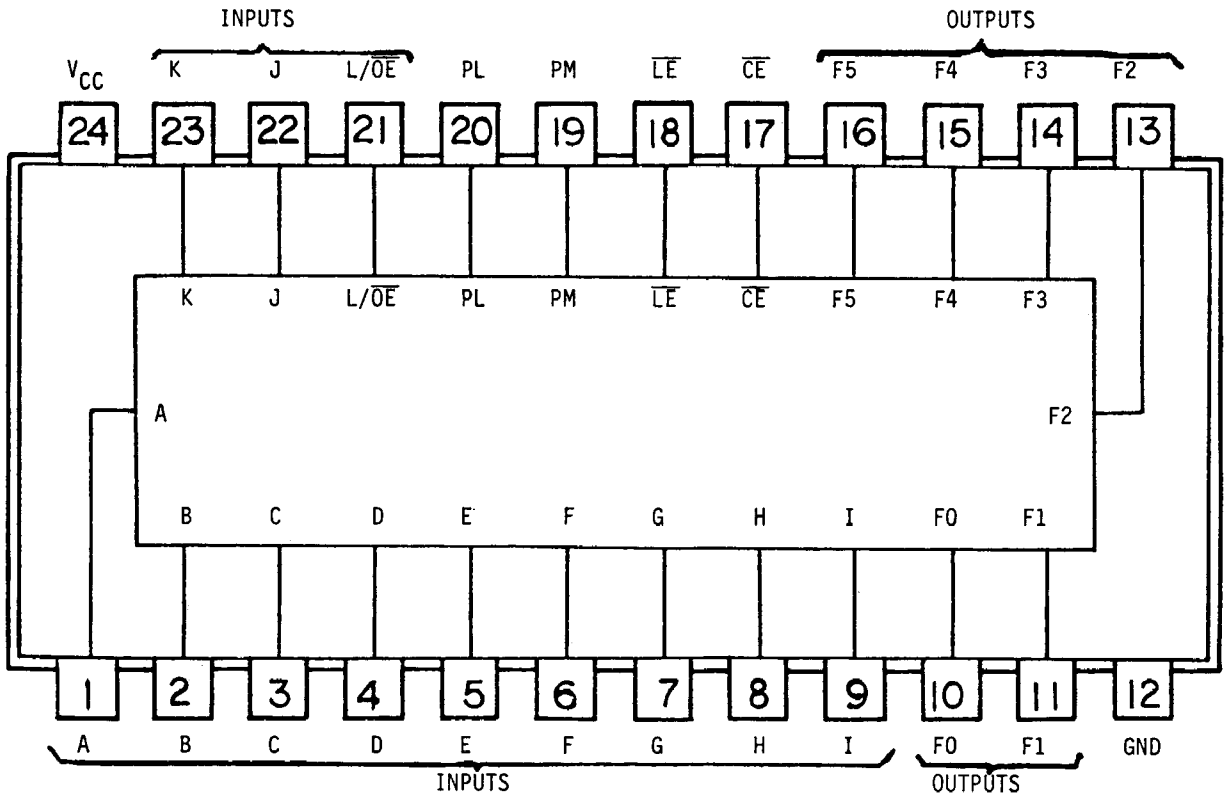
programming the L/$\overline{OE}$ input, pin 21

The L/$\overline{OE}$ input must be programmed either to function as a dedicated output enable or to function as the 12th input, L.

If it is to become the 12th data input, a single fuse at term 32 should be programmed in accordance with the L/$\overline{OE}$ function procedure below. Input L is then logically equivalent to the other eleven inputs A thru K and must be programmed in the same fashion.

If the L/$\overline{OE}$ input is to function as a dedicated output enable, term 32 is not fused, however, both AND/$\overline{AND}$ fuse links at each of the 32 product term addresses (0 thru 31) must be fused as outlined in the AND matrix programming procedure creating a "don't care" for input L. This causes the input to become ORed with the $\overline{CE}$. chip enable, pin for 3-state control of the outputs.

SN54LS333, SN54LS335.....J OR W PACKAGE
SN74LS333, SN74LS335.....J OR N PACKAGE



SN54LS334, SN54LS336.....J OR W PACKAGE
SN74LS334, SN74LS336.....J OR N PACKAGE