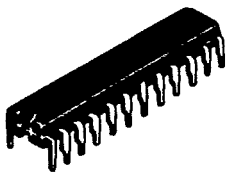
65536-word x 4-bit High Speed Hi-BiCMOS Static RAM

Features

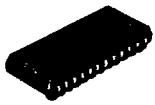
- Super Fast Access Time : 20/25ns (max.)
- Low Power Dissipation
  Operating: 350mW (typ.) (f = 50MHz)
- +5V Single Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Balanced Read and Write Cycle Time
- Fully TTL Compatible Input and Output

HM6708P



(DP-24NC)

HM6708JP

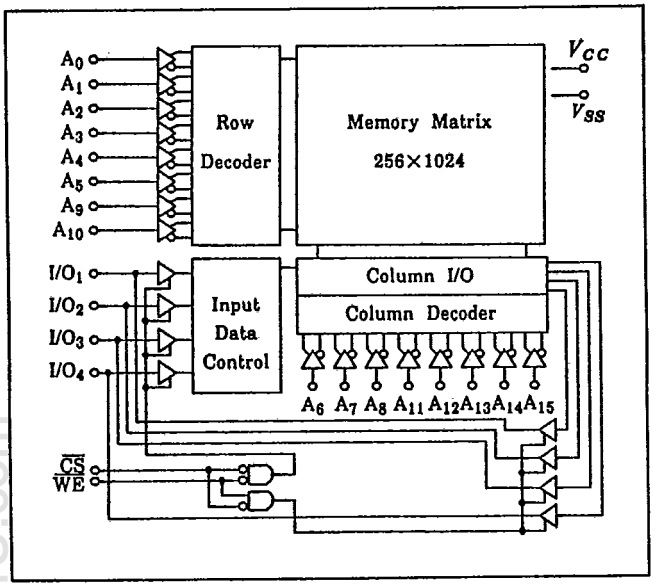


(CP-24D)

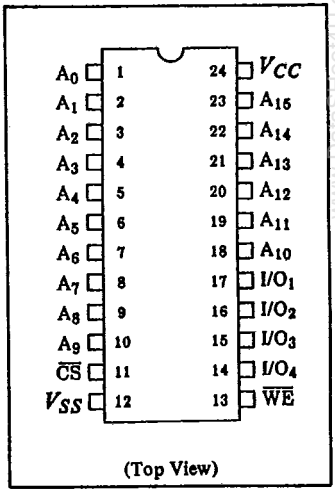
Ordering Information

Type No.	Access Time	Package
HM6708P-20	20ns	300mil 24 pin
HM6708P-25	25ns	Plastic DIP
HM6708JP-20	20ns	300 mil
HM6708JP-25	25ns	24 pin SOJ

Block Diagram



Pin Arrangement



(Top View)

Note) The specifications of this device are subject to change without notice.
Please contact Hitachi's Sales Dept. regarding specifications.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (with bias)	$T_{stg(bias)}$	−10 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

Recommended DC Operating Conditions (T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0 V for pulse width 20ns.

Function Table

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	Not selected	I_{SB}, I_{SB1}	High Z	–
L	H	Read	I_{CC}, I_{CC1}	Data Out	Read Cycle
L	L	Write	I_{CC}, I_{CC1}	Data In	Write Cycle

DC and Operating Characteristics (V_{CC} = 5 V ±10%, T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	–	–	2	μA	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	–	–	10	μA	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	–	–	100	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA
Average Operating Current	I_{CC1}	–	–	120	mA	Min. Cycle, Duty: 100%, $I_{I/O}$ = 0mA
Standby Power Supply Current	I_{SB}	–	–	30	mA	$\overline{CS}$ = V_{IH}, V_{IN} = V_{IH} or V_{IL}
	I_{SB1}	–	–	10	mA	$\overline{CS}$ ≧ V_{CC}−0.2 V V_{IN} ≦ 0.2 V or V_{IN} ≧ V_{CC}−0.2V
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH} = −4 mA

Capacitance (T_a = 25°C, f = 1 MHz)

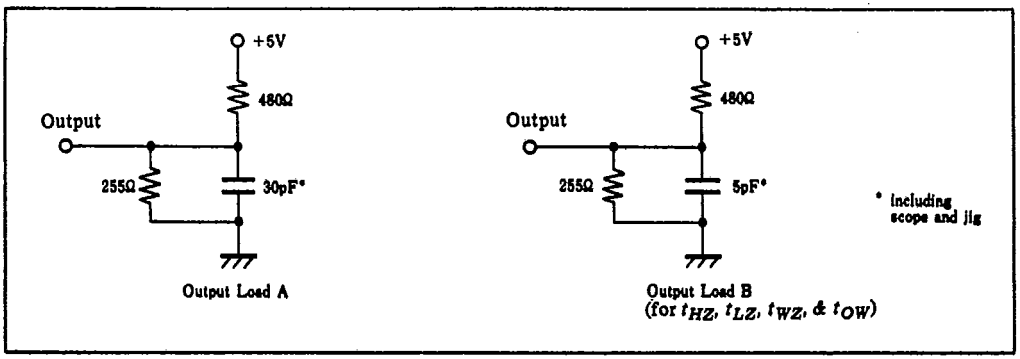
Item	Symbol	max.	Unit	Test Conditions
Input Capacitance	C_{IN}	6.0	pF	V_{IN} = 0 V
Input/Output Capacitance	$C_{I/O}$	10.0	pF	$V_{I/O}$ = 0V

Note) This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC} = 5 V ±10%, T_a = 0 to +70°C, unless otherwise noted)

AC Test Conditions

- Input pulse levels : V_{SS} to 3.0 V
- Input timing reference levels : 1.5 V
- Output Load : See Figure
- Input rise and fall times : 4 ns
- Output reference levels : 1.5 V

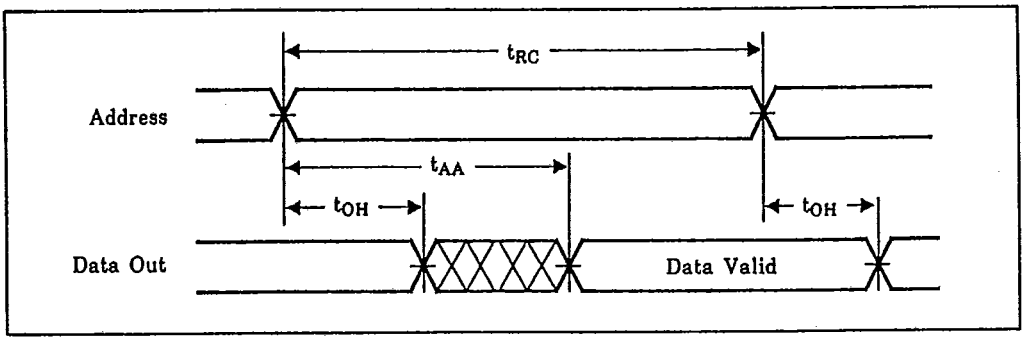


Read Cycle

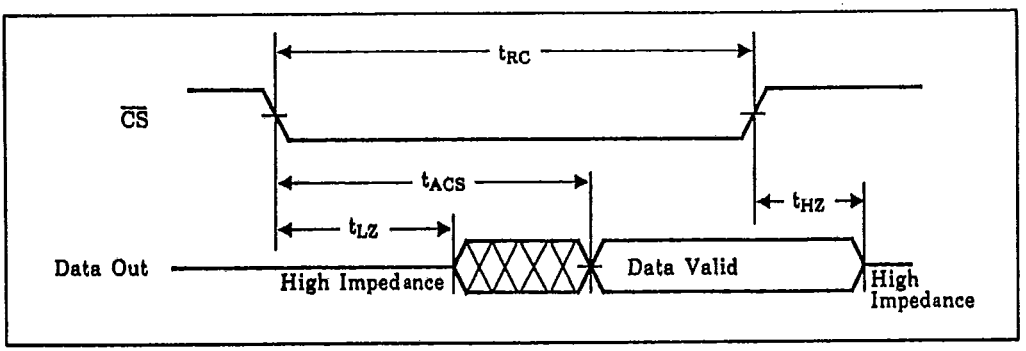
Item	Symbol	HM6708-20		HM6708-25		Unit	Notes
		min.	max.	min.	max.		
Read Cycle Time	t_{RC}	20	–	25	–	ns	–
Address Access Time	t_{AA}	–	20	–	25	ns	–
Chip Select Access Time	t_{ACS}	–	20	–	25	ns	–
Output Hold from Address Change	t_{OH}	5	–	5	–	ns	–
Chip Selection to Output in Low Z	t_{LZ}	0	–	0	–	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	8	0	10	ns	1, 2

Note) 1. This parameter is sampled and not 100% tested.
2. Transition is measured ±200 mV from steady state voltage with specified loading in Load B.

Read Cycle-1*1,*2



Read Cycle-2*1,*3



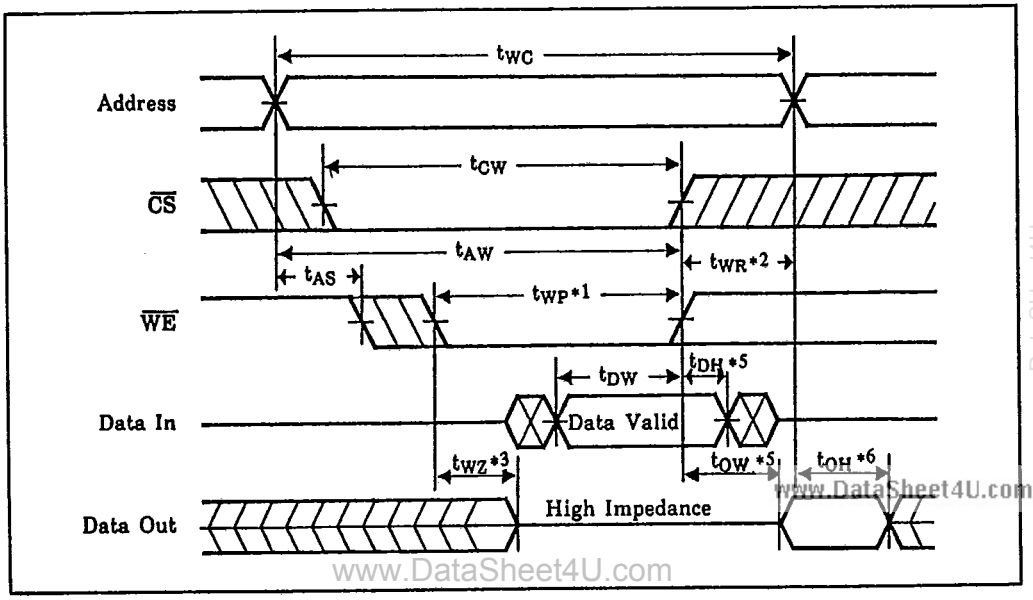
Notes) *1. $\overline{WE}$ is High for Read cycle.
*2. Device is continuously selected, $\overline{CS} = V_{IL}$.
*3. Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle

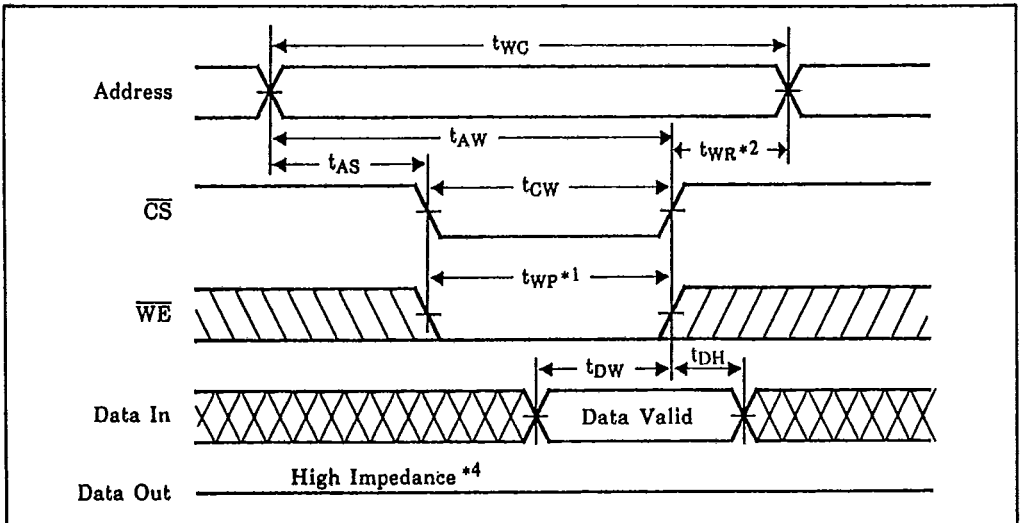
Item	Symbol	HM6708-20		HM6708-25		Unit	Notes
		min.	max.	min.	max.		
Write Cycle Time	t_{WC}	20	–	25	–	ns	2
Chip Selection to End of Write	t_{CW}	15	–	20	–	ns	–
Address Valid to End of Write	t_{AW}	15	–	20	–	ns	–
Address Setup Time	t_{AS}	0	–	0	–	ns	–
Write Pulse Width	t_{WP}	15	–	20	–	ns	–
Write Recovery Time	t_{WR}	3	–	3	–	ns	–
Data Valid to End of Write	t_{DW}	12	–	15	–	ns	–
Data Hold Time	t_{DH}	0	–	0	–	ns	–
Write Enable to Output in High Z	t_{WZ}	0	8	0	10	ns	3, 4
Output Active from End of Write	t_{OW}	0	–	0	–	ns	3, 4

Note) 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±200 mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

Write Cycle-1 ($\overline{WE}$ Controlled)



Write Cycle-2 ($\overline{CS}$ Controlled)



Note) *1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP})
*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
*5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
*6. Output is the same phase of write data of this write cycle.