PS21867

Transfer-Mold Type
Insulated Type

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Apr.	M.Iwasaki '01-12/21			M.Fukunaga '03-8/6

Applications : AC100V~200V three-phase inverter drive for small power motor control.

Integrated Power Functions :

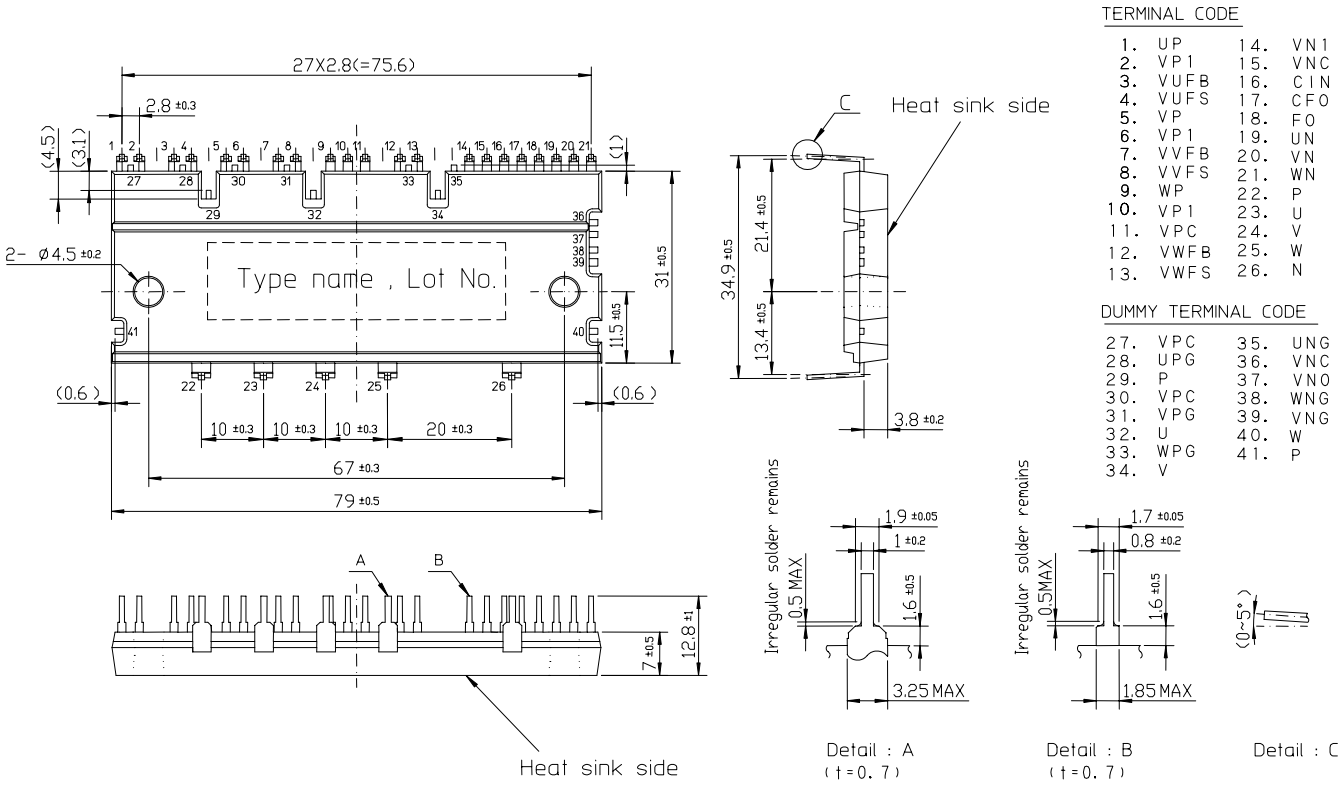
600V/30A low-loss 5th generation IGBT inverter bridge for 3 phase DC-to-AC power conversion

Integrated drive, protection and system control functions :

- For upper-leg IGBTs : Drive circuit, High voltage isolated high-speed level shifting, Control supply under-voltage (UV) protection.
- For lower-leg IGBTs : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC). (Fig.3)
- Fault signaling : Corresponding to an SC fault (Lower-side IGBT) or a UV fault (Low-sideer supply).
- Input interface : 5V line CMOS/TTL compatible.(high Active)

UL Approved : Yellow Card No. E80276

Fig. 1 Package Outlines



TERMINAL CODE

1.	UP	14.	VN1
2.	VP1	15.	VNC
3.	VUFB	16.	CIN
4.	VUFS	17.	CFO
5.	VP	18.	FO
6.	VP1	19.	UN
7.	VVFB	20.	VN
8.	VVFS	21.	WN
9.	WP	22.	P
10.	VP1	23.	U
11.	VPC	24.	V
12.	VWFB	25.	W
13.	VWFS	26.	N

DUMMY TERMINAL CODE

27.	VPC	35.	UNG
28.	UPG	36.	VNC
29.	P	37.	VNO
30.	VPC	38.	WNG
31.	VPG	39.	VNG
32.	U	40.	W
33.	WPG	41.	P
34.	V		

Maximum Ratings (Tj=25 °C, unless otherwise noted) :
Inverter Part :

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}	Applied between P-N	450	V
Supply voltage (surge)	$V_{CC(surge)}$	Applied between P-N	500	V
Collector-emitter voltage	V_{CES}		600	V
Each IGBT collector current	$\pm I_C$	Tf=25°C	30	A
Each IGBT collector current (peak)	$\pm I_{CP}$	Tf=25°C, less than 1ms	60	A
Collector dissipation	P_C	Tf=25°C, per 1 chip	60.6	W
Junction temperature	T_j	(Note 1)	-20～+125	°C

(Note1) The maximum junction temperature rating of the power chips integrated within the DIP-IPM is 150°C(@Tf≤100°C) however, to insure safe operation of the DIP-IPM, the average junction temperature should be limited to Tj(ave)≤125°C (@Tf≤100°C).

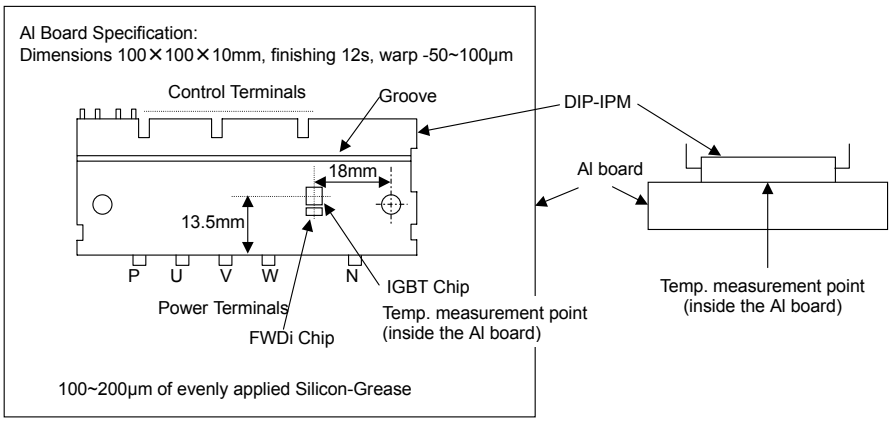
Control (Protection) Part :

Item	Symbol	Condition	Rating	Unit
Control supply voltage	V_D	Applied between V_{P1}-V_{PC}, V_{N1}-V_{NC}	20	V
Control supply voltage	V_{DB}	Applied between V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS} , V_{WFB}-V_{WFS}	20	V
Input voltage	V_{IN}	Applied between U_P, V_P, W_P-V_{PC}, U_N, V_N, W_N-V_{NC}	-0.5～V_D+0.5	V
Fault output supply voltage	V_{FO}	Applied between Fo-V_{NC}	-0.5～V_D+0.5	V
Fault output current	I_{FO}	Sink current at Fo terminal	1	mA
Current sensing input voltage	V_{SC}	Applied between CIN-V_{NC}	-0.5～V_D+0.5	V

Total System :

Item	Symbol	Condition	Rating	Unit
Self protection supply voltage limit (short circuit protection capability)	$V_{CC(PROT)}$	V_D=13.5~16.5V, Inverter part Tj=125°C, non-repetitive less than 2μs	400	V
Module case operation temperature	Tf	(Note2)	-20～+100	°C
Storage temperature	Tstg		-40～+125	°C
Isolation voltage	Viso	60Hz, Sinusoidal, AC 1 minutes, connecting pins to heat-sink plate	2500	Vrms

(Note2) Tf measurement point :



Thermal Resistance :

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Junction to case thermal resistance (Note3)	$R_{th(j-f)Q}$	Inverter IGBT part (per 1/6 module)	–	–	1.65	°C／W
	$R_{th(j-f)F}$	Inverter FWD part (per 1/6 module)	–	–	3.00	

(Note3) Grease with good thermal conductivity should be applied evenly about +100μm～+200μm on the contact surface of DIP-IPM and a heat-sink.

Electrical Characteristics (Tj=25 °C, unless otherwise noted) :
Inverter Part :

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Collector-emitter saturation voltage	$V_{CE(sat)}$	$V_D=V_{DB}=15V$, $V_{IN}=0V$	I_C=30A, Tj=25°C	–	1.6	2.1	V
			I_C=30A, Tj=125°C	–	1.7	2.2	
FWD forward voltage	V_{EC}	Tj=25°C, $-I_C$=30A, V_{IN}=5V		–	1.5	2.0	V
Switching times	t_{on}	V_{CC}=300V, $V_D=V_{DB}$=15V		0.7	1.3	1.9	μs
	t_{rr}	I_C=30A		–	0.3	–	
	$t_{c(on)}$	Tj=125°C		–	0.4	0.6	
	t_{off}	Inductive load (upper-lower arm)		–	1.7	2.4	
	$t_{c(off)}$	V_{IN}=5⇔0V		–	0.5	0.8	
Collector-emitter cut-off current	I_{CES}	$V_{CE}=V_{CES}$	Tj=25°C	–	–	1	mA
			Tj=125°C	–	–	10	

Control (Protection) Part :

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Circuit current	I_D	$V_D=V_{DB}$=15V, V_{IN}=5V	Total of V_{P1}-V_{PC}, V_{N1}-V_{NC}	–	–	5.00	mA
			V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	–	–	0.40	mA
		$V_D=V_{DB}$=15V, V_{IN}=0V	Total of V_{P1}-V_{PC}, V_{N1}-V_{NC}	–	–	7.00	mA
			V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	–	–	0.55	mA
Fo output voltage	V_{FOH}	V_{SC}=0V, Fo circuit pull-up to 5V with 10kΩ		4.9	–	–	V
	V_{FOL}	V_{SC}=1V, I_{FO}=1mA		–	–	0.95	V
Input current	I_{IN}	V_{IN}=5V		1.0	1.50	2.0	mA
short circuit trip level	$V_{SC(ref)}$	Tj=25°C, V_D=15V (Note4)		0.43	0.48	0.53	V
Supply circuit under-voltage protection	UV_{DBt}	Tj≤125°C	Trip level	10.0	–	12.0	V
	UV_{DBr}		Reset level	10.5	–	12.5	V
	UV_{Dt}		Trip level	10.3	–	12.5	V
	UV_{Dr}		Reset level	10.8	–	13.0	V
Fault output pulse width	t_{FO}	C_{FO}=22nF (Note5)		1.0	1.8	–	ms
ON threshold voltage	Vth(on)	Applied between U_P,V_P,W_P-V_{PC},		2.1	2.3	2.6	V
OFF threshold voltage	Vth(off)	U_N,V_N,W_N-V_{NC}		0.8	1.4	2.1	

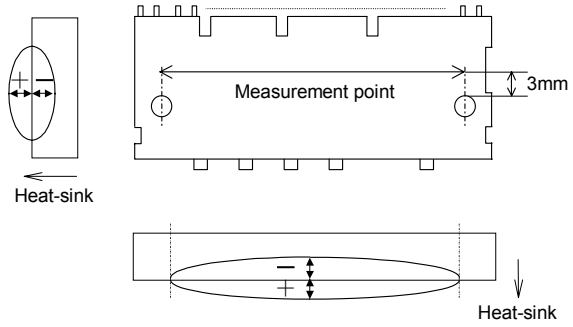
(Note4) Short circuit protection is functioning only at the low-arms. Please select the value of the external shunt resistor such that the SC trip-level is less than 51A

(Note5) Fault signal is output when the low-arms short circuit or control supply under-voltage protective functions operate. The fault output pulse-width t_{FO} depends on the capacitance value of C_{FO} according to the following approximate equation : $C_{FO}= 12.2 \times 10^{-6} \times t_{FO}$ [F]

Mechanical Characteristics and Ratings :

Item	Condition		Min.	Typ.	Max.	Unit
Mounting torque	Mounting screw: M4	Recommended: 1.18 N·m	0.98	–	1.47	N·m
Weight			–	65	–	g
Heat-sink flatness	(Note6)		–50	–	100	μm

(Note6)



Recommended Operation Conditions :

Item	Symbol	Condition		Recommended			Unit
				Min.	Typ.	Max.	
Supply voltage	V_{CC}	Applied between P-N		0	300	400	V
Control supply voltage	V_D	Applied between V_{P1}-V_{PC}, V_{N1}-V_{NC}		13.5	15.0	16.5	V
Control supply voltage	V_{DB}	Applied between V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}		13.0	15.0	18.5	V
Control supply variation	ΔV_D, ΔV_{DB}			-1	–	1	V/μs
Arm-shoot-through blocking time	t_{dead}	For each input signal, Tf≤100°C		2	–	–	μs
PWM input frequency	f_{PWM}	Tf≤100°C, Tj≤125°C		–	–	20	kHz
Allowable r.m.s current	I_O	V_{CC}=300V, V_D=V_{DB}=15V, P.F=0.8, sinusoidal PWM, Tj≤125°C, Tf≤100°C (Note7)	f_{PWM}=5kHz	–	–	19	Arms
			f_{PWM}=15kHz	–	–	11.6	
Minimum input pulse width	PWIN(on)	(Note8)		0.3	–	–	μs
	PWIN(off)	200≦V_{CC}≦350V, 13.5≦V_D≦16.5V, 13.0≦V_{DB}≦18.5V, -20°C≦Tf≦100°C, N-line wiring inductance less than 10nH (Note 9)	Below rated current	1.5	–	–	
			Between rated current and 1.7 times of rated current	3.0	–	–	
V_{NC} variation	V_{NC}	between V_{NC}-N (including surge)		-5.0	–	5.0	V

(Note 7) The Allowable r.m.s. current value depends on the actual application conditons.
(Note 8) Input signal with ON pulse width less than PWIN(on) might make no response.
(Note 9) IPM might not work properly or make response for the Input signal with OFF pulse width less than PWIN(off). Please refer to Fig. 5 for recommended wiring method.

Fig.2 The DIP-IPM Internal Circuit :

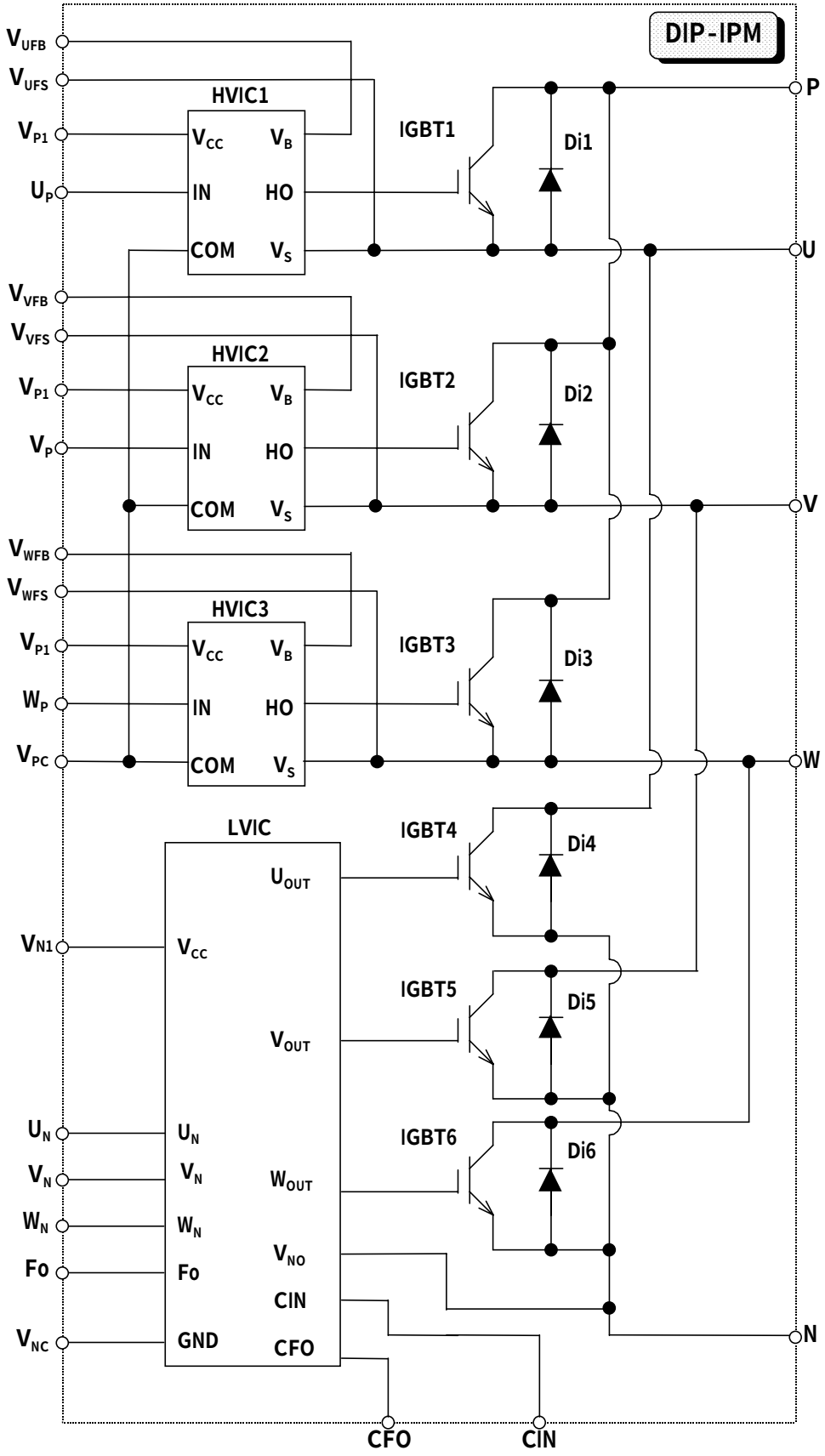
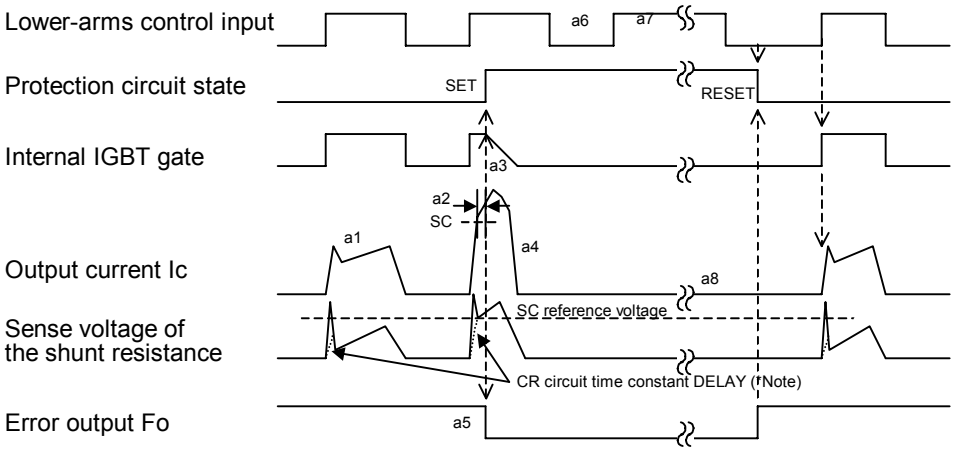


Fig.3 Timing Charts of the DIP-IPM Protective Functions

[A] Short-Circuit Protection (Lower-arms only)
(For the external shunt resistance and CR connection)

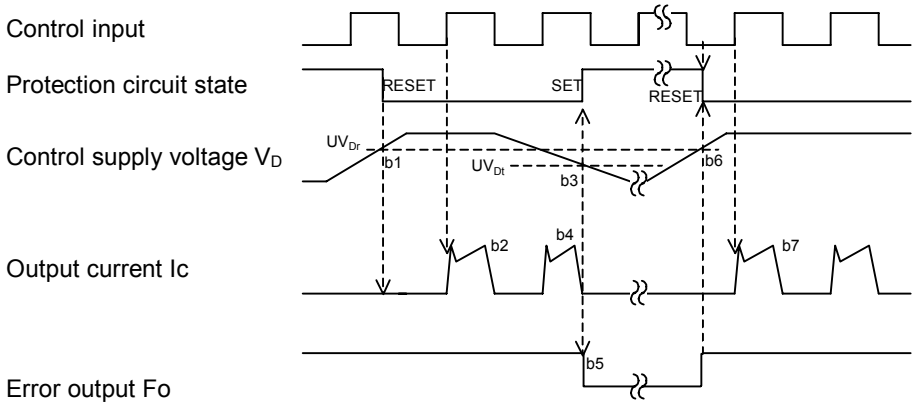
a1. Normal operation : IGBT ON and carrying current.
a2. Short circuit current detection (SC trigger).
a3. Hard IGBT gate interrupt.
a4. IGBT turns OFF.
a5. Fo timer operation starts : The pulse width of the Fo signal is set by the external capacitor C_{FO}.
a6. Input "L" : IGBT OFF state.
a7. Input "H" : IGBT ON state, but during the Fo active signal the IGBT doesn't turn ON.
a8. IGBT OFF state.



(*note) The CR time constant safe guards against erroneous SC signal resulting from di/dt generated voltages when the IGBT turns ON. The optimum setting for the CR circuit time constant is 1.5~2.0μs.

[B] Under- Voltage Protection (Lower-arm, UV_D)

b1. Control supply voltage rises : After the voltage level reaches UV_{Dr}, the circuits start to operate when t he next input is applied.
b2. Normal operation : IGBT ON and carrying current.
b3. Under voltage trip (UV_{Dt}).
b4. IGBT OFF in spite of control input condition.
b5. Fo operation starts.
b6. Under voltage reset (UV_{Dr}).
b7. Normal operation : IGBT ON and carrying current.



[C] Under- Voltage Protection (Upper-arm, UV_{DB})

c1. Control supply voltage rises : After the voltage level reaches UV_{DBr}, the circuits start to operate when the next input is applied.
c2. Normal operation : IGBT ON and carrying current.
c3. Under voltage trip (UV_{DBt}).
c4. IGBT OFF in spite of control input condition, but there is no Fo signal output.
c5. Under voltage reset (UV_{DBr}).
c6. Normal operation : IGBT ON and carrying current.

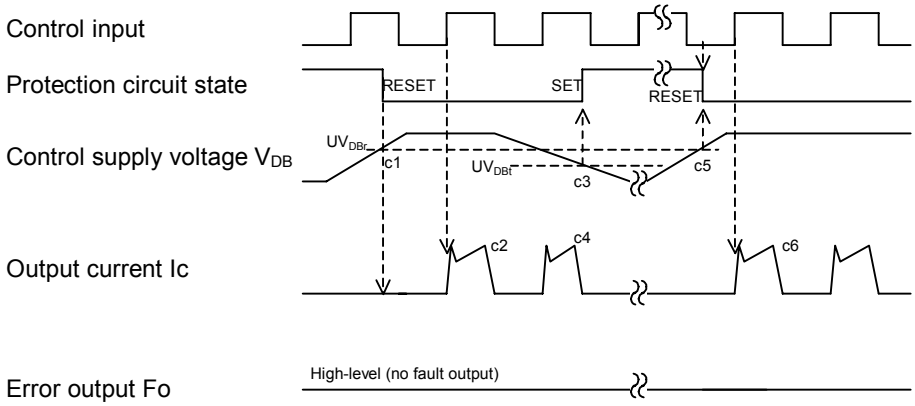
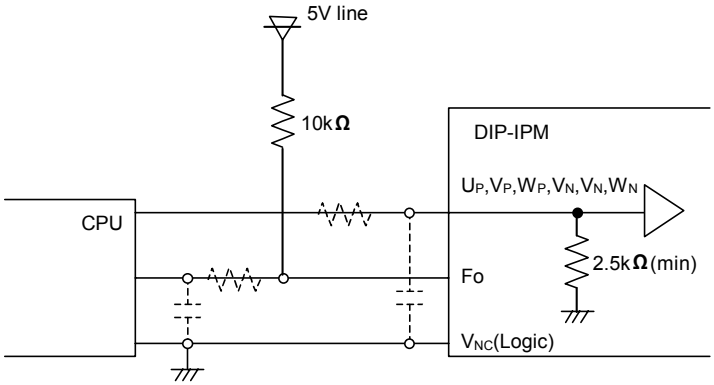


Fig.4 Recommended CPU I/O interface circuit :



Note) RC coupling at each input (parts shown dotted) may change depending on the PWM control scheme used in the application and on the wiring impedance of the application's printed circuit board.
The DIP-IPM input signal section integrates a 2.5kΩ(min) pull-down resister. Therefore, when an external filtering resistor is used, care must be taken to satisfy the turn-on threshold voltage requirement.

Fig.5 Recommended wiring of shunt resistor :

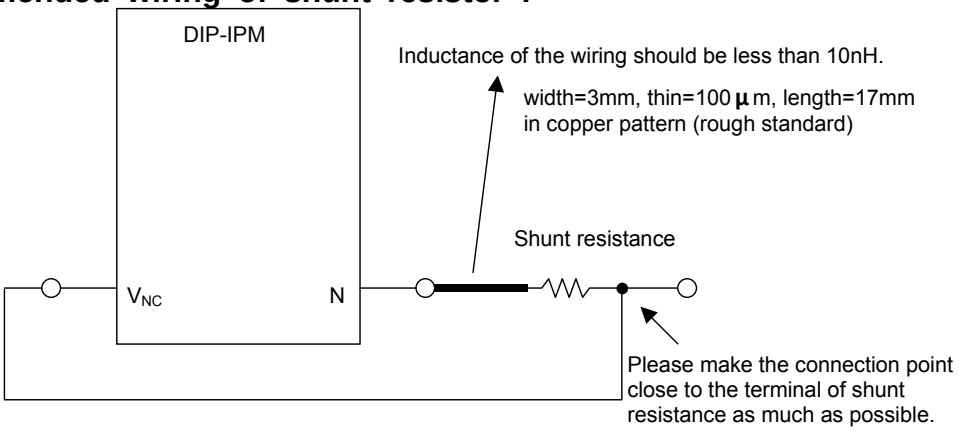
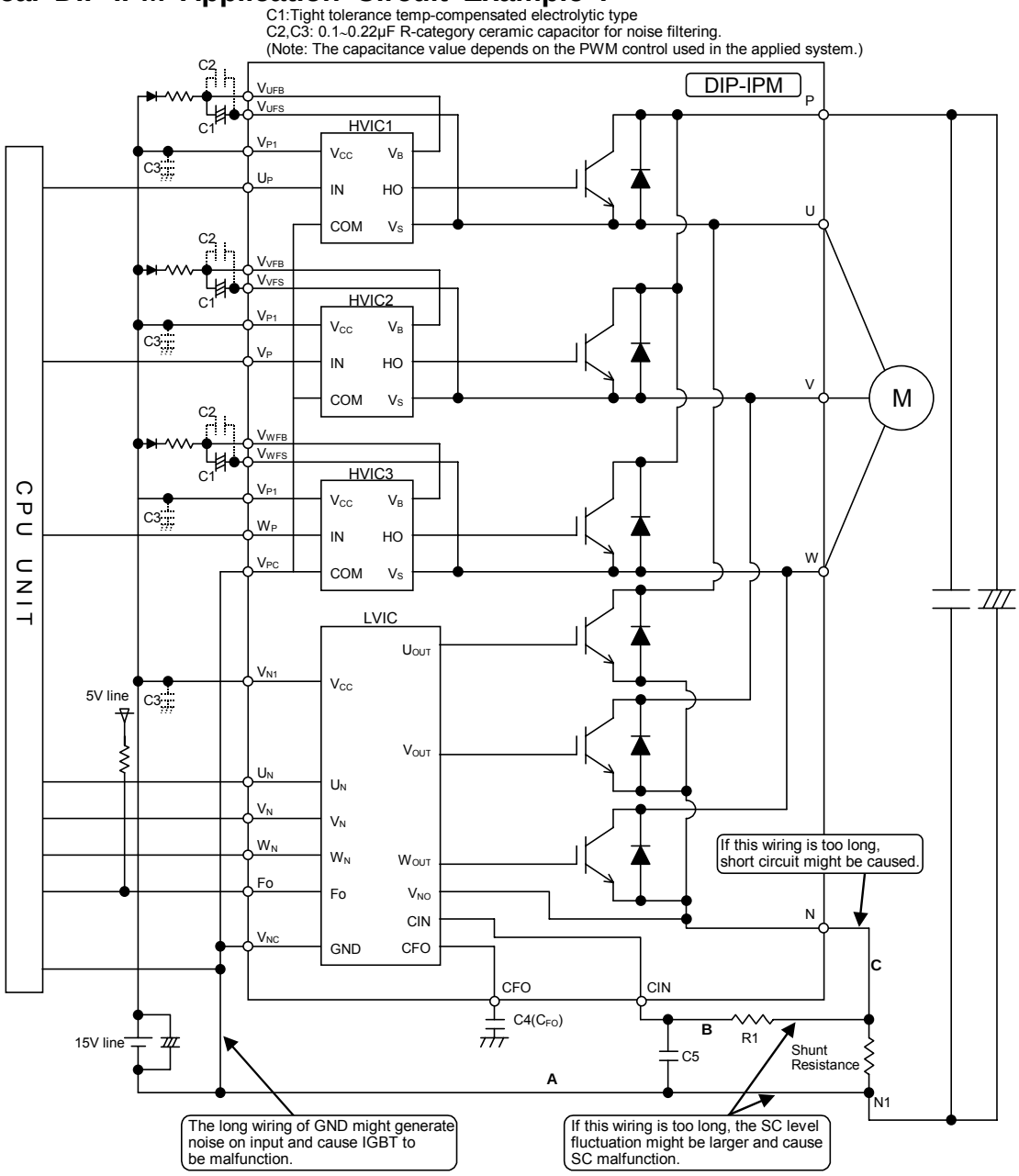


Fig.6 Typical DIP-IPM Application Circuit Example :



Note1) To prevent the input signals oscillation, the wiring of each input should be as short as possible. (Less than 2cm)

Note2) By virtue of integrating an application specific type HVIC inside the module, direct coupling to CPU terminals without any opto-coupler or transformer isolation is possible.

Note3) Fo output is open collector type. This signal line should be pulled up to the positive side of the 5V power supply with approximately 10kΩ resistance.

Note4) Fo output pulse width should be decided by connecting an external capacitor between CFO and V_{NC} terminals (C_{FO}). (Example：C_{FO} = 22 nF → t_{FO} = 1.8 ms (typ.))

Note5) The logic of input signal is active high. The DIP-IPM input signal section integrates a 2.5kΩ(min) pull-down resister. Therefore, when an external filtering resistor is used, care must be taken to satisfy the turn-on threshold voltage requirement.

Note6) To prevent errors of the protection function, the wiring of A, B, C should be as short as possible.

Note7) In the recommended protection circuit, please select the R_1C_5 time constant in the range 1.5~2μs.

Note8) Each capacitor should be put as nearby the pins of the DIP-IPM as possible.

Note9) To prevent surge destruction, the wiring between the smoothing capacitor and the P&N1 pins should be as short as possible. Approximately a 0.1~0.22μF snubber capacitor between the P&N1 pins is recommended.