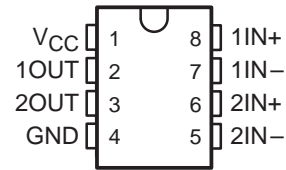


uA9637AC DUAL DIFFERENTIAL LINE RECEIVER

SLLS111B – SEPTEMBER 1980 – REVISED MAY 1995

- Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-422-B and EIA/TIA-423-B and ITU Recommendations V.10 and V.11
- Operates From Single 5-V Power Supply
- Wide Common-Mode Voltage Range
- High Input Impedance
- TTL-Compatible Outputs
- High-Speed Schottky Circuitry
- 8-Pin Dual-in-Line and Small-Outline Packages
- Designed to Be Interchangeable With National DS9637A

uA9637AC . . . D OR P PACKAGE
(TOP VIEW)

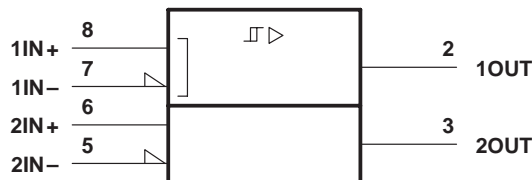


description

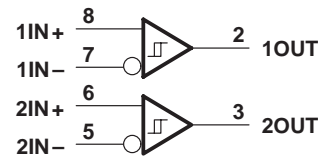
The uA9637AC is a dual differential line receiver designed to meet ANSI Standards EIA/TIA-422-B and EIA/TIA-423-B and ITU Recommendations V.10 and V.11. The line receiver utilizes Schottky circuitry and has TTL-compatible outputs. The inputs are compatible with either a single-ended or a differential-line system. This device operates from a single 5-V power supply and is supplied in an 8-pin dual-in-line package or small-outline package.

The uA9637AC is characterized for operation from 0°C to 70°C.

logic symbol†



logic diagram



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

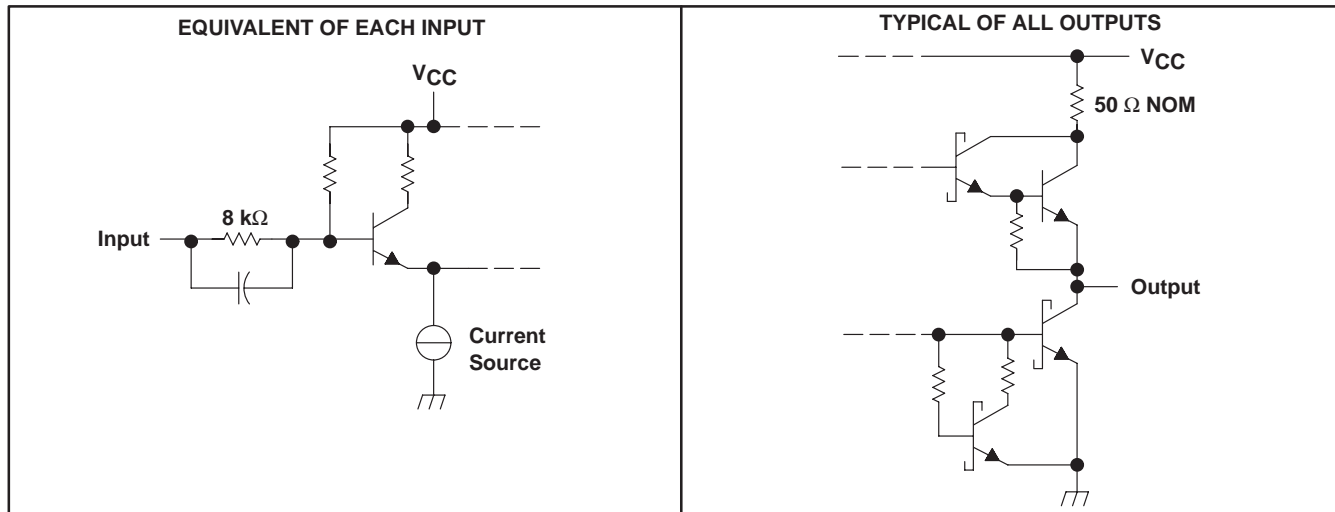
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1995, Texas Instruments Incorporated

uA9637AC DUAL DIFFERENTIAL LINE RECEIVER

SLLS111B – SEPTEMBER 1980 – REVISED MAY 1995

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	-0.5 V to 7 V
Input voltage, V_I	± 15 V
Differential input voltage, V_{ID} (see Note 2)	± 15 V
Output voltage range, V_O (see Note 1)	-0.5 V to 5.5 V
Low-level output current, I_{OL}	50 mA
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.
 2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$	OPERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$	$T_A = 125^\circ\text{C}$
	POWER RATING		POWER RATING	POWER RATING
D	725 mW	5.8 mW/°C	464 mW	—
P	1000 mW	8.0 mW/°C	640 mW	—

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			± 7	V
Operating free-air temperature, T_A	0		70	$^{\circ}\text{C}$

electrical characteristics over recommended ranges of supply voltage, common-mode input voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT	
V_{IT+}	Positive-going input threshold voltage	See Note 3			0.2 0.4	V	
V_{IT-}	Negative-going input threshold voltage	See Note 3	-0.2		-0.4 [‡]	V	
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)			70		mV	
V_{OH}	High-level output voltage	$V_{ID} = 0.2\text{ V}$, $I_O = -1\text{ mA}$	2.5	3.5		V	
V_{OL}	Low-level output voltage	$V_{ID} = -0.2\text{ V}$, $I_O = 20\text{ mA}$		0.35	0.5	V	
I_I	Input current	$V_{CC} = 0\text{ to }5.5\text{ V}$, See Note 4		$V_I = 10\text{ V}$ $V_I = -10\text{ V}$	1.1 -1.6	3.25 -3.25	mA
I_{OS}	Short-circuit output current [§]	$V_O = 0$, $V_{ID} = 0.2\text{ V}$	-40	-75	-100	mA	
I_{CC}	Supply current	$V_{ID} = -0.5\text{ V}$, No load		35	50	mA	

[†] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡] The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.

[§] Only one output should be shorted at a time, and duration of the short circuit should not exceed one second.

NOTES: 3. The expanded threshold parameter is tested with a 500- Ω resistor in series with each input.

4. The input not under test is grounded.

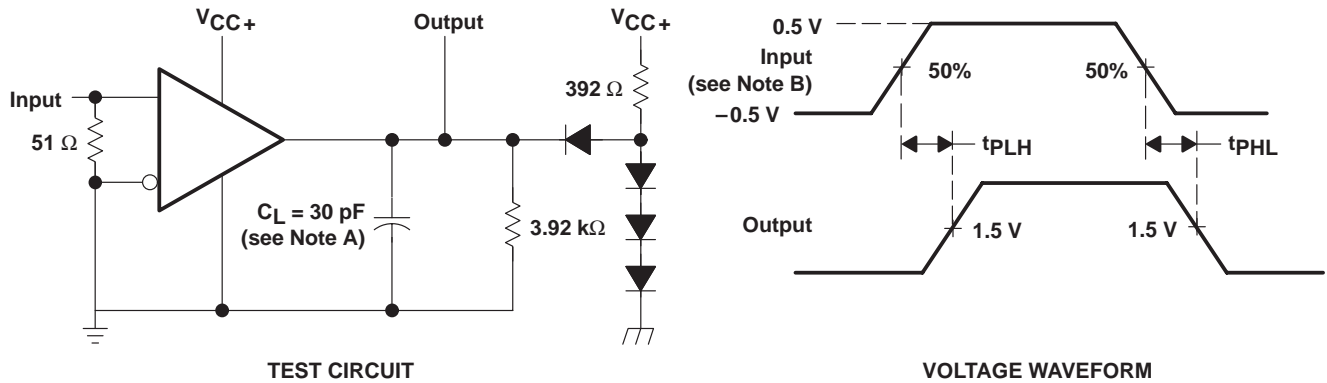
switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	$C_L = 30\text{ pF}$, See Figure 1		15	25	ns
t_{PHL}	Propagation delay time, high- to low-level output			13	25	ns

uA9637AC DUAL DIFFERENTIAL LINE RECEIVER

SLLS111B – SEPTEMBER 1980 – REVISED MAY 1995

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, $PRR \leq 5$ MHz, duty cycle = 50%.

Figure 1. Test Circuit and Voltage Waveform

TYPICAL CHARACTERISTICS

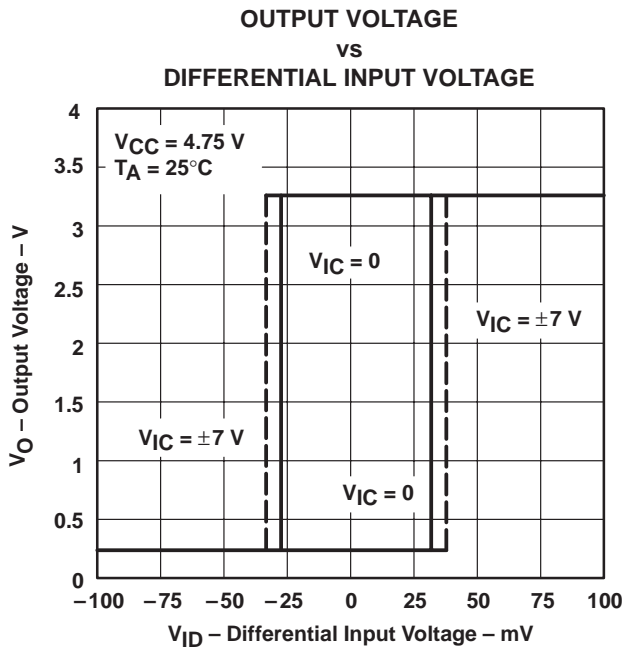


Figure 2

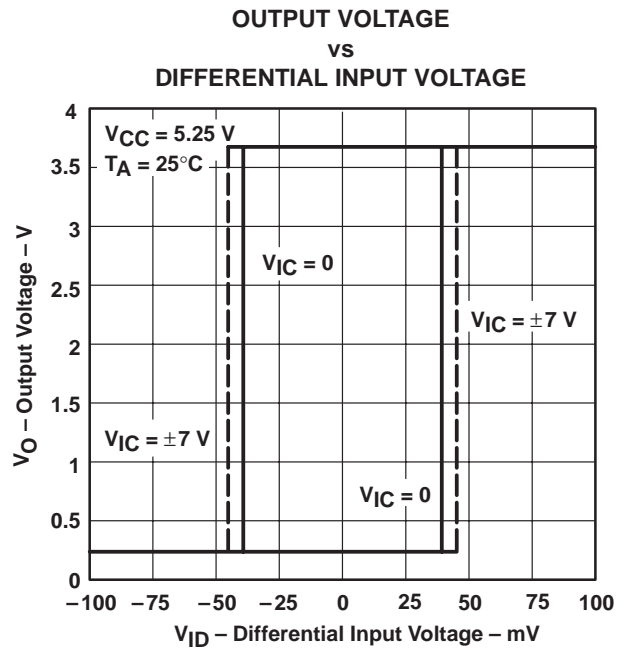


Figure 3

TYPICAL CHARACTERISTICS

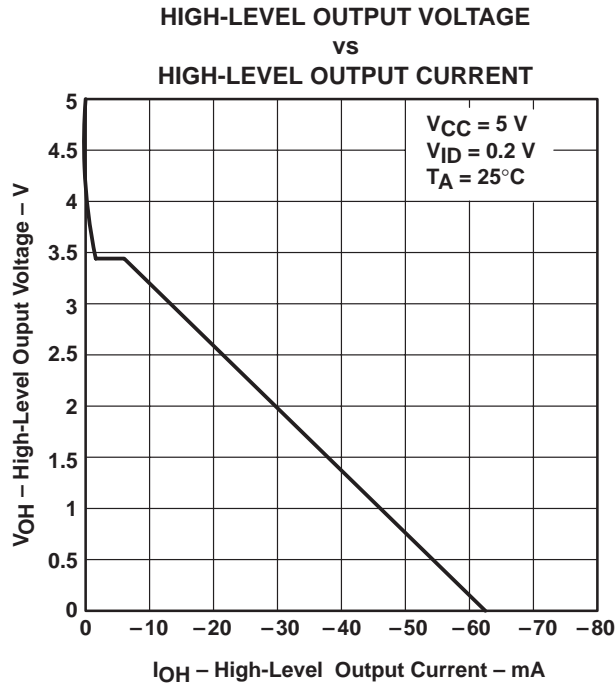


Figure 4

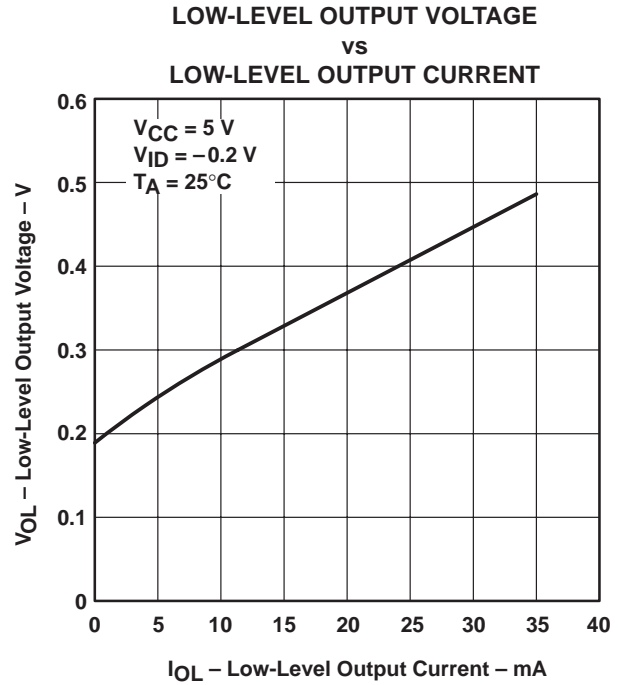


Figure 5

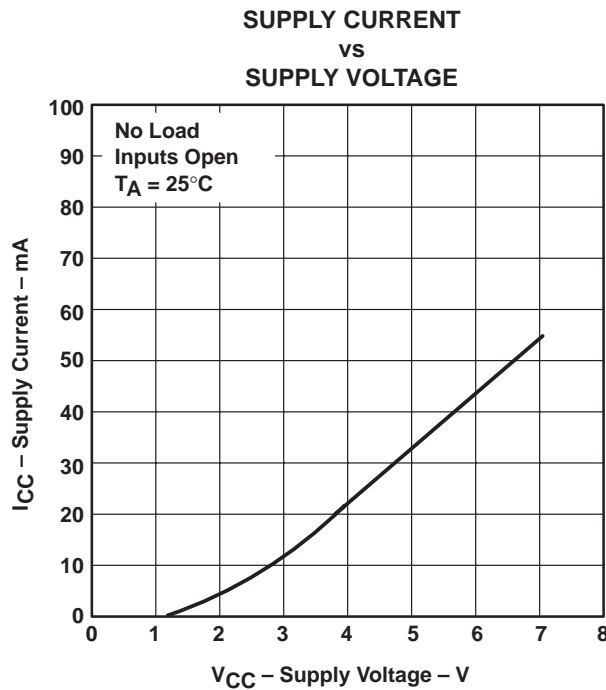


Figure 6

uA9637AC DUAL DIFFERENTIAL LINE RECEIVER

SLLS111B – SEPTEMBER 1980 – REVISED MAY 1995

APPLICATION INFORMATION

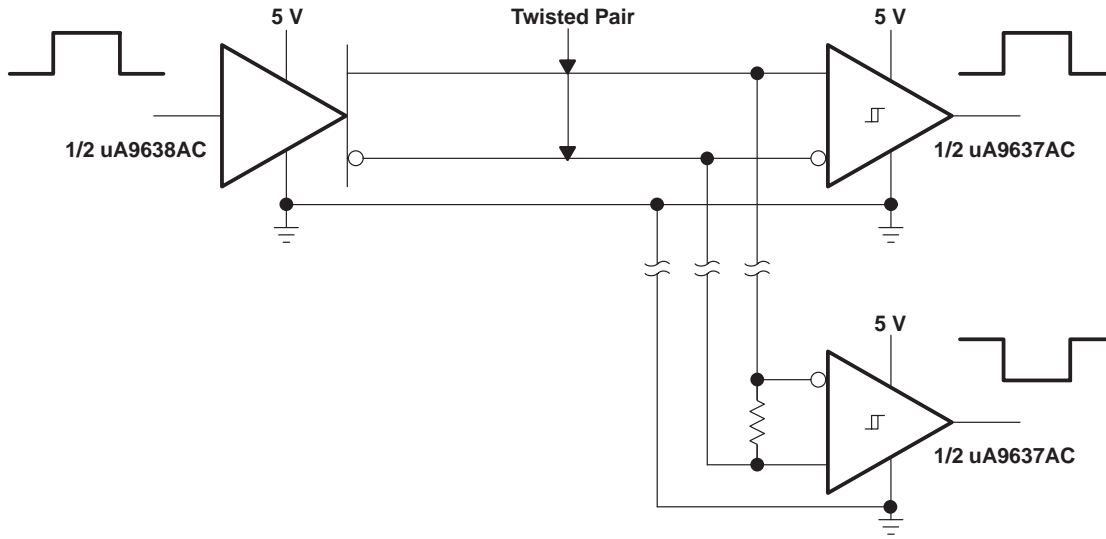


Figure 7. EIA/TIA-422-B System Applications

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UA9637ACD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	9637AC	Samples
UA9637ACDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	9637AC	Samples
UA9637ACDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	9637AC	Samples
UA9637ACDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	9637AC	Samples
UA9637ACDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	9637AC	Samples
UA9637ACP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UA9637ACP	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA9637ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA9637ACDR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
UA9637ACD	D	SOIC	8	75	507	8	3940	4.32
UA9637ACDG4	D	SOIC	8	75	507	8	3940	4.32
UA9637ACP	P	PDIP	8	50	506	13.97	11230	4.32



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



4040082/E 04/2010

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated