

1, Description

TM1638 is LED driver controller with key-scan interface, MCU digital interface, data latch, LED high pressure driver, key-scan is integrated into a single chip. TM1638 main apply for fridge, air condition and home theatre as high-seg display driver.

2. Feature

- | Power CMOS technology
- | Display mode 10seg × 8grid
- | Key-scan(8 × 3bit)
- | Gray adjust circuit(duty ratio 8 level is adjustable)
- | Serial connection (CLK , STB , DIO)
- | Oscillation type: RC oscillation(450Hz+5%)
- | Build-in power-on reset circui
- | SOP28 package

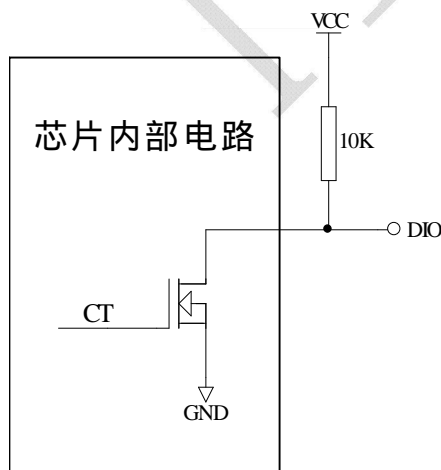
3. Pin definition

1			28
2	K1	STB	27
3	K2	CLK	26
4	K3	DIO	25
5	VDD	GND	24
6	SEG1/KS1	GRID1	23
7	SEG2/KS2	GRID2	22
8	SEG3/KS3	GRID3	21
9	SEG4/KS4	GRID4	20
10	SEG5/KS5	GRID5	19
11	SEG6/KS6	GRID6	18
12	SEG7/KS7	GND	17
13	SEG8/KS8	GRID7	16
14	SEG9	GRID8	15
	SEG10	VDD	

4. Pin function definition

Symbol	Pin name	description
DIO	Data input/output	Input/output serial data during the rising of shift clock, from low.
STB	Chip select	Initialize serial interface during the falling/rising edge, then receive instruction. The first byte as instruction when STB is low, another disposal would be closed during handle the instruction. CLK would be ignored when STB is high.
CLK	Clock input	Output/input serial data at the rising edge
K1 ~ K3	Key-scan data input	data inputted into the Pin would be latch after display cycle close.
SEG1/KS1~ SEG8/KS8	output (segment)	Segment output, P pipe open-drain output
SEG9 ~ SEG10	output (segment)	Segment output, p pipe open-drain output
GRID1 ~ GRID8	Output(grid)	Grid output, N pipe open-drain output
VDD	Logic power	5V±10%
GND	Logic ground	Connect ground system

Note: DIO output data is N pipe open-drain output, when read key demand connect 1K-10K rising resistance. We promote 10K rising resistance. The read data is unsteady during DIO control N pipe action at the falling edge of shift close. You could refer to below chart(6), the data is steady during the rising edge.



5. Display register address and display mode

The register transmits data from outside device to TM1638 via serial interface, address from 00H-0FH total 16 byte units. And separately correspond with LED light of chip SGE and GRID pin. As below chart:

Write LED display data from high to low of display address, from low to high of data byte.

SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	X	X	X	X	X	X	
xxHL(低四位)				xxHU(高四位)				xxHL(低四位)				xxHU(高四位)				
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	
00HL				00HU				01HL				01HU				GRID1
02HL				02HU				03HL				03HU				GRID2
04HL				04HU				05HL				05HU				GRID3
06HL				06HU				07HL				07HU				GRID4
08HL				08HU				09HL				09HU				GRID5
0AHL				0AHU				0BHL				0BHU				GRID6
0CHL				0CHU				0DHL				0DHU				GRID7
0EHL				0EHU				0FHL				0FHU				GRID8

chart (2)

Write LED display data from high to low of display address, from low to high of data byte. For don't used SEG output interface, please input 0 into correspond BIT address.

6. key-scan and key-scan data register

Key-scan frame is 8 x 3bit, as chart(3):

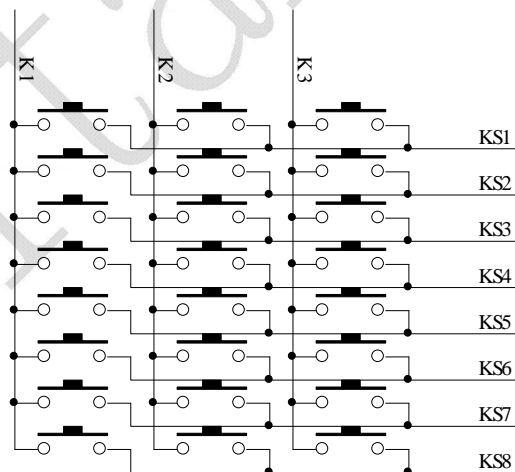


Chart (3)

Key-scan data stock address as chart(4), after send read key instruction, start to read key data BYTE1-BYTE4, read data from low to output, when press pin of chipK and KS, the BIT of correspond byte is 1.

B0	B1	B2	B3	B4	B5	B6	B7	
K3	K2	K1	X	K3	K2	K1	X	
KS1				KS2				BYTE1
KS3				KS4				BYTE2
KS5				KS6				BYTE3
KS7				KS8				BYTE4

Chart(4)

Note: 1, TM1638 read up to 4 byte, no more than 4.

2, read data byte just from BYTE1-BYTE4 in turn, cannot cut across byte to read. For example: when press the key corresponds with K2 and KS8, if want to read this key's data, must read the 4th byte the 5th bit, then can get the data; when K1 and KS8, K2 and KS8, K3 and KS8 press in the same time, the B4,B5 and B6 of BYTE4's data is 1.

3. Combination key just is same KS, different K pin. Same K and different KS cannot combine together as key combination.

7. Instruction description

Instruction to set display mode and LED driver status.

Input DIO the 1st byte as an instruction at STB falling edge. After coding, get the highest byte of B7,B6 to distinguish different instruction.

B7	B6	instruction
0	1	Data instruction set
1	0	Display control instruction set
1	1	Address instruction set

7.1 data instruction set

The instruction to set data writes and read, B1 and B0 cannot be set 01 or 11.

MSB

LSB

B7	B6	B5	B4	B3	B2	B1	B0	Function	instruction	
0	1	Not available, input 0				0	0	Data write mode set	Write data to register	
0	1						1	0	Address add mode set	Read key-scan data
0	1					0			Address add mode set	Auto address add
0	1					1			Address add mode set	Fixed address
0	1				0				test mode set(inner use)	Normal mode
0	1				1				test mode set(inner use)	Test mode

7.2 Address instruction setting

MSB				LSB				Display address
B7	B6	B5	B4	B3	B2	B1	B0	
1	1	Not available , input 0		0	0	0	0	00H
1	1			0	0	0	1	01H
1	1			0	0	1	0	02H
1	1			0	0	1	1	03H
1	1			0	1	0	0	04H
1	1			0	1	0	1	05H
1	1			0	1	1	0	06H
1	1			0	1	1	1	07H
1	1			1	0	0	0	08H
1	1			1	0	0	1	09H
1	1			1	0	1	0	0AH
1	1			1	0	1	1	0BH
1	1			1	1	0	0	0CH
1	1			1	1	0	1	0DH
1	1			1	1	1	0	0EH
1	1			1	1	1	1	0FH

The instruction is to set display register address
If address set 10H or higher, data would be ignored, till available address is set.
When power on, address default 00H.

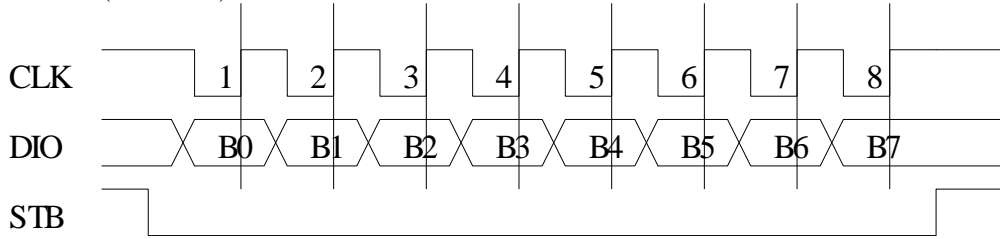
7.3 display control

MSB				LSB				Function	description	
B7	B6	B5	B4	B3	B2	B1	B0			
1	0	Irrelevant term, input 0			0	0	0	Clean light quantity set	Set pulse width is 1/16	
1	0				0	0	1		Set pulse width is 2/16	
1	0				0	1	0		Set pulse width is 4/16	
1	0				0	1	1		Set pulse width is 10/16	
1	0				1	0	0		Set pulse width is 11/16	
1	0				1	0	1		Set pulse width is 12/16	
1	0				1	1	0		Set pulse width is 13/16	
1	0				1	1	1		Set pulse width is 14/16	
					0					Display turn on/off set
1	0				1					Show turn on

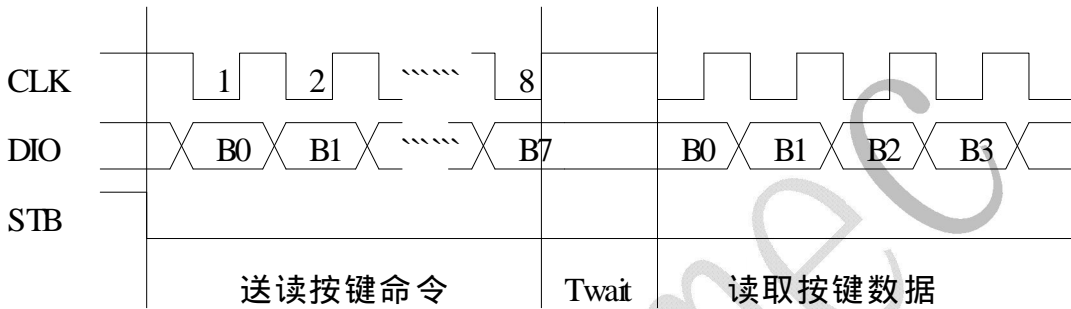
8. serial data transmit pattern:

Read and receive 1 bit should at the rising edge of shift clock.

8.1 data receive (write data)



8.2 data read

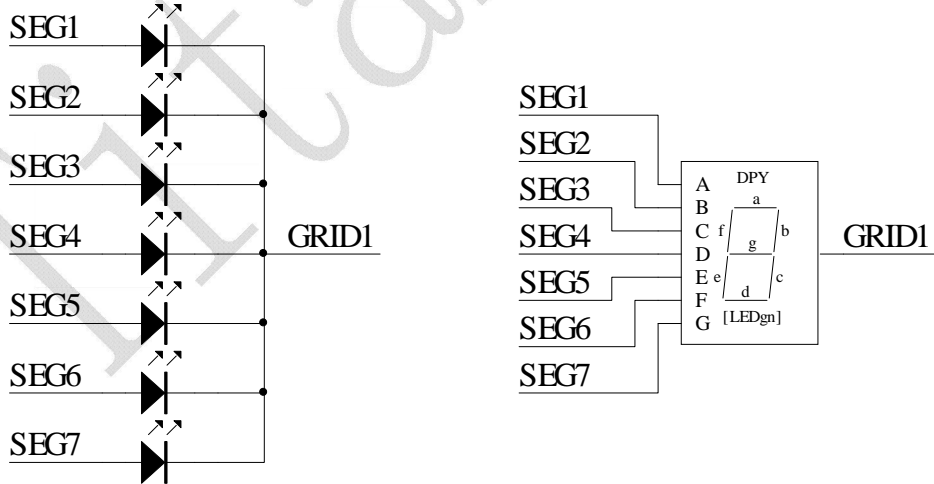


Notice: When read data, set instruction from the 8th rising edge of clock to CLK falling edge to read data that demand a waiting time Twait(min 1 μS).

9. Display and key

(1) Display

1, Driver common cathode:



Chart(7)

Chart(7) is sketch map for common cathode digitron connection, if demand the nixie tube display "0", SEG1, SEG2, SEG3, SEG4, SEG5, SEG6 should be high level, SEG7 is low level when GRID1 is low level.

Please refer to chart(2) display address fom, just write data 3FH in 00H address unit to make nixie tube show "0".

SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	
0	0	1	1	1	1	1	1	00H
B7	B6	B5	B4	B3	B2	B1	B0	

2. Driver common anode nixie tube

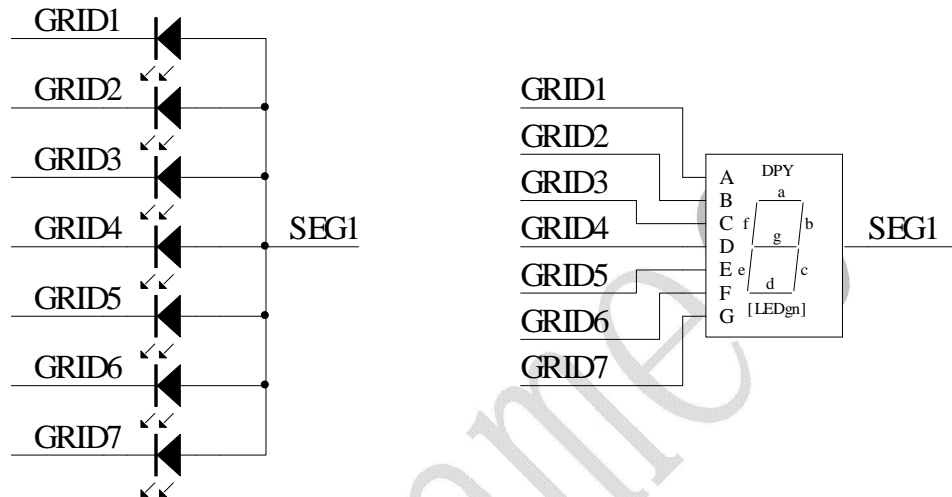


chart (8)

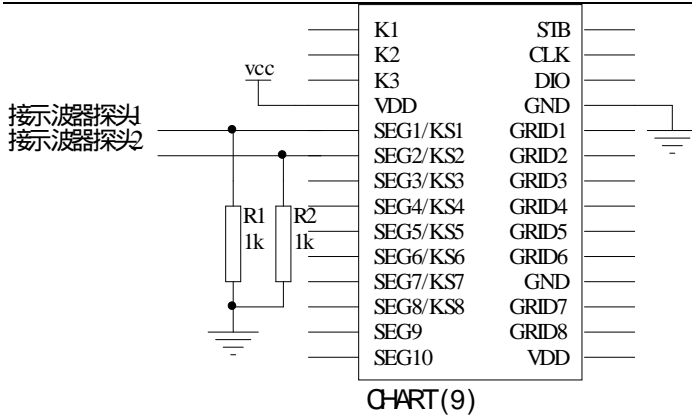
chart(8) is sketch map for common anode digitron connection, if demand the nixie tube display "0", SEG1, SEG2, SEG3, SEG4, SEG5, SEG6 should be high level, SEG7 is low level when GRID1 is low level. Please input 01H into 00H, 02H, 04H, 06H, 08H, 0AH, and input 00H into the rest address unit.

SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	
0	0	0	0	0	0	0	1	00H
0	0	0	0	0	0	0	1	02H
0	0	0	0	0	0	0	1	04H
0	0	0	0	0	0	0	1	06H
0	0	0	0	0	0	0	1	08H
0	0	0	0	0	0	0	1	0AH
0	0	0	0	0	0	0	0	0CH
B7	B6	B5	B4	B3	B2	B1	B0	

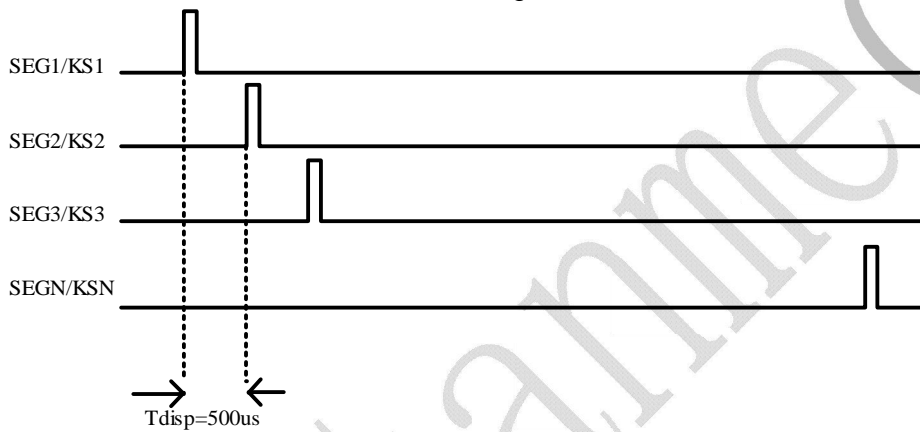
Notice: SEG1-10 is open-drain output, GRID1-10 is N pipe open-drain output, during the use, SEG1 just can connect LED anode, GRID connect cathode.

(2) KEY:

Follow chart(9) to observe SEG1/KS1 and SEG2/KS2, the output key-scan wave as chart(10)

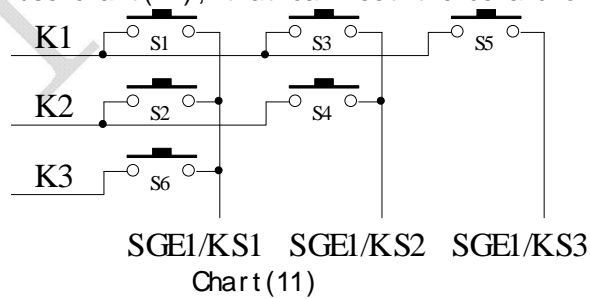


The SEGN/KSN wave of IC board scanning:



Tdisp relate with IC work frequency, TM1638 has been improved many times and oscillation frequency don't entirely same. 500US just for reference, please measure for exact data.

Normal situation please use chart(11), that can meet the demand of key design.



When press S1, BO at the 1st byte read " 1" , if multiple key is pressed, would read multiple " 1"

NOTE: Composite key use notice

SEG1/KS1-SEG10/KS10 is for display and keyscan. chart(12) as example, display demand light D1, light outD2, SEG1 should be " 1" , SEG2 is " 0" , if S1,S2 pressed at the same time,

that equal to SEG1,SEG2 is short circuit, then D1,D2 all light.

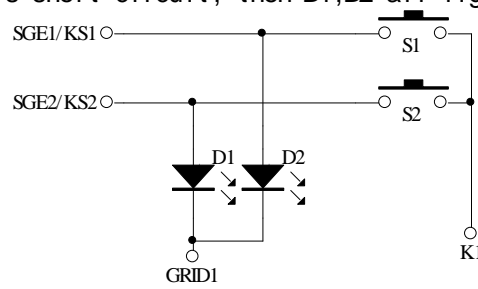
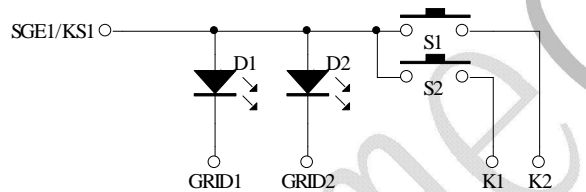


Chart (12)

SOLUTION:

1. in hardware, could set the key need press at the same time to different K-line, as chart(13)



2. Serial resistance in SEG1---SEGN like chart (14), the value of resistance should be 510 , too high will invalid key, too low cannot solve disturb problem.

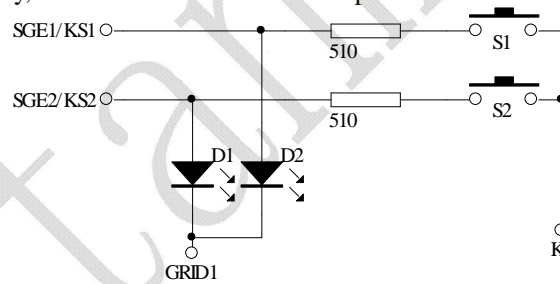


Chart (14)

3. serial connection LED as chart(15)

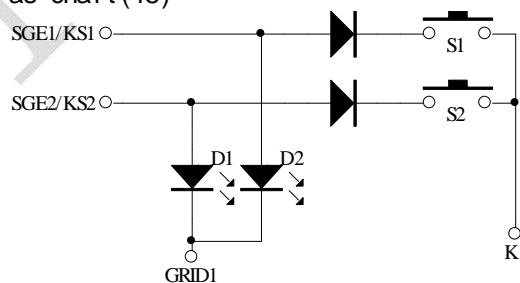


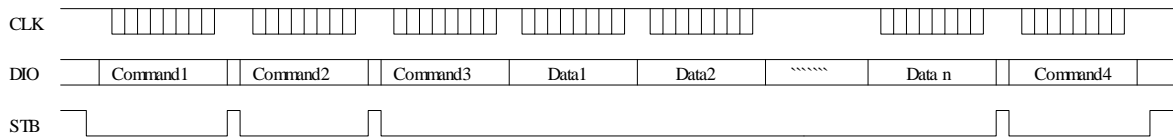
Chart (15)

10. Transmit of serial data when application

10.1 Address add mode

Use address auto- add 1 mode, set address actually is set a original address for stock transmit data. Once send over the original address instruction byte, “ STB” don’ t demand set high and follow closely to transmit data, up to 14BYTE. After send over the data, “ STB”

could be set high.



Command1: set display mode

Command2: set data instruction

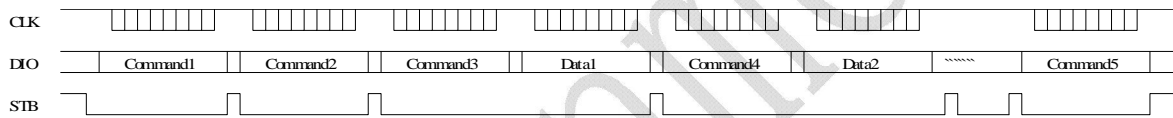
Command3: set display address

Data1-n: transmit display data to Command3 address and behind address(up to 14bytes)

Command4: display control instruction

10.2 fixed address mode

Use fixed address mode, set address actually is set an address for stock demand transmit data. Once send over address, “STB” don’t demand set high, and follow closely to transmit data, After send over the data, “STB” could be set high. Then reset address to stock the 2ed data, up to 16byte is send over, “STB” set high.



Command1: set display mode

Command2: set data instruction

Command3: set display address 1

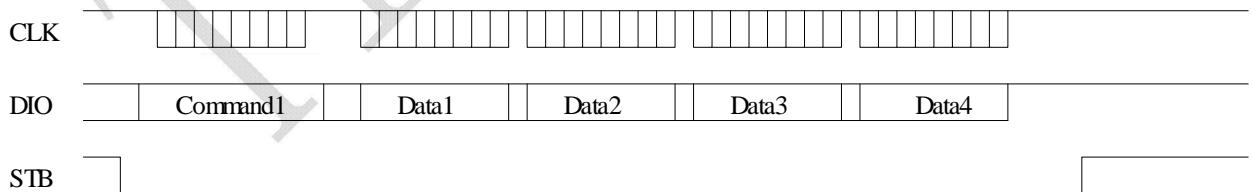
Data1: transmit display data1 to command3 address

Command4: set display address2

Data2: transmit display data2 to command4 address

Command5: display control instruction

10.3 Read key timing

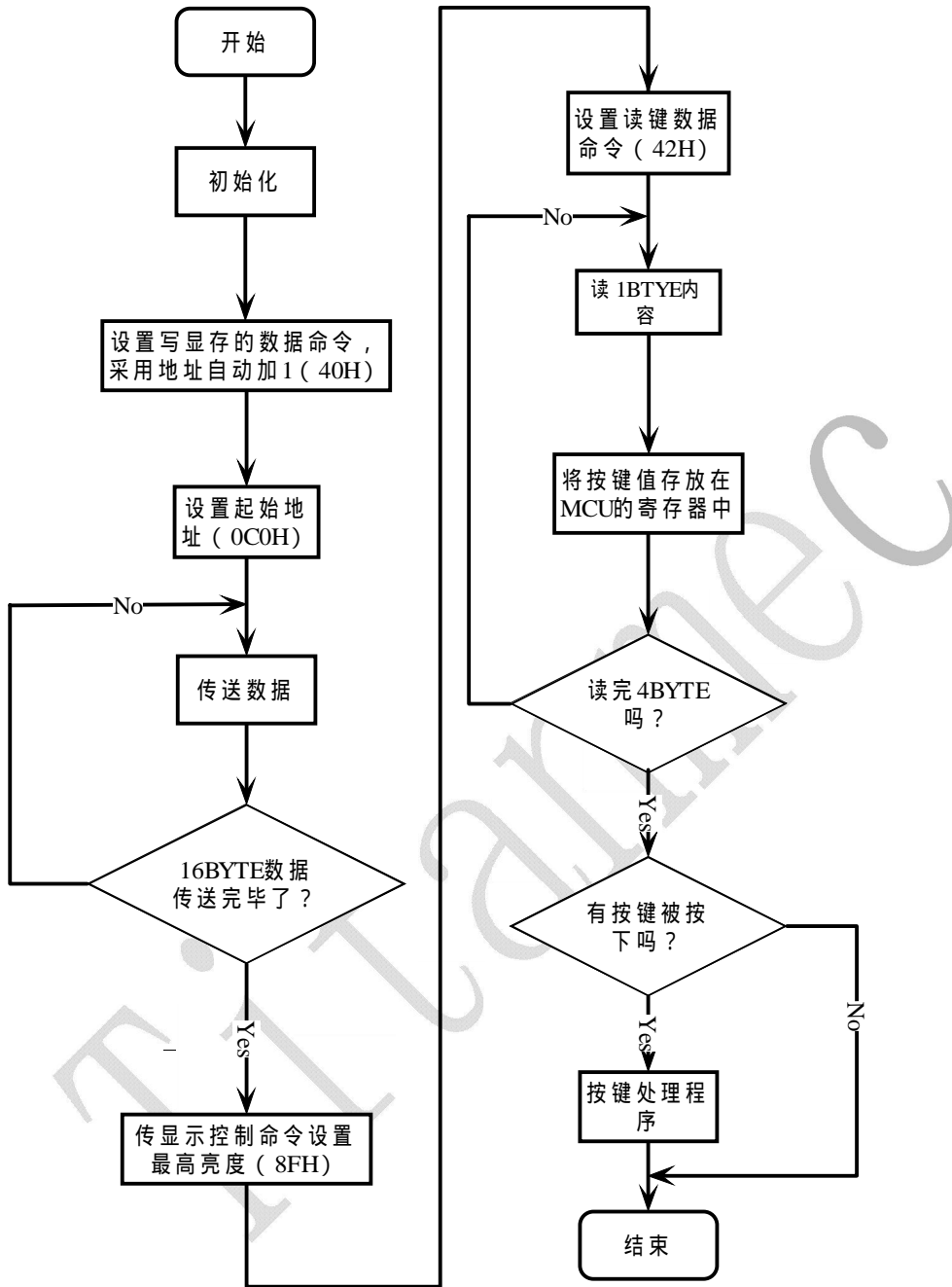


Command1: set display mode

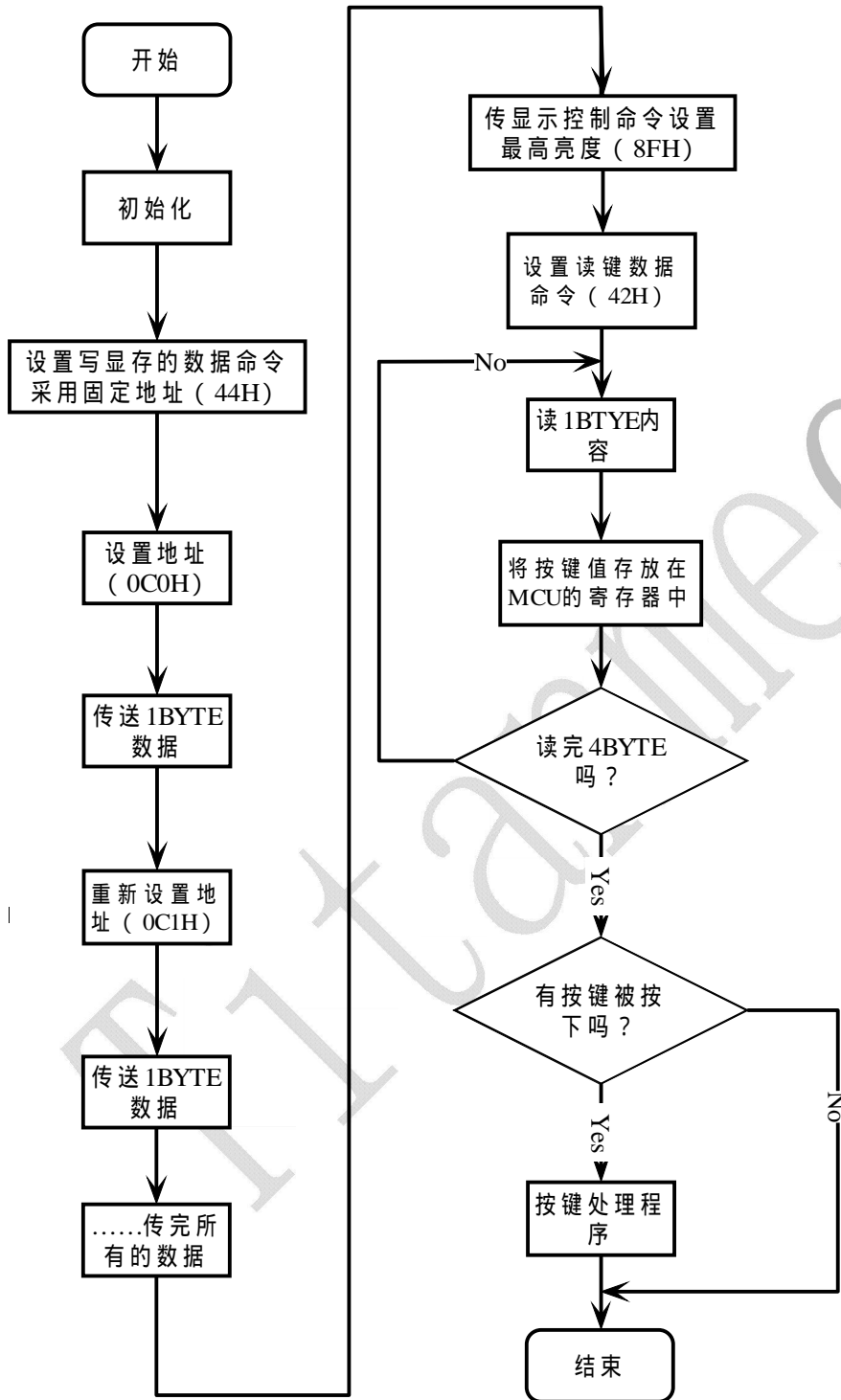
Data1-4: read key data

10.4 procedure design flow chart

procedure design flow chart for address auto-add1

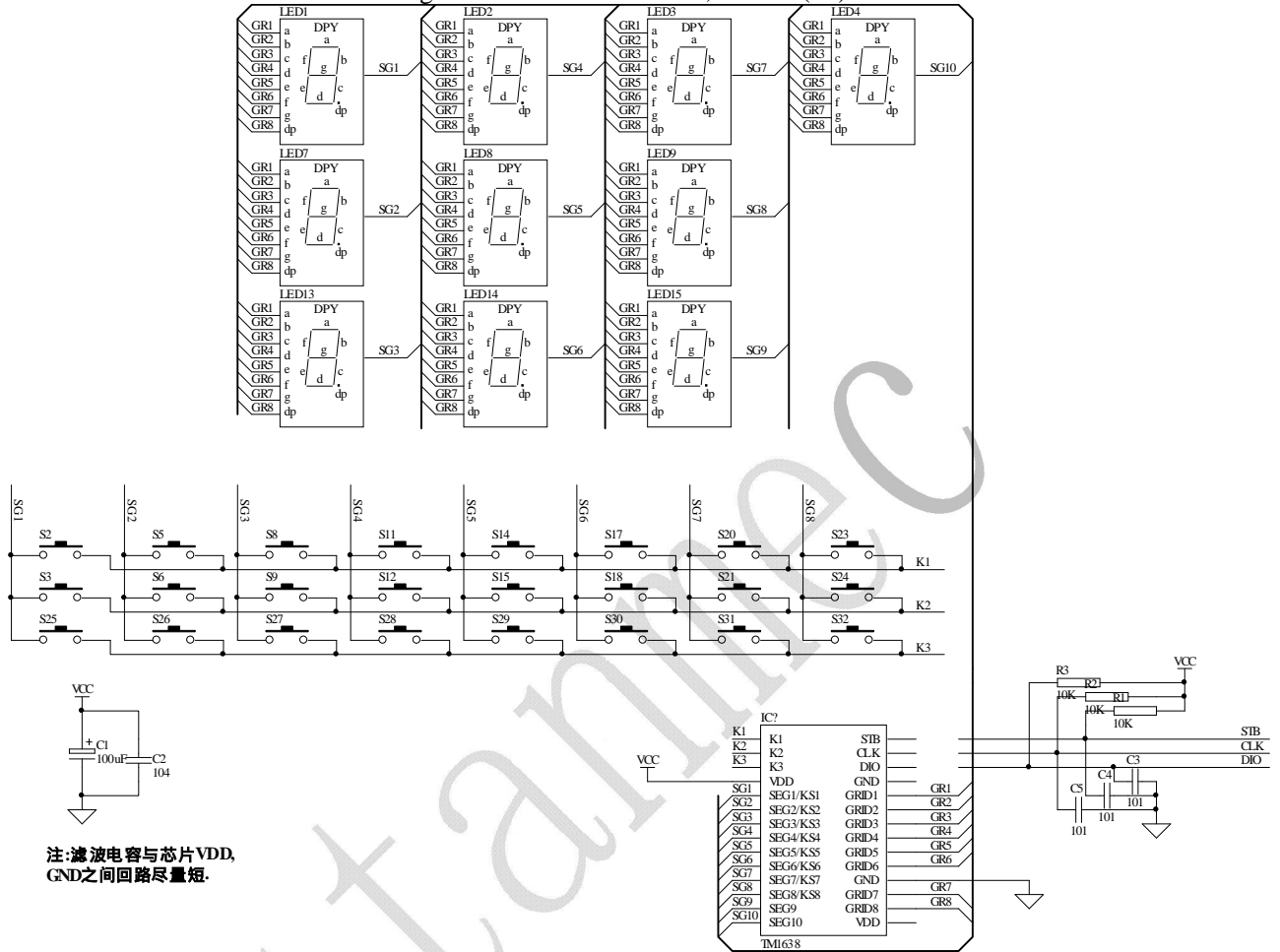


Procedure design flow chart for fixed address



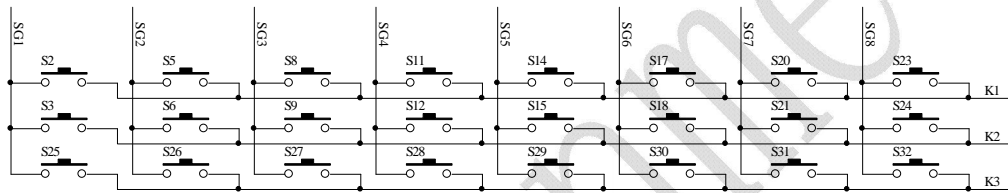
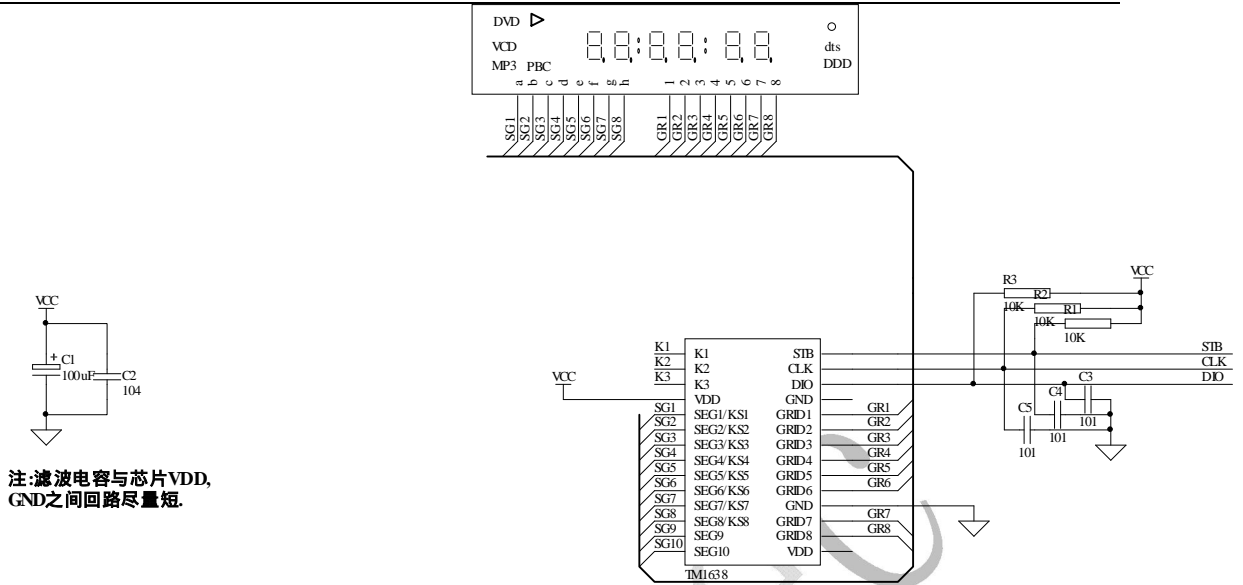
11. Application circuit

11.1 TM1638 driver common anode digit screen hardware circuit, as chart(16):



Chart(16)

11.2 TM1638 Driver common cathode digit screen hardware circuit, as chart(17):



Chart(17)

- Notice:**
1. the filter capacity between VDD and GND should near TM1638 chip when PCB layout to enhance filter effort.
 2. The 3 100p capacity connect DIO, CLK, STB port could reduce the interference to communication port.
 3. because the break-over reduce voltage of blue-ray digitron about 3V, TM1638 supply electronic should choose 5V.

12. Electric parameter

Limit parameter ($T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{V}$)

Parameter	Symbol	Range	Unit
Logic power voltage	VDD	-0.5 ~ +7.0	V
Logic input voltage	VI1	-0.5 ~ VDD + 0.5	V
LED Seg driver output current	IO1	-50	mA
LED Grid driver output current	IO2	+200	mA
Power consumption	PD	400	mW

Wbrk temperature	Topt	-40 ~ +80	
Stock temperature	Tstg	-65 ~ +150	

Normal work range($T_a = -20 \sim +70$, $V_{ss} = 0$ V)

Parameter	Symbol	Min	Typical	Max	Unit	Test condition
Logic power voltage	VDD		5		V	-
High level input voltage	VIH	0.7 VDD	-	VDD	V	-
High level input voltage	VIL	0	-	0.3 VDD	V	-

Electric feature($T_a = -20 \sim +70$, $V_{DD} = 4.5 \sim 5.5$ V, $V_{ss} = 0$ V

Parameter	Symbol	Min	Typical	Max	Unit	Test condition
High level output current	Ioh1	-20	-25	-40	mA	Seg1~Seg11, $V_o = v_{dd}-2V$
	Ioh2	-20	-30	-50	mA	Seg1~Seg11, $V_o = v_{dd}-3V$
Low level output current	ICL1	80	140	-	mA	Grid1~Grid6 $V_o=0.3V$
Low level output current	Idout	4	-	-	mA	$V_O = 0.4V$, dout
Capacity for high level output current	ItoIsg	-	-	5	%	$V_O = V_{DD} - 3V$, Seg1~ Seg11
Output falling resistance	RL		10		K	K1-K3
Input current	II	-	-	± 1	μ A	$V_I = V_{DD} / V_{SS}$
High level input voltage	VIH	0.7 VDD	-		V	CLK, DIN, STB
Low level input voltage	VIL	-	-	0.3 VDD	V	CLK, DIN, STB
Delay voltage	VH	-	0.35	-	V	CLK, DIN, STB

Active current consumption	IDDdyn	-	-	5	mA	No load, show turn-off
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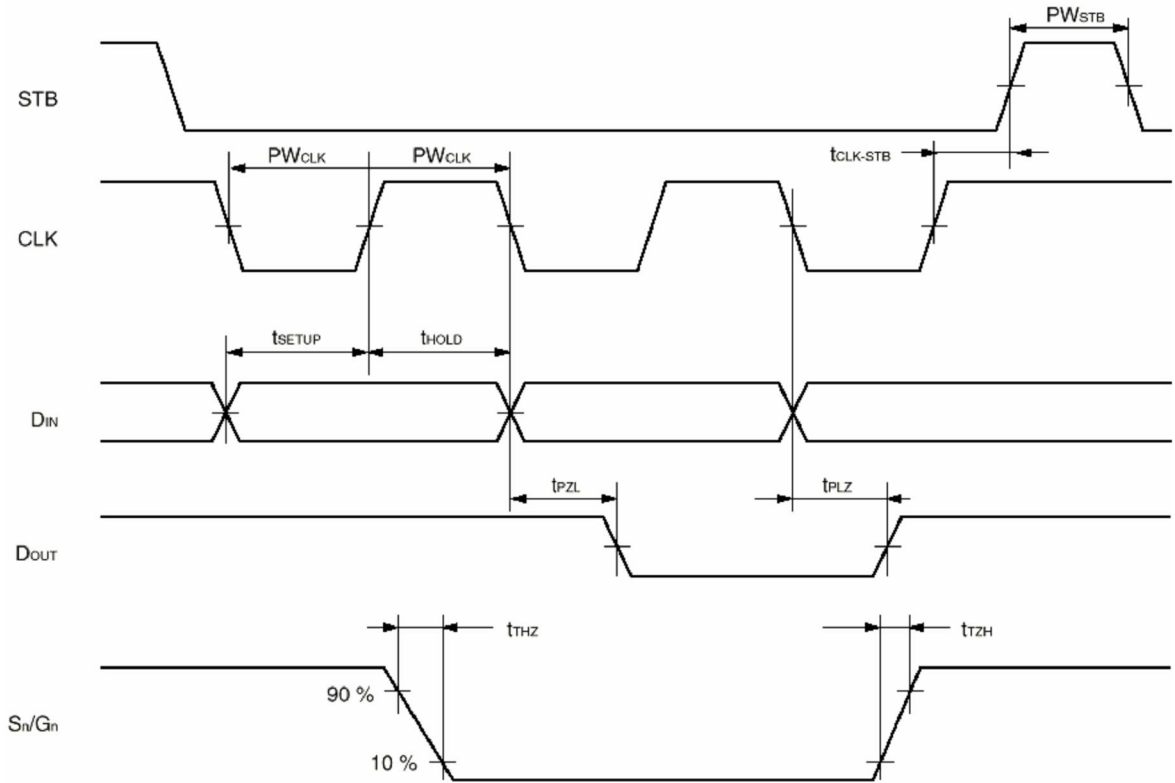
Switch feature(Ta = -20 ~ +70 , VDD = 4.5 ~ 5.5 V)

Parameter	Symbol	Min	Typical	Max	Unit	Test condition
Oscillation	fosc	-	500	-	KHz	R = 16.5 K
Transmit delay time	tPLZ	-	-	300	ns	CLK DOUT
	tPZL	-	-	100	ns	CL = 15pF, RL = 10K
Rising time	TTZH 1	-	-	2	μ s	Seg1~ Seg11
	TTZH 2	-	-	0.5	μ s	CL = 300p F Grid1~ Grid4 Seg12/Grid7~ Seg14/Grid5
Falling time	TTHZ	-	-	120	μ s	CL = 300pF, Segn, Gridn
Max clock frequency	Fmax	1	-	-	MHz	Duty ratio 50%
Input capacity	CI	-	-	15	pF	-

Timing feature (Ta = -20 ~ +70 , VDD = 4.5 ~ 5.5 V)

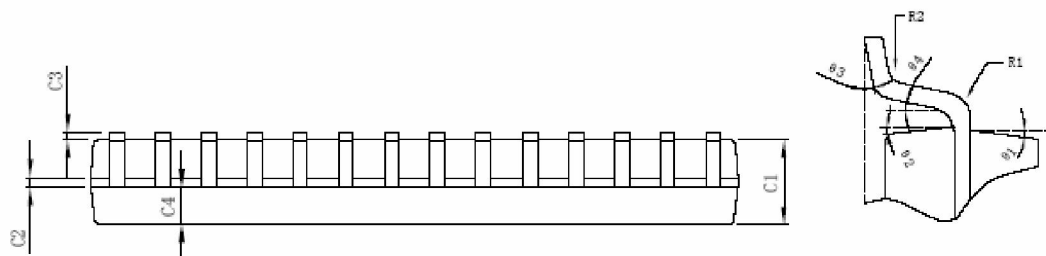
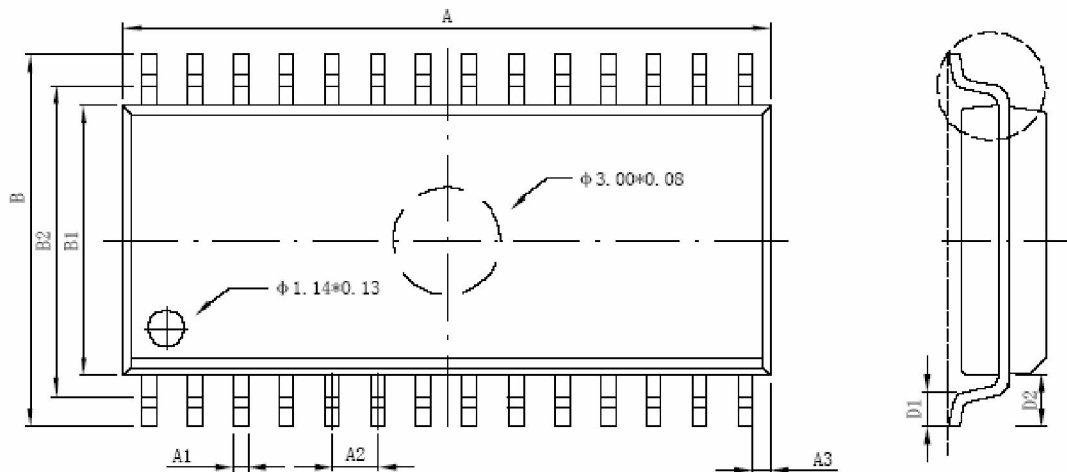
Parameter	Symbol	Min	Typical	Max	Unit	Test condition
Clock pulsewidth	PWCLK	400	-	-	ns	-
Gate pulse width	PWSTB	1	-	-	μ s	-
Data building time	tSETUP	100	-	-	ns	-
Data stock time	tHOLD	100	-	-	ns	-
CLK STB time	tCLK STB	1	-	-	μ s	CLK STB
Waiting time	tWAIT	1	-	-	μ s	CLK CLK

Timing wave chart:



13.Package Size

尺寸 标注	最小 (mm)	最大 (mm)	尺寸 标注	最小 (mm)	最大 (mm)
A	17.83	18.03	C4	1.043TYP	
A1	0.4064TYP		D1	0.70	0.90
A2	1.27TYP		D2	1.395TYP	
A3	0.51TYP		R1	0.508TYP	
B	9.90	10.50	R2	0.508TYP	
B1	7.42	7.62	θ 1	7° TYP	
B2	8.9TYP		θ 2	5° TYP	
C1	2.24	2.44	θ 3	4° TYP	
C2	0.204	0.33	θ 4	10° TYP	
C3	0.10	0.25			



DETAIL "X"