



# **Specification**

**For**

**LCD Module**

**TS2040-1**



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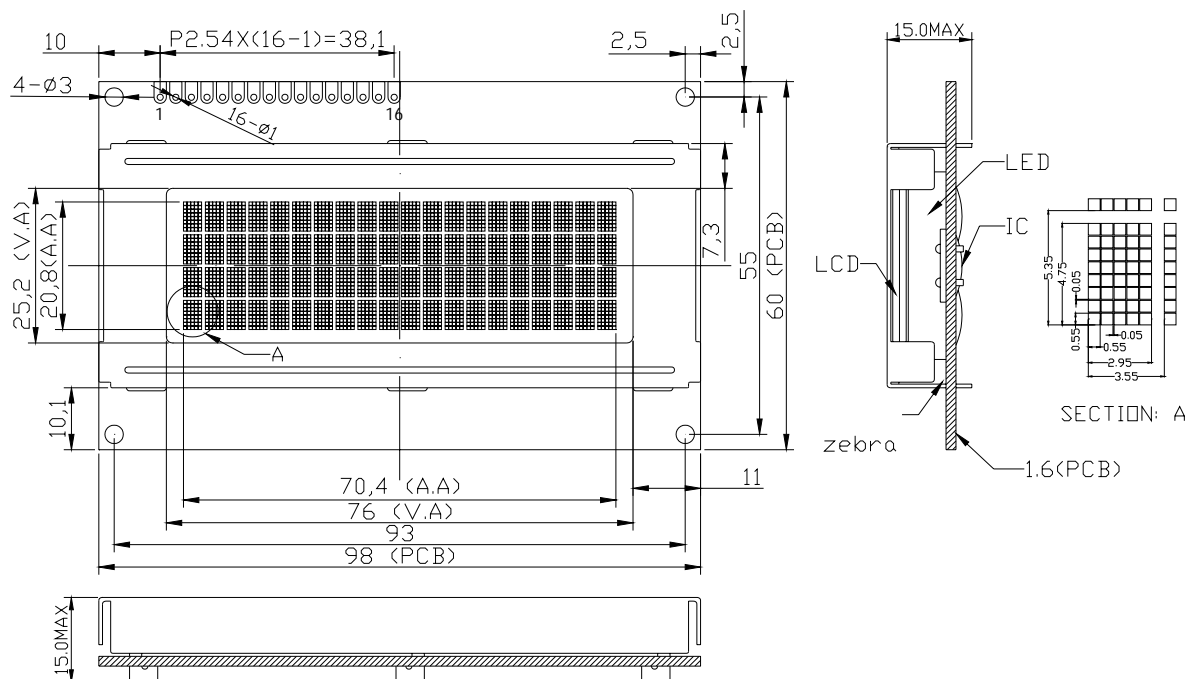
## 1.0 INTRODUCTION

This USER'S MANUAL is introduced the outside dimensions, optical characteristics, electrical characteristics, interface, controller commands, etc. of the custom design LCD module.

## 1.1 FEATURE

- (1) Display mode: STN POSITIVE, TRANSFLECTIVE, YELLOW-GREEN COLOR
- (2) Display format: 20 characters X 4 line
- (3) Driving method: 1/16 Duty, 1/5 Bias
- (4) Viewing direction: 6 o'clock
- (5) Control IC: ST7066U-0A ST7065C
- (6) Interface Input Data : 4-Bits or 8-Bits interface available
- (7) Back light: LED (Yellow-Green )

## 2.0 DIMENSION DIAGRAM





### 3.0 MECHANICAL SPECIFICATIONS

ITEM	STANDARD VALUE	UNIT
DOTS	5X8	characters -
DOT SIZE	0.55X0.55	mm
DOT PITCH	0.60X0.60	mm
MODULE DIMENSION	98.0(W) × 60.0(H) × 1.6(T)	mm
EFFECTIVE DISPLAY AREA	84.0(W) × 31.0(H)MIN	mm

### 4.0 MAX STANDARD VALUE

ITEM	SYMBOL	MIN.	TYPE	MAX	UNIT
OPERATING TEMPERATURE	Top	-10	25	60	
STORAGE TEMPERATURE	Tst	-20	/	70	
INPUT VOLTAGE	VI	VSS	/	VDD	V
SUPPLY VOLTAGE FOR LOGIC	VDD-VSS	-0.3	/	7.0	V
SUPPLY VOLTAGE FOR LCD	VDD-V0	VDD-10.0	/	VDD+0.3	V

### 5.0 ELECTRICAL CHARACTERISTICS

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
SUPPLY VOLTAGE FOR LOGIC	$V_{DD}-V_{SS}$	Ta = 25 °C	2.7	5.0	5.5	V

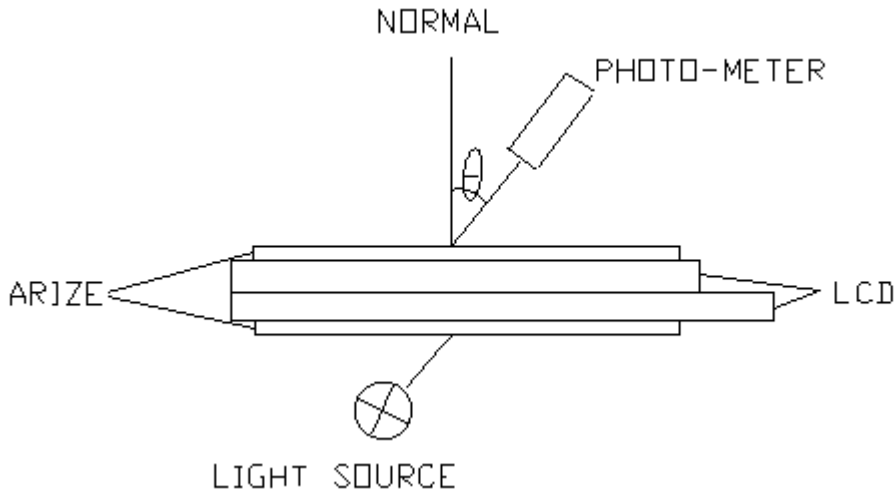


SUPPLY VOLTAGE FOR LCD	$V_{DD}-V_O$ ( $V_{OP}$ )	$T_a = 25\text{ }^\circ\text{C}$	3.0	5.0	10.0	V
INPUT HIGH VOL.	$V_{IH}$	$T_a = 25\text{ }^\circ\text{C}$	0.7VDD	-	VDD	V
INPUT LOW VOL.	$V_{IL}$	$T_a = 25\text{ }^\circ\text{C}$	-0.3	-	0.6	V
OUTPUT HIGH VOL.	$V_{OH}$	$T_a = 25\text{ }^\circ\text{C}$	0.75VDD	-	-	V
OUTPUT LOW VOL.	$V_{OL}$	$T_a = 25\text{ }^\circ\text{C}$	-	-	0.2VDD	V
SUPPLY CURRENT	$I_{DD}$	$V_{DD} = 3.0\text{V}$	-	0.1	0.25	mA

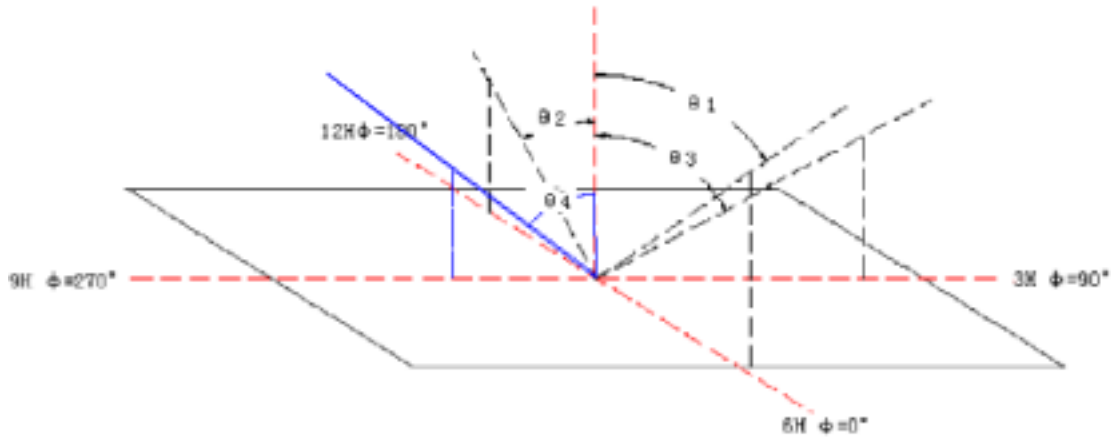
## 6.0 OPTICAL CHARACTERISTICS

No	Item	Symbol	Measurement temperature	MIN.	TYP.	MAX.	Unit	
1	Contrast Ratio	Cr	25	2.60	3.17			
2	Response Time	Rise time	Tr	25	-	-	0.2	us
		Fall time	Tf	25	-	-	0.2	us
3	Viewing Angle	$6H, =0\text{ }^\circ$	1	25	55			Deg.
		$12H, =180$	2	25	0			Deg.
		$=90\text{ }^\circ$	3	25	45			Deg.
		$=270$	4	25	45			Deg.
4	Frame Frequency		25	190	270	350	Hz	

## 6.1 OPTICAL MEASUREMENT SYSTEM



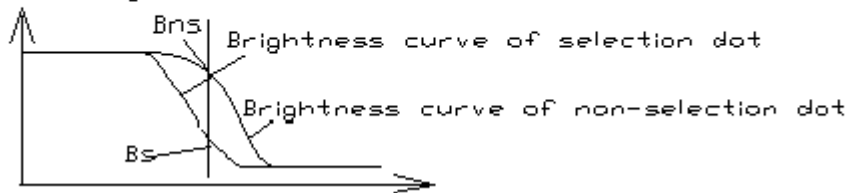
### 6.2 DEFINITION OF $\theta$ AND $\phi$



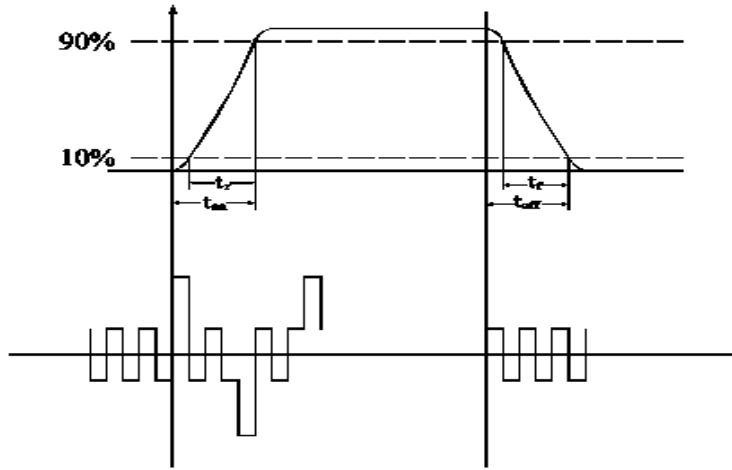
### 6.3 DEFINITION OF CONTRAST RATIO $C_r$

DEFINITION:

$$C_r = \frac{\text{Brightness of non-selection dot (} b_{ns} \text{)}}{\text{Brightness of selection dot (} b_s \text{)}}$$



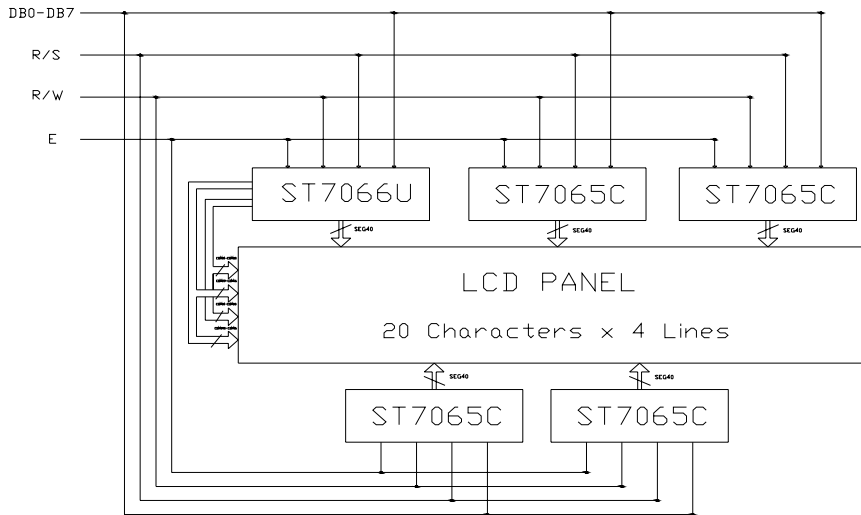
### 6.4 DEFINITION OF OPTICAL RESPONSE TIME



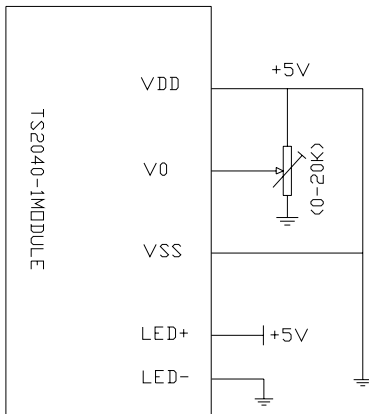
### 7.0 INTERFACE PIN FUNCTION DESCRIPTION

PIN NO	SYMBOL	FUNCTION
1	VSS	Power Ground
2	VDD	Power supply for logic circuit (+5V)
3	V0	For LCD drive voltage (variable)
4	RS(C/D)	H: Display Data, L:Display Instruction
5	R/W	H: Data Read (LCM to MPU) ; L: Data Write (MPU to LCM)
6	E	Enable signal .  Write mode (R/W = L) data of DB<0: 7> is latched at the falling edge of E.  Read mode (R/W = H) DB<0: 7> appears the reading data while E is at high level
7-14	DB0-DB7	Data bus. There state I/O common terminal.
15	A	Power for LED Backlight (+5V)
16	K	Power for LED Backlight (Ground)

### 8.0 BLOCK DIAGRAM



## 8.1 POWER SUPPLY BLOCK DIAGRAM



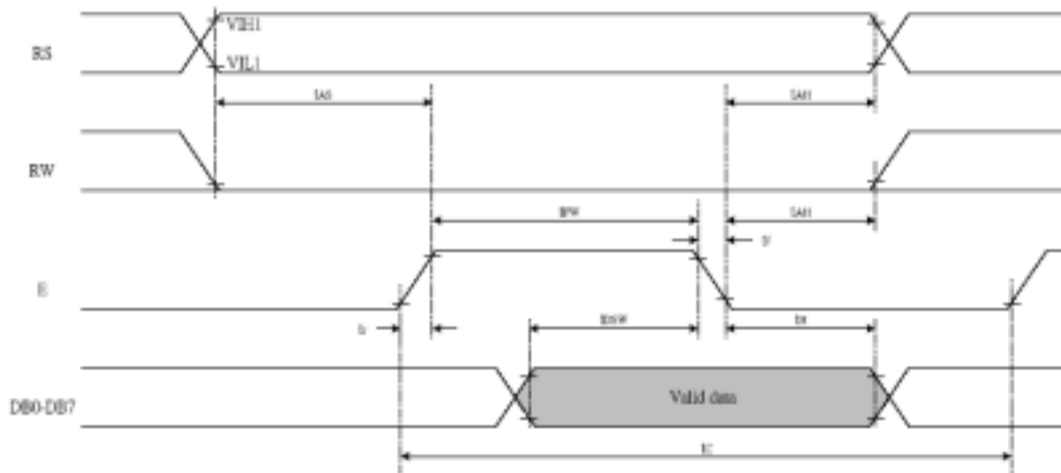
## 9.0 TIMING CHARACTERISTICS





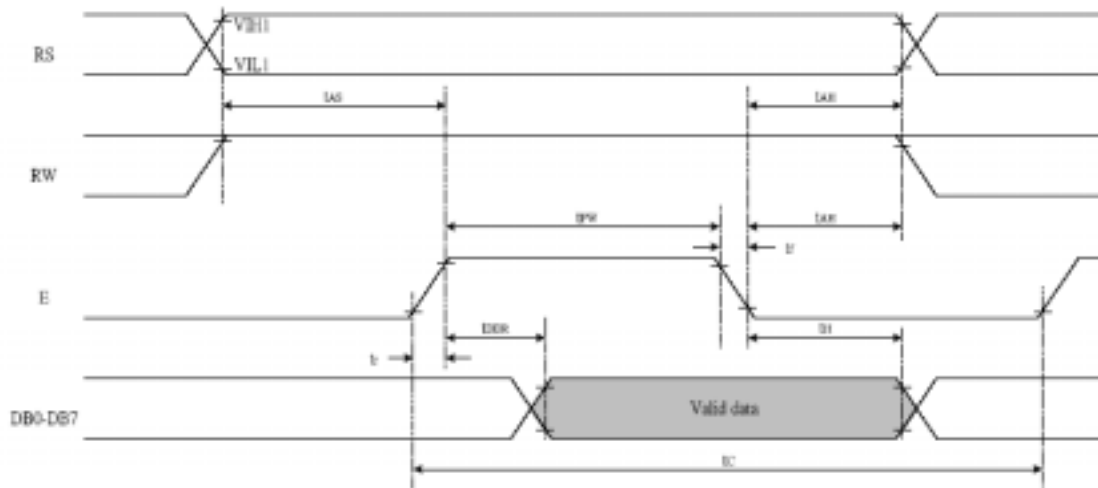
Write Mode (Writing data from MPU to ST7066U)						
T <sub>C</sub>	Enable Cycle Time	Pin E	1200	-	-	ns
T <sub>PW</sub>	Enable Pulse Width	Pin E	140	-	-	ns
T <sub>R</sub> ,T <sub>F</sub>	Enable Rise/Fall Time	Pin E	-	-	25	ns
T <sub>AS</sub>	Address Setup Time	Pins: RS,RW,E	0	-	-	ns
T <sub>AH</sub>	Address Hold Time	Pins: RS,RW,E	10	-	-	ns
T <sub>DSW</sub>	Data Setup Time	Pins: DB0 - DB7	40	-	-	ns
T <sub>H</sub>	Data Hold Time	Pins: DB0 - DB7	10	-	-	ns
Read Mode (Reading Data from ST7066U to MPU)						
T <sub>C</sub>	Enable Cycle Time	Pin E	1200	-	-	ns
T <sub>PW</sub>	Enable Pulse Width	Pin E	140	-	-	ns
T <sub>R</sub> ,T <sub>F</sub>	Enable Rise/Fall Time	Pin E	-	-	25	ns
T <sub>AS</sub>	Address Setup Time	Pins: RS,RW,E	0	-	-	ns
T <sub>AH</sub>	Address Hold Time	Pins: RS,RW,E	10	-	-	ns
T <sub>DDR</sub>	Data Setup Time	Pins: DB0 - DB7	-	-	100	ns
T <sub>H</sub>	Data Hold Time	Pins: DB0 - DB7	10	-	-	ns

● Writing data from MPU to ST7066U





● Reading data from ST7066U to MPU



### 10.0 Display control instruction

The display control instructions control the internal state of the ST7066U-0A. Instruction is received from MPU to ST7066U-0A for the display control. The following table shows various instructions.

There are four categories of instructions that:

- Designate ST7066U functions, such as display format, data length, etc.
- Set internal RAM addresses
- Perform data transfer with internal RAM
- Others

Instruction Table:

Instruction	Instruction Code										Description	Description Time (270KHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM, and set DDRAM address to "00H" from AC	1.52 ms
Return Home	0	0	0	0	0	0	0	0	1	x	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.52 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	37 us
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	D=1:entire display on C=1:cursor on B=1:cursor position on	37 us
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	x	x	Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	37 us



Function Set	0	0	0	0	1	DL	N	F	x	x	DL:interface data is 8/4 bits N:number of line is 2/1 F:font size is 5x11/5x8	37 us
Set CGRAM address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter	37 us
Set DDRAM address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	37 us
Read Busy flag and address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0 us
Write data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM)	37 us
Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM)	37 us

Note:

Be sure the ST7066U is not in the busy state (BF = 0) before sending an instruction from the MPU to the ST7066U. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to Instruction Table for the list of each instruction execution time.

## ■ Instruction Description

### ● Clear Display

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

### ● Return Home

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	1	x

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change.

### ● Entry Mode Set

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	1	I/D	S

Set the moving direction of cursor and display.



- **I/D : Increment / decrement of DDRAM address (cursor or blink)**  
 When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.  
 When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.  
 \* CGRAM operates the same as DDRAM, when read from or write to CGRAM.
- **S: Shift of entire display**  
 When DDRAM read (CGRAM read/write) operation or S = "Low", shift of entire display is not performed. If  
 S = "High" and DDRAM write operation, shift of entire display is performed according to I/D value (I/D =  
 "1" : shift left, I/D = "0" : shift right).

S	I/D	Description
H	H	Shift the display to the left
H	L	Shift the display to the right

- **Display ON/OFF**



Control display/cursor/blink ON/OFF 1 bit register.

- **D : Display ON/OFF control bit**  
 When D = "High", entire display is turned on.  
 When D = "Low", display is turned off, but display data is remained in DDRAM.
- **C : Cursor ON/OFF control bit**  
 When C = "High", cursor is turned on.  
 When C = "Low", cursor is disappeared in current display, but I/D register remains its data.
- **B : Cursor Blink ON/OFF control bit**  
 When B = "High", cursor blink is on, that performs alternate between all the high data and display  
 character at the cursor position.  
 When B = "Low", blink is off.

- **Cursor or Display Shift**



Without writing or reading of display data, shift right/left cursor position or display. This instruction is used to correct or search display data. During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line. Note that display shift is performed simultaneously in all the line. When displayed data is shifted repeatedly, each line shifted individually. When display shift is performed, the contents of address counter are not changed.

S/C	R/L	Description	AC Value
L	L	Shift cursor to the left	AC=AC-1
L	H	Shift cursor to the right	AC=AC+1
H	L	Shift display to the left. Cursor follows the display shift	AC=AC
H	H	Shift display to the right. Cursor follows the display shift	AC=AC



● **Function Set**

RS RW DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0

Code	0	0	0	0	1	DL	N	F	x	x
------	---	---	---	---	---	----	---	---	---	---

- **DL : Interface data length control bit**  
 When DL = "High", it means 8-bit bus mode with MPU.  
 When DL = "Low", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode.  
 When 4-bit bus mode, it needs to transfer 4-bit data by two times.
- **N : Display line number control bit**  
 When N = "Low", it means 1-line display mode.  
 When N = "High", 2-line display mode is set.
- **F : Display font type control bit**  
 When F = "Low", it means 5 x 8 dots format display mode  
 When F = "High", 5 x 11 dots format display mode.

N	F	No. of Display Lines	Character Font	Duty Factor
L	L	1	5x8	1/8
L	H	1	5x11	1/11
H	x	2	5x8	1/16

● **Set CGRAM Address**

RS RW DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0

Code	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0
------	---	---	---	---	-----	-----	-----	-----	-----	-----

Set CGRAM address to AC.  
This instruction makes CGRAM data available from MPU.

● **Set DDRAM Address**

RS RW DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0

Code	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0
------	---	---	---	-----	-----	-----	-----	-----	-----	-----

Set DDRAM address to AC.  
This instruction makes DDRAM data available from MPU.  
When 1-line display mode (N = 0), DDRAM address is from "00H" to "4FH".  
In 2-line display mode (N = 1), DDRAM address in the 1st line is from "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".

● **Read Busy Flag and Address**

RS RW DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0

Code	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0
------	---	---	----	-----	-----	-----	-----	-----	-----	-----

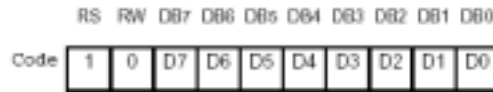


When BF = "High", indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted.

The address Counter (AC) stores DDRAM/CGRAM addresses, transferred from IR.

After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1.

● **Write Data to CGRAM or DDRAM**

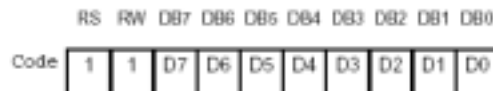


Write binary 8-bit data to DDRAM/CGRAM.

The selection of RAM from DDRAM, CGRAM, is set by the previous address set instruction : DDRAM address set, CGRAM address set. RAM set instruction can also determine the AC direction to RAM.

After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

● **Read Data from CGRAM or DDRAM**



Read binary 8-bit data from DDRAM/CGRAM.

The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data.

In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction : it also transfer RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.

\* In case of RAM write operation, after this AC is increased/decreased by 1 like read operation. In this time, AC indicates the next address position, but you can read only the previous data by read instruction.