PlanAhead Design and Analysis Tool

A faster, more efficient design solution to help achieve your performance goals.

PlanAhead™ offers an RTL to bit stream design flow with new and improved user interface and project management capabilities. With PlanAhead software, you can view implementation and timing results to easily analyze critical logic, and make targeted decisions to improve design performance with floorplanning, constraint modification, and many Synthesis and Implmentation settings. It helps you make tradeoffs between RTL Coding and Synthesis and Implementation, with extensive design exploration and analysis features.

With convenient access through integration with the ISE Project Navigator, PlanAhead software extends the methodology of the logic design flow to help you get the most out of your design through floorplanning, multiple implementation runs, hierarchy exploration, quick timing analysis, and block based implementation.

PlanAhead software also provides an easy and convenient method of creating & inserting the ChipScope™ Pro debug cores to simplify the process of on-chip verification.

Design Entry for RTL, IP, EDK and DSP Designs	Provides a comprehensive cockpit for creating and verifying RTL designs in either Verilog or VHDL, including access to the Xilinx IP catalog through CORE Generator integration. PlanAhead includes an RTL technology view, where a fast elaboration of RTL sources will yield access to a schematic view, resource and power estimation. Management of synthesis runs is achieved through integration with XST. Offers integration with Xilinx Platform Studio (XPS) and System Generator for DSP designs. Create and add XPS and DSP subsystems to a project through the .xmp and .sgp source type. Integration support also includes importing and converting ISE® tools projects to PlanAhead design tool projects and generating files from the XPS tool appropriately in the synthesis and implementation flow tools.
Design Verification	Integrated with ISE Simulator to perform behavioral and functional verification of HDL code and IP at various stages of the design. PlanAhead also allows you to choose Mentor Graphics simulators as the target simulator in the project settings, enabling multiple simulation filesets with their own sets of properties. Simultaneously create and maintain multiple simulation configurations which could vary in areas such as the testbench being used or other simulation properties.

Simplified Pin Planning	Provides features to help you simplify the complexities of pin assignments with an environment for fully automatic or semi-automated assignment of I/O ports to physical Package Pins.
Synthesis and Implementation Management	Includes an exploration tool to help with experimentation of HDL, tool options, and floorplanning trials to achieve design closure. By managing multiple runs, PlanAhead allows you to execute multiple trials based on strategies the user defines or predefined strategies shipped as factory defaults. In a Linux environment, PlanAhead software provides the ability to execute runs in parallel on remote hosts.
Design Analysis and Floorplanning	Provides extensive capabilities to help designers achieve design closure. This includes a GUI with comprehensive cross-probing to analyze your designs and track issues such as timing violations and DRCs and then trace them back to schematics, netlists and constraints. This allows designers to experiment with physical constraints such as pblocks (area groups) and location constraints for cell instances.
Design Debug	Provides integration with ChipScope Pro and provides the ability to insert logic which works in conjunction with the ChipScope Analyzer tool to facilitate logic analysis and debug in the lab when your design is running on a device.
Hierarchical Design Methodology	Provides the graphical user interface to control hierarchical design flows for the ISE implementation tools, including support for the Design Preservation and Team Based Design flows. The Design Preservation Flows allow users to implement critical portions of their design and then “preserve” them while iterating on other portions of the design, which ensures that critical logic is not perturbed by further logic development. Team Based Design builds on Design Preservation flow to allow parallel implementation of modules by separate members of a design team, with integration and assembly of the top level performed by other individuals.
Signal Integrity	Includes functionality allowing users to analyze pinouts for Simultaneous Switching Noise (SSN) or Weighted Average Simultaneous Switching Output (WASSO), based on device family. This allows designers to more easily limit the amount of ground bounce present immediately at the output of the

	FPGA and prevent corruption of the operation of other devices driven by the FPGA.
Timing Analysis	Includes a flexible, integrated timing analyzer allowing you to estimate route delays before running place and route. This capability can be used in various modes during different stages of design completion. It can provide early estimations of path delays to assist during floorplanning, as well as for detailed path tracing, debugging and constraint assignment.