

# 1M x 16 Static RAM

## Features

- **High speed**
  - $t_{AA} = 10 \text{ ns}$
- **Low active power**
  - 990 mW (max.)
- **Operating voltages of  $3.3 \pm 0.3\text{V}$**
- **2.0V data retention**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with  $\overline{CE}_1$  and  $\overline{CE}_2$  features**
- **Available in Pb-free and non Pb-free 54-pin TSOP II package and non Pb-free 60-ball fine-pitch ball grid array (FBGA) package**

## Functional Description

The CY7C1061AV33 is a high-performance CMOS Static RAM organized as 1,048,576 words by 16 bits.

Writing to the device is accomplished by enabling the chip ( $\overline{CE}_1$  LOW and  $\overline{CE}_2$  HIGH) while forcing the Write Enable

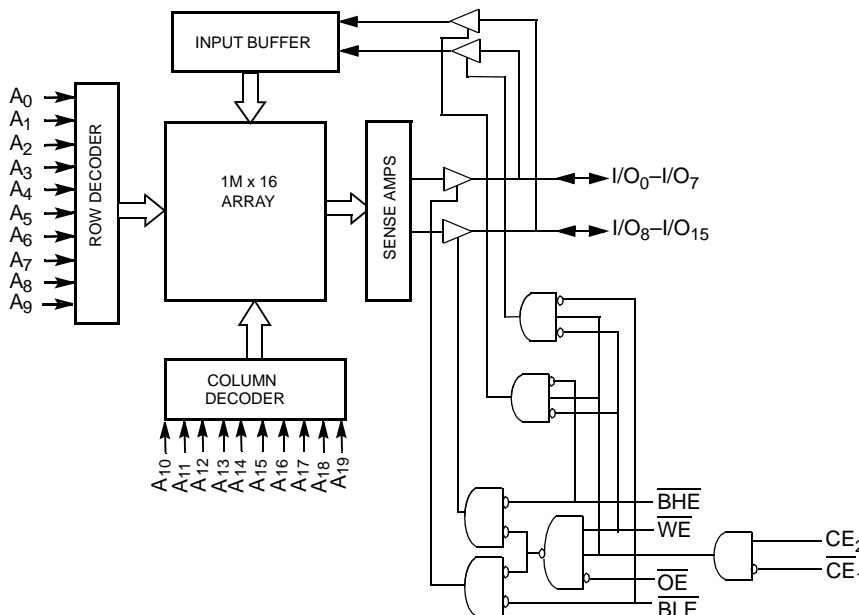
( $\overline{WE}$ ) input LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins ( $I/O_0$  through  $I/O_7$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{19}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins ( $I/O_8$  through  $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{19}$ ).

Reading from the device is accomplished by enabling the chip by taking  $\overline{CE}_1$  LOW and  $\overline{CE}_2$  HIGH while forcing the Output Enable ( $\overline{OE}$ ) LOW and the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $I/O_0$  to  $I/O_7$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on  $I/O_8$  to  $I/O_{15}$ . See the truth table at the back of this data sheet for a complete description of Read and Write modes.

The input/output pins ( $I/O_0$  through  $I/O_{15}$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}_1$  HIGH/ $\overline{CE}_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), the  $\overline{BHE}$  and  $\overline{BLE}$  are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a Write operation ( $\overline{CE}_1$  LOW,  $\overline{CE}_2$  HIGH, and  $\overline{WE}$  LOW).

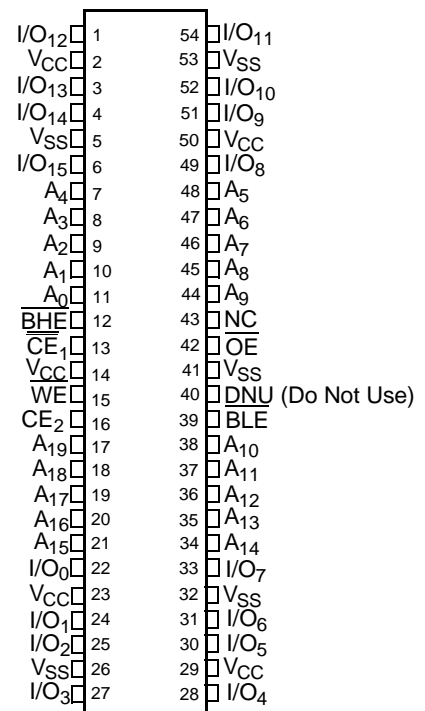
The CY7C1061AV33 is available in a 54-pin TSOP II package with center power and ground (revolutionary) pinout, and a 60-ball fine-pitch ball grid array (FBGA) package.

## Logic Block Diagram



## Pin Configurations<sup>[1, 2]</sup>

### TSOP II (Top View)



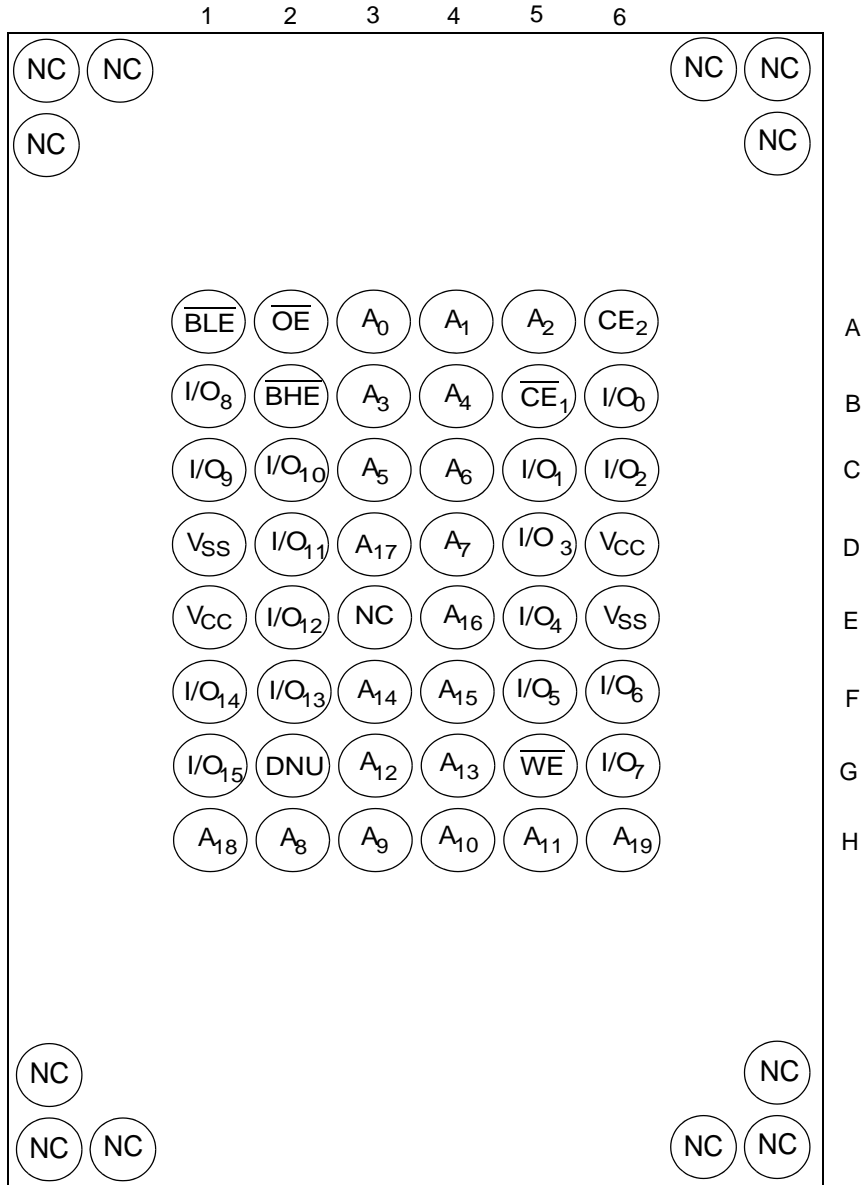
**Selection Guide**

		-10	-12	Unit
Maximum Access Time		10	12	ns
Maximum Operating Current	Commercial	275	260	mA
	Industrial	275	260	
Maximum CMOS Standby Current	Commercial/Industrial	50	50	mA

**Pin Configurations<sup>[1, 2]</sup>**

**60-ball FBGA**

(Top View)



**Notes:**

1. NC pins are not connected on the die.
2. DNU pins have to be left floating or tied to VSS to ensure proper application.

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied ..... -55°C to +125°C  
 Supply Voltage on  $V_{CC}$  to Relative GND<sup>[3]</sup> .... -0.5V to +4.6V  
 DC Voltage Applied to Outputs in High-Z State<sup>[3]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

DC Input Voltage<sup>[3]</sup> ..... -0.5V to  $V_{CC} + 0.5V$   
 Current into Outputs (LOW) ..... 20 mA

**Operating Range**

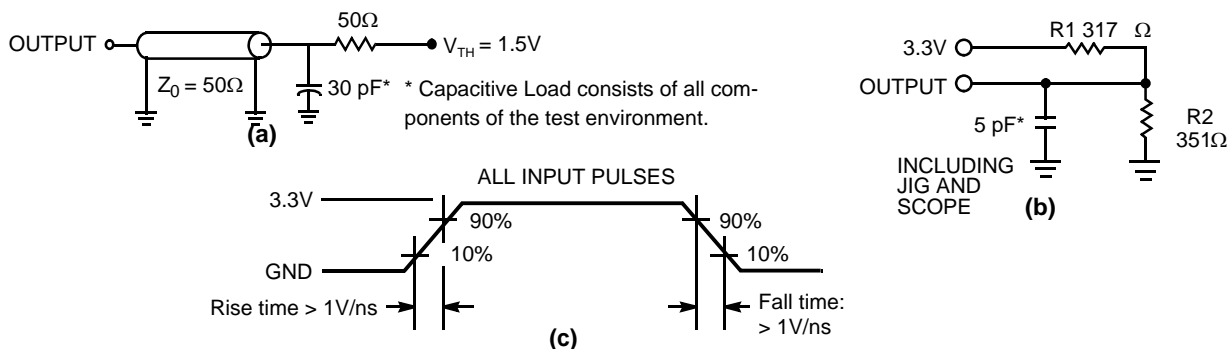
Range	Ambient Temperature	$V_{CC}$
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	-40°C to +85°C	

**DC Electrical Characteristics Over the Operating Range**

Parameter	Description	Test Conditions	-10		-12		Unit	
			Min.	Max.	Min.	Max.		
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		V	
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4	V	
$V_{IH}$	Input HIGH Voltage		2.0	$V_{CC} + 0.3$	2.0	$V_{CC} + 0.3$	V	
$V_{IL}$	Input LOW Voltage <sup>[3]</sup>		-0.3	0.8	-0.3	0.8	V	
$I_{IX}$	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	µA	
$I_{OZ}$	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC}$ , Output Disabled	-1	+1	-1	+1	µA	
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max.}, f = f_{MAX} = 1/t_{RC}$	Commercial		275		260	mA
			Industrial		275		260	mA
$I_{SB1}$	Automatic CE Power-down Current —TTL Inputs	$CE_2 \leq V_{IL}$ , Max. $V_{CC}$ , $CE \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$		70		70	mA	
$I_{SB2}$	Automatic CE Power-down Current —CMOS Inputs	$CE_2 \leq 0.3V$ Max. $V_{CC}$ , $CE \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ , or $V_{IN} \leq 0.3V$ , $f = 0$	Commercial/Industrial	50		50	mA	

**Capacitance<sup>[4]</sup>**

Parameter	Description	Test Conditions	TSOP II	FBGA	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}, f = 1 \text{ MHz}, V_{CC} = 3.3V$	6	8	pF
$C_{OUT}$	I/O Capacitance		8	10	pF

**AC Test Loads and Waveforms<sup>[5]</sup>**

**Notes:**

- $V_{IL}$  (min.) = -2.0V for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.
- Valid SRAM operation does not occur until the power supplies have reached the minimum operating  $V_{DD}$  (3.0V). As soon as 1ms ( $T_{power}$ ) after reaching the minimum operating  $V_{DD}$ , normal SRAM operation can begin including reduction in  $V_{DD}$  to the data retention ( $V_{CCDR}$ , 2.0V) voltage.

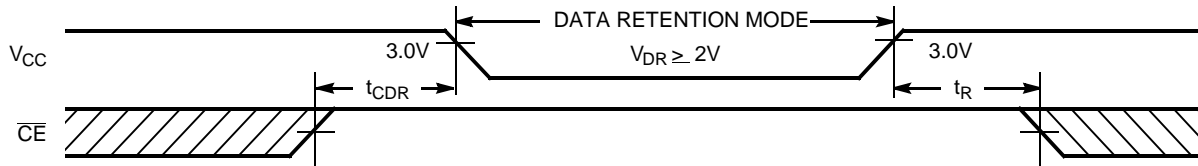
**AC Switching Characteristics** Over the Operating Range <sup>[7]</sup>

Parameter	Description	-10		-12		Unit
		Min.	Max.	Min.	Max.	
<b>Read Cycle</b>						
$t_{power}$	$V_{CC}$ (typical) to the first access <sup>[8]</sup>	1		1		ms
$t_{RC}$	Read Cycle Time	10		12		ns
$t_{AA}$	Address to Data Valid		10		12	ns
$t_{OHA}$	Data Hold from Address Change	3		3		ns
$t_{ACE}$	$\overline{CE}_1$ LOW/ $CE_2$ HIGH to Data Valid		10		12	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		5		6	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low-Z	1		1		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High-Z <sup>[9]</sup>		5		6	ns
$t_{LZCE}$	$\overline{CE}_1$ LOW/ $CE_2$ HIGH to Low-Z <sup>[9]</sup>	3		3		ns
$t_{HZCE}$	$\overline{CE}_1$ HIGH/ $CE_2$ LOW to High-Z <sup>[9]</sup>		5		6	ns
$t_{PU}$	$\overline{CE}_1$ LOW/ $CE_2$ HIGH to Power-Up <sup>[10]</sup>	0		0		ns
$t_{PD}$	$\overline{CE}_1$ HIGH/ $CE_2$ LOW to Power-Down <sup>[10]</sup>		10		12	ns
$t_{DBE}$	Byte Enable to Data Valid		5		6	ns
$t_{LZBE}$	Byte Enable to Low-Z	1		1		ns
$t_{HZBE}$	Byte Disable to High-Z		5		6	ns
<b>Write Cycle</b> <sup>[11, 12]</sup>						
$t_{WC}$	Write Cycle Time	10		12		ns
$t_{SCE}$	$\overline{CE}_1$ LOW/ $CE_2$ HIGH to Write End	7		8		ns
$t_{AW}$	Address Set-up to Write End	7		8		ns
$t_{HA}$	Address Hold from Write End	0		0		ns
$t_{SA}$	Address Set-up to Write Start	0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	7		8		ns
$t_{SD}$	Data Set-up to Write End	5.5		6		ns
$t_{HD}$	Data Hold from Write End	0		0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low-Z <sup>[9]</sup>	3		3		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High-Z <sup>[9]</sup>		5		6	ns
$t_{BW}$	Byte Enable to End of Write	7		8		ns

**Notes:**

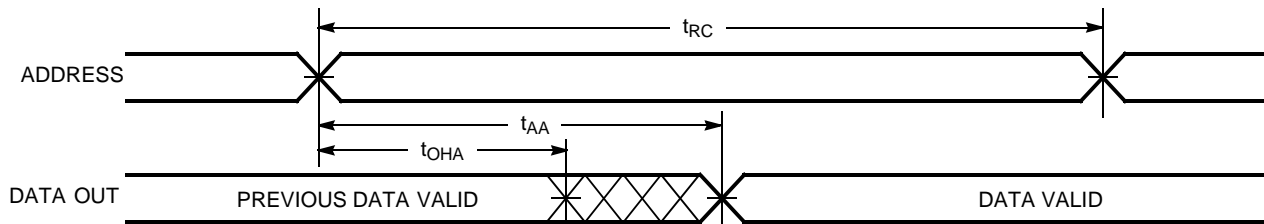
6. Valid SRAM operation does not occur until the power supplies have reached the minimum operating  $V_{DD}$  (3.0V). As soon as 1ms ( $T_{power}$ ) after reaching the minimum operating  $V_{DD}$ , normal SRAM operation can begin including reduction in  $V_{DD}$  to the data retention ( $V_{CCDR}$ , 2.0V) voltage.
7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and specified transmission line loads. Test conditions for the Read cycle use output loading shown in part a) of the AC test loads, unless specified otherwise.
8. This part has a voltage regulator which steps down the voltage from 3V to 2V internally.  $t_{power}$  time has to be provided initially before a Read/Write operation is started.
9.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZWE}$ ,  $t_{HZBE}$  and  $t_{LZOE}$ ,  $t_{LZCE}$ ,  $t_{LZWE}$ ,  $t_{LZBE}$  are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured  $\pm 200$  mV from steady-state voltage.
10. These parameters are guaranteed by design and are not tested.
11. The internal Write time of the memory is defined by the overlap of  $\overline{CE}_1$  LOW ( $CE_2$  HIGH) and  $\overline{WE}$  LOW. Chip enables must be active and  $\overline{WE}$  and byte enables must be LOW to initiate a Write, and the transition of any of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
12. The minimum Write cycle time for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

Data Retention Waveform

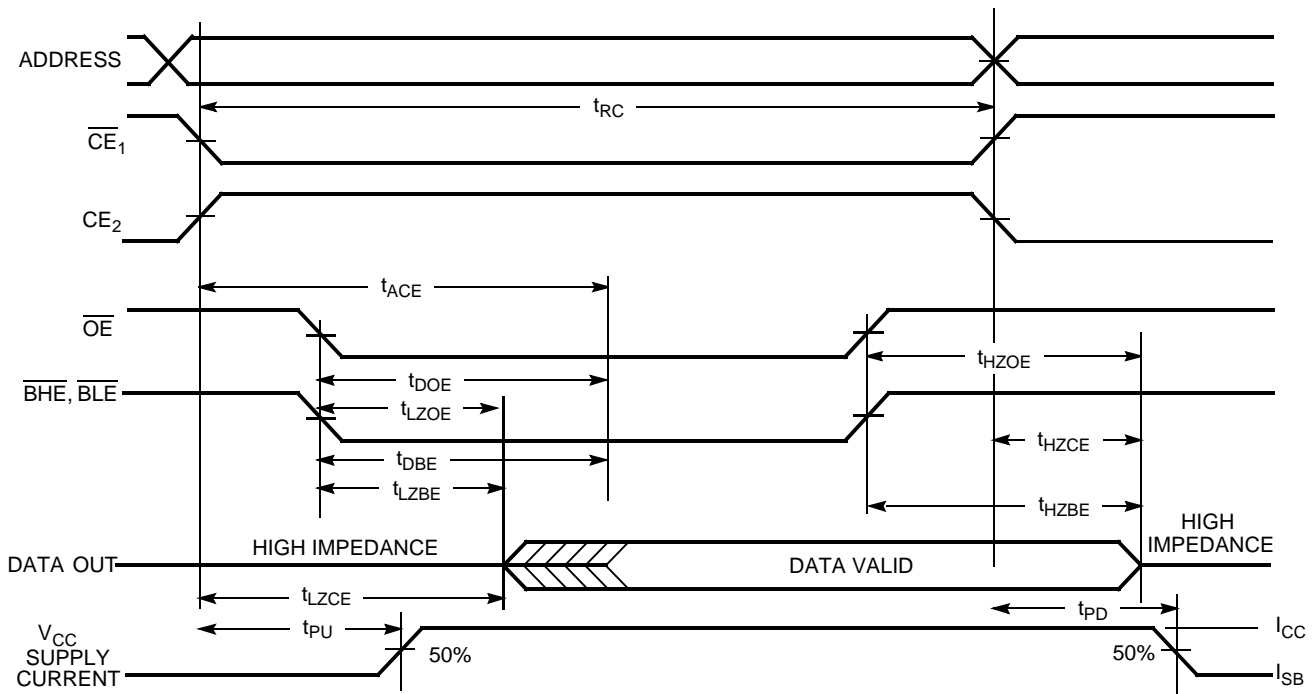


Switching Waveforms

Read Cycle No. 1<sup>[13,14]</sup>



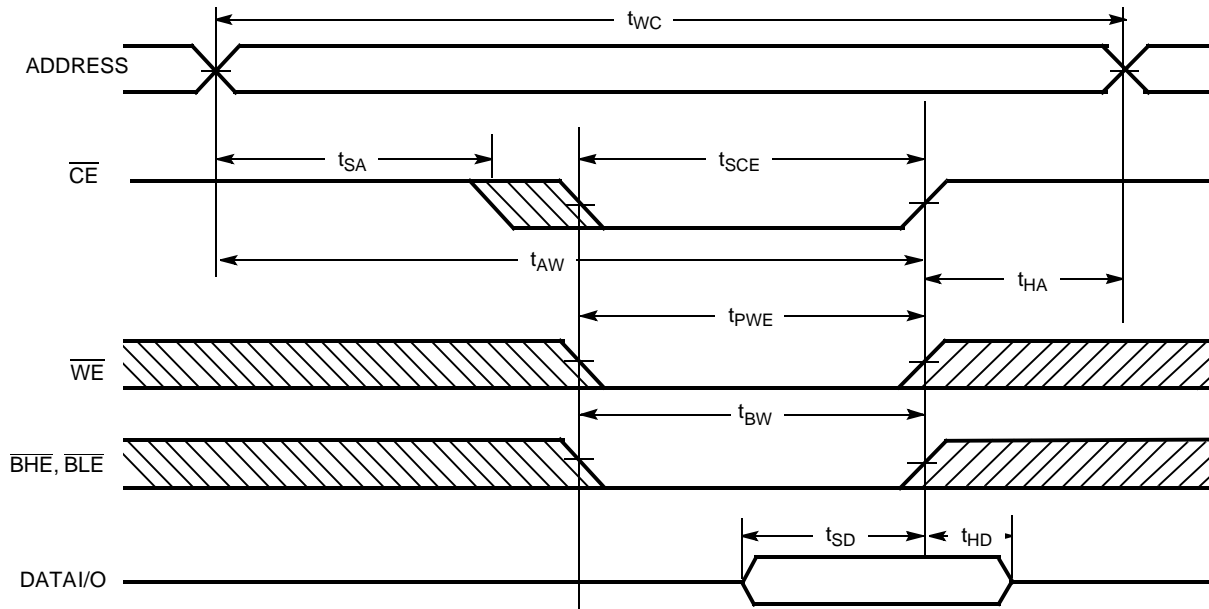
Read Cycle No. 2(OE Controlled)<sup>[14, 15]</sup>



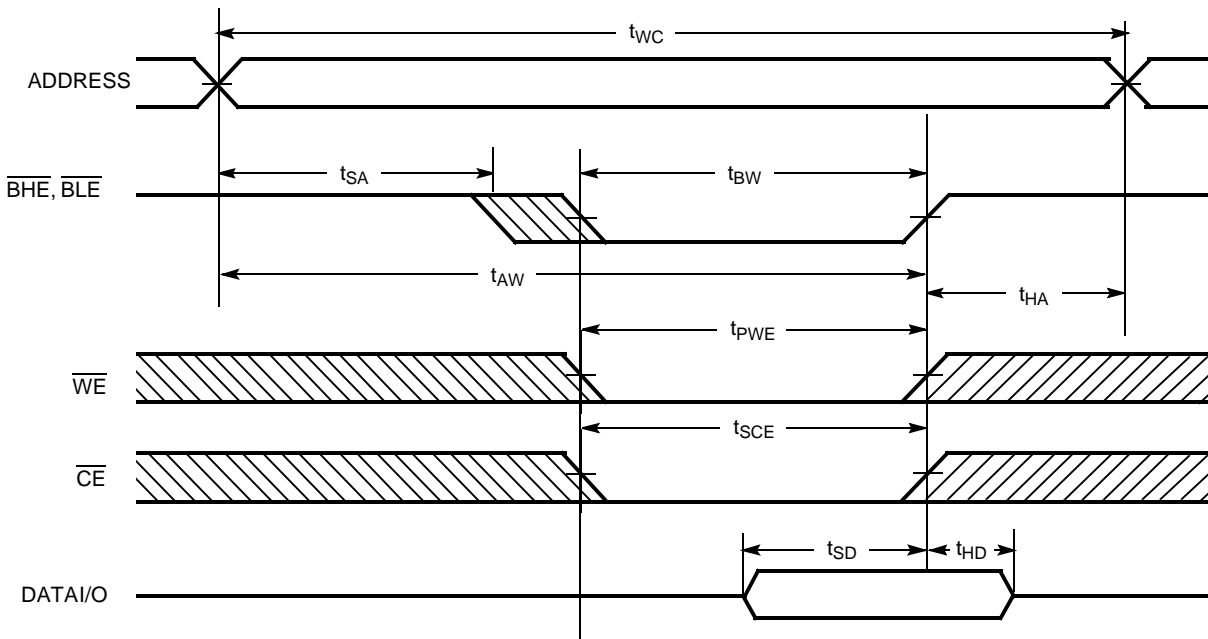
- Notes:**  
 13. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ .  $CE_2 = V_{IH}$ .  
 14.  $\overline{WE}$  is HIGH for Read cycle.  
 15. Address valid prior to or coincident with  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.

Switching Waveforms (continued)

Write Cycle No. 1 ( $\overline{CE}$  Controlled)<sup>[16,17,18]</sup>



Write Cycle No. 2 ( $\overline{BLE}$  or  $\overline{BHE}$  Controlled)

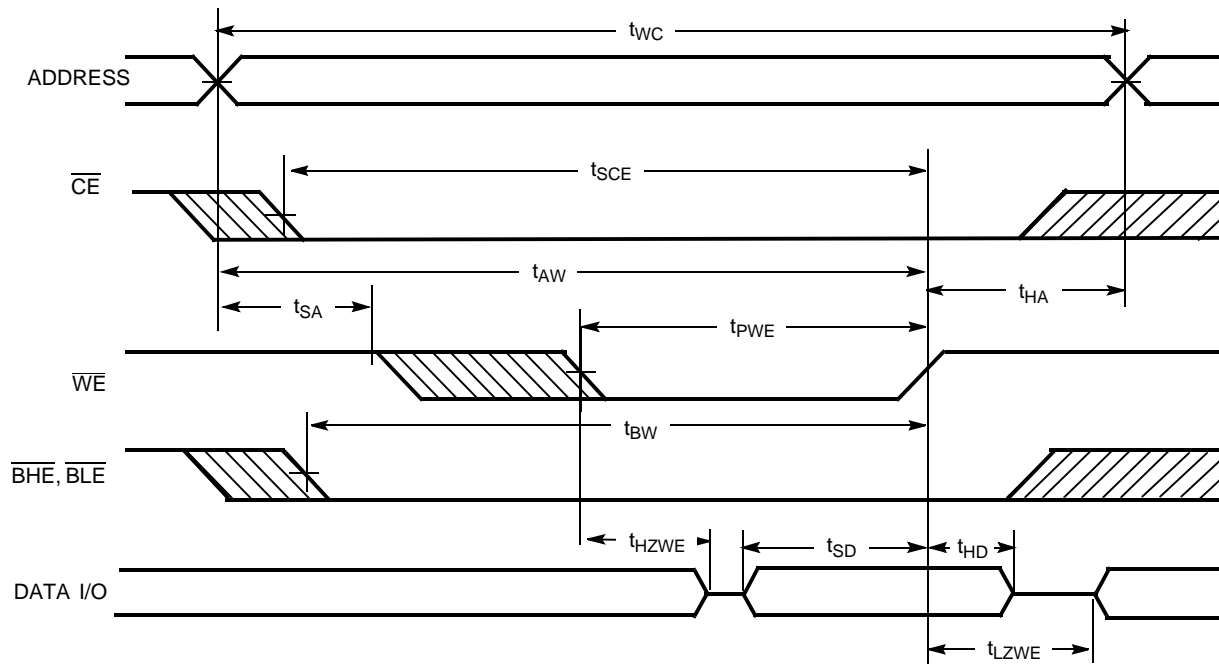


Notes:

- 16. Data I/O is high-impedance if  $\overline{OE}$  or  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IH}$ .
- 17. If  $\overline{CE}_1$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.
- 18.  $\overline{CE}$  is a shorthand combination of both  $\overline{CE}_1$  and  $\overline{CE}_2$  combined. It is active LOW.

Switching Waveforms (continued)

Write Cycle No. 3 (WE Controlled, OE LOW)<sup>[16,17,18]</sup>



**Truth Table**

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O <sub>0</sub> -I/O <sub>7</sub>	I/O <sub>8</sub> -I/O <sub>15</sub>	Mode	Power
H	X	X	X	X	X	High-Z	High-Z	Power-down	Standby (I <sub>SB</sub> )
X	L	X	X	X	X	High-Z	High-Z	Power-down	Standby (I <sub>SB</sub> )
L	H	L	H	L	L	Data Out	Data Out	Read All Bits	Active (I <sub>CC</sub> )
L	H	L	H	L	H	Data Out	High-Z	Read Lower Bits Only	Active (I <sub>CC</sub> )
L	H	L	H	H	L	High-Z	Data Out	Read Upper Bits Only	Active (I <sub>CC</sub> )
L	H	X	L	L	L	Data In	Data In	Write All Bits	Active (I <sub>CC</sub> )
L	H	X	L	L	H	Data In	High-Z	Write Lower Bits Only	Active (I <sub>CC</sub> )
L	H	X	L	H	L	High-Z	Data In	Write Upper Bits Only	Active (I <sub>CC</sub> )
L	H	H	H	X	X	High-Z	High-Z	Selected, Outputs Disabled	Active (I <sub>CC</sub> )

**Ordering Information**

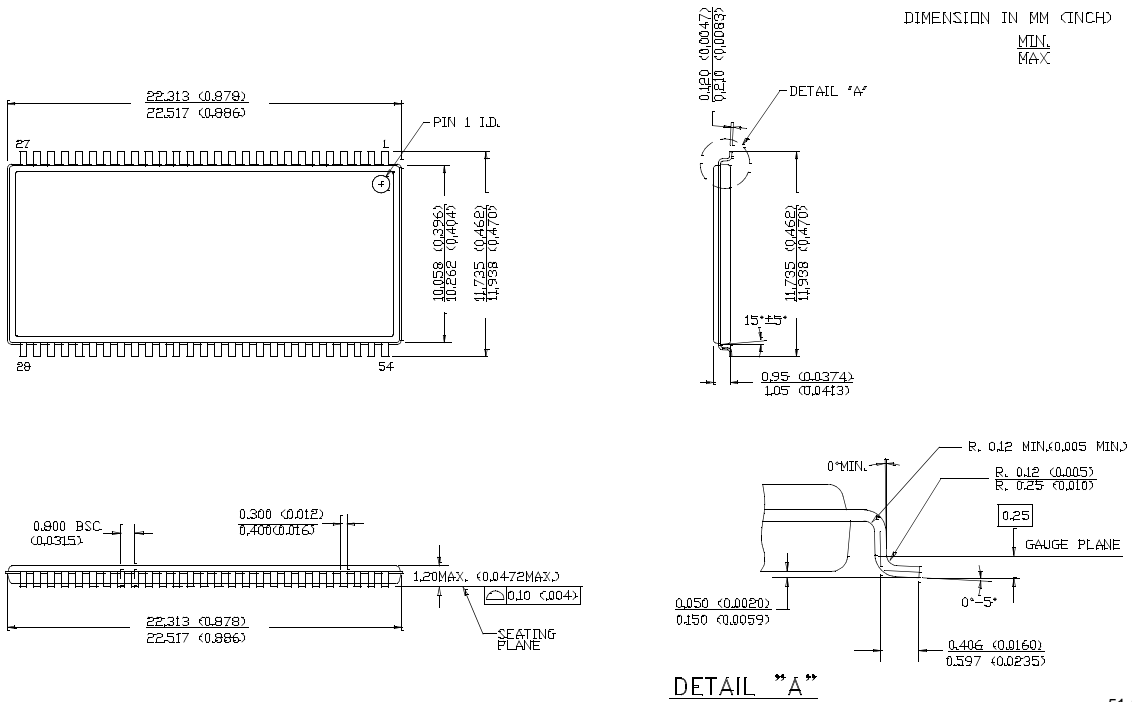
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1061AV33-10ZXC	51-85160	54-pin TSOP II (Pb-free)	Commercial
	CY7C1061AV33-10BAC	51-85162	60-ball (8 mm x 20 mm x 1.2 mm) FBGA	
	CY7C1061AV33-10ZI	51-85160	54-pin TSOP II	Industrial
	CY7C1061AV33-10ZXI		54-pin TSOP II (Pb-free)	
	CY7C1061AV33-10BAI		60-ball (8 mm x 20 mm x 1.2 mm) FBGA	
12	CY7C1061AV33-12ZC	51-85160	54-pin TSOP II	Commercial
	CY7C1061AV33-12ZXC		54-pin TSOP II (Pb-free)	
	CY7C1061AV33-12BAC	51-85162	60-ball (8 mm x 20 mm x 1.2 mm) FBGA	Industrial
	CY7C1061AV33-12ZI	51-85160	54-pin TSOP II	
	CY7C1061AV33-12ZXI		54-pin TSOP II (Pb-free)	
	CY7C1061AV33-12BAI	51-85162	60-ball (8 mm x 20 mm x 1.2 mm) FBGA	

Contact local Cypress representative for availability of the these parts.



Package Diagrams

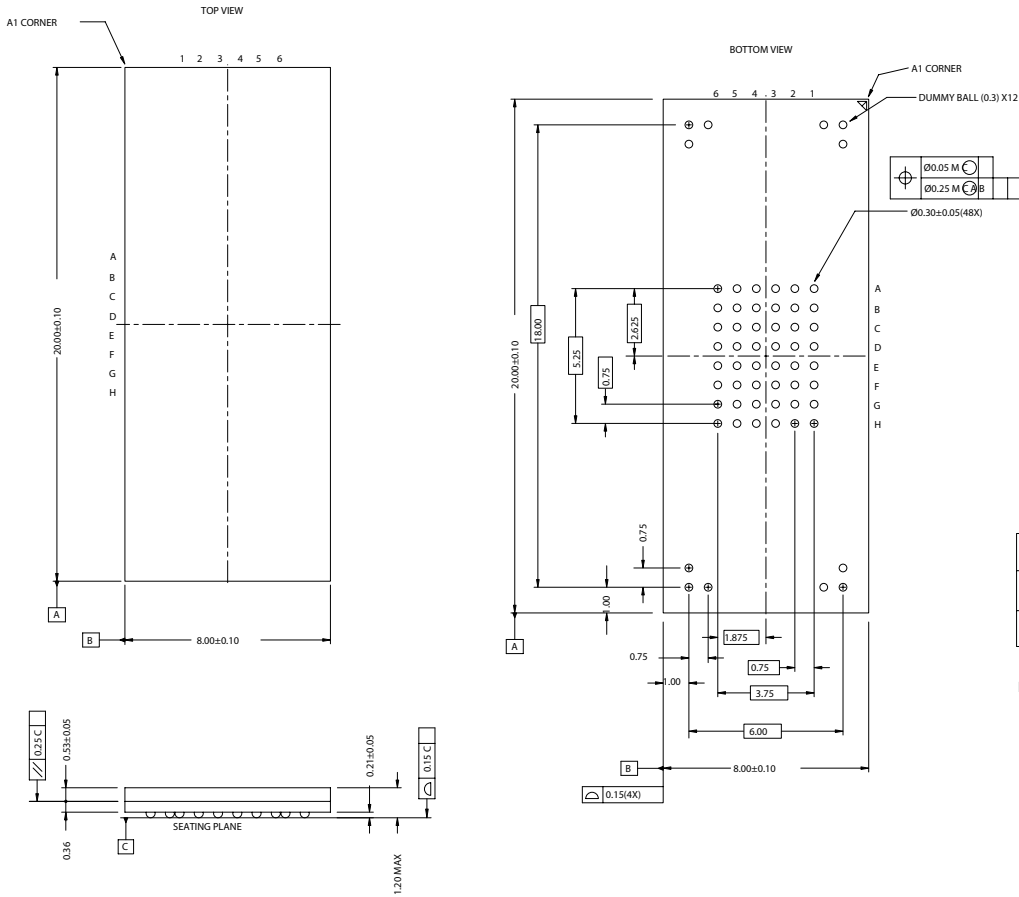
54-pin TSOP II (51-85160)



51-85160-\*\*

Package Diagrams (continued)

60-ball FBGA (8 mm x 20 mm x 1.2 mm) (51-85162)



DIMENSIONS IN MM

PART #	
BA60A	STANDARD PKG.
BK60A	LEAD FREE PKG.

PKG WEIGHT: 0.30 gms

51-85162-1D

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**Document History Page**

Document Title: CY7C1061AV33 1M x 16 Static RAM				
Document Number: 38-05256				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	113725	03/28/02	NSL	New Data Sheet
*A	117058	07/31/02	DFP	Removed 15-ns bin
*B	117989	08/30/02	DFP	Added 8-ns bin Changed Icc for 8, 10, 12 bins t <sub>power</sub> changed from 1 μs to 1 ms. Load Cap Comment changed (for Tx line load) t <sub>SD</sub> changed to 5.5 ns for the 10-ns bin Changed some 8-ns bin numbers (t <sub>HZ</sub> , t <sub>DOE</sub> , t <sub>DBE</sub> ) Removed hz<lz comments from data sheet
*C	120383	11/06/02	DFP	Final data sheet Added note 3 to "AC Test Loads and Waveforms" and note 7 to t <sub>pu</sub> and t <sub>pd</sub> Updated Input/Output Caps (for 48BGA only) to 8 pF/10 pF and for the 54-pin TSOP to 6/8 pF
*D	124439	2/25/03	MEG	Changed ISB1 from 100 mA to 70 mA Shaded fBGA production ordering information
*E	492137	See ECN	NXR	Corrected Block Diagram on page #1 Removed 8 ns speed bin Changed 48-Ball FBGA to 60-Ball FBGA in Pin Configuration Included Note #1 and 2 on page #2 Changed the description of I <sub>IX</sub> from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Updated the Ordering Information Table
*F	508117	See ECN	NXR	Updated FBGA Pin Configuration Updated Ordering Information table