19-5041; Rev 0; 1987

4½ Digit A/D Converter with Multiplexed BCD Outputs

ICL7135

General Description

The Maxim ICL7135 is a high precision monolithic 4½ digit A/D converter. Dual slope conversion reliability is combined with ±1 in 20,000 count accuracy and a 2.0000V full scale capability. It features high impedance differential inputs, nearly ideal differential linearity, true ratiometric operation, auto zero and auto-polarity. The multiplexed BCD outputs and digit drivers provide easy interface to external display drivers like the Maxim ICM7211A. The only other external components needed to make precision DVM/DPMs are a reference and a clock. For more complex systems the BCD outputs are enhanced by $\overline{\text{STROBE}}$, OVERRANGE, UNDERRANGE, RUN/$\overline{\text{HOLD}}$ and BUSY lines providing easy interface to microprocessors and UARTs. This interfacing capability makes the ICL7135 an ideal device for use in microprocessor based data acquisition and control systems.

The ICL7135 has auto-zero accuracy better than 10μV, zero drift of 0.5μV/°C, input bias current of 10pA max. and rollover error of less than 1 count.

Features

- **Improved 2nd Source (See our "Maxim Advantage™" Page 3)**
- **±20,000 Count Resolution**
- **Guaranteed ±1 Count accuracy**
- **Over-range, under-range signals for auto-range capability**
- **Easy interface to UARTs and μPs**
- **TTL compatible, Multiplexed BCD outputs**
- **True differential input. Zero reading guaranteed for 0 volt input**
- **True polarity at zero for precise null detection**
- **Monolithic CMOS design**

Applications

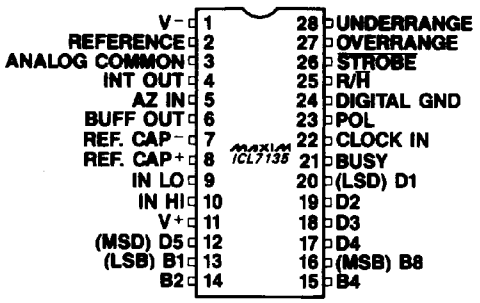
This device is used in a wide range of measurement applications involving the manipulation and display of analog data:

Pressure	Weight
Voltage	Current
Resistance	Speed
Temperature	Material Thickness

Ordering Information

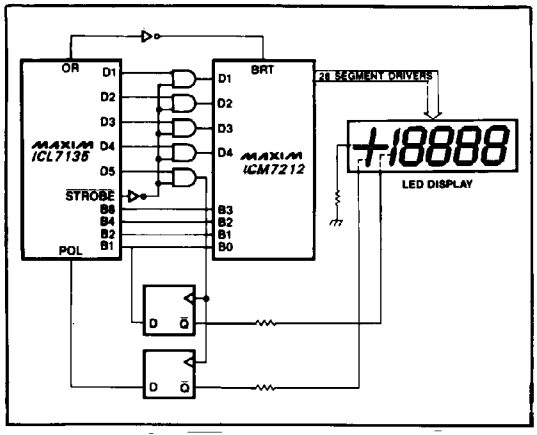
PART	TEMP. RANGE	PACKAGE
ICL7135CJI	0°C to 70°C	28 Lead CERDIP
ICL7135CPI	0°C to 70°C	28 Lead Plastic DIP
ICL7135CQI	0°C to 70°C	28 Lead Plastic chip carrier
ICL7135C/D	0°C to 70°C	Dice

Pin Configuration



NOTE: All packages have the same pinout.

Typical Operating Circuit



The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

4½ Digit A/D Converter with Multiplexed BCD Outputs

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 2)
- CERDIP Package 1000mW
- Plastic Package 800mW

Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +160°C
Lead Temperature (Soldering, 10 sec) ..... 300°C
Supply Voltage V+ ..... +6V
V− ..... −9V
Analog Input Voltage (either input) (Note 1) ..... V+ to V−
Reference Input Voltage (either input) ..... V+ to V−
Clock Input ..... Gnd to V+

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to +100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ICL7135 ELECTRICAL CHARACTERISTICS (Note 1)

($V^+ = +5V$, $V^- = -5V$, $T_A = 25°C$, Clock Frequency Set for 3 Reading/Sec

		CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG (Note 1) (Note 2)		Zero Input Reading		$V_{IN} = 0.0V$ Full Scale = 2.000V	−0.0000	±0.0000	+0.0000	Digital Reading
		Ratiometric Reading (2)		$V_{IN} = V_{REF}$ Full Scale = 2.000V	+0.9998	+0.9999	+1.0000	Digital Reading
		Linearity over ± Full Scale (error of reading from best straight line)		$-2V \le V_{IN} \le +2V$		0.5	1	Digital Count Error
		Differential Linearity (difference between worse case step of adjacent counts and ideal step)		$-2V \le V_{IN} \le +2V$		.01		LSB
		Rollover error (Difference in reading for equal positive & negative voltage near full scale)		$-V_{IN} \equiv +V_{IN} \approx 2V$		0.5	1	Digital Count Error
		Noise (P-P value not exceeded 95% of time)	e_n	$V_{IN} = 0V$ Full Scale = 2.000V		15		μV
		Leakage Current at Input	I_{ILK}	$V_{IN} = 0V$		1	10	pA
		Zero Reading Drift		$V_{IN} = 0V$ $0° \le T_A \le 70°C$		0.5	2	μV/°C
		Scale Factor Temperature Coefficient (3)	TC	$V_{IN} = +2V$ $0° \le T_A \le 70°C$ (ext. ref. 0 ppm/°C)		2	5	ppm/°C
DIGITAL	INPUTS	Clock In, Run/$\overline{Hold}$	V_{INH} V_{INL} I_{INL} I_{INH}	$V_{IN} = 0$ $V_{IN} = +5V$	2.8	2.2 1.6 0.02 0.1	0.8 0.1 10	V mA μA
	OUTPUTS	All Outputs B_1, B_2, B_4, B_8 D_1, D_2, D_3, D_4, D_5	V_{OL} V_{OH}	$I_{OL} = 1.6mA$ $I_{OH} = -1mA$	2.4	0.25 4.2	0.40	V V
		BUSY, $\overline{STROBE}$ OVER-RANGE, UNDER-RANGE POLARITY	V_{OH}	$I_{OH} = -10\mu A$	4.9	4.99		V
	SUPPLY	+5V Supply Range	V^+		+4	+5	+6	V
		−5V Supply Range	V^-		−3	−5	−8	V
		+5V Supply Current	I^+	$f_c = 0$		1.1	3.0	mA
		−5V Supply Current	I^-	$f_c = 0$		0.8	3.0	
		Power Dissipation Capacitance	C_{PD}	vs. Clock Freq		40		pF
	Clock	Clock Freq. (Note 4)			DC	2000	1200	kHz

Note 1: Tested in 4½ digit (20,000 count) circuit shown in Fig. 1, clock frequency 120kHz.

Note 2: Tested with a low dielectric absorption integrating capacitor. See Component Selection Section.

Note 3: The temperature range can be extended to +70°C and beyond as long as the auto-zero and reference capacitors are increased to absorb the higher leakage of the ICL7135.

Note 4: This specification relates to the clock frequency range over which the ICL7135 will correctly perform its various functions. See "Max Clock Frequency" below for limitations on the clock frequency range in a system.

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with the descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

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- **Guaranteed 2mA Max Supply Current**
- **Key Parameters Guaranteed Over Temperature**
- **Significantly Improved ESD Protection (Note 6)**
- **Low Noise**
- **Maxim Quality and Reliability**

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS Specifications below satisfy or exceed all "tested" parameters on adjacent page.

($V^+ = +5V$, $V^- = -5V$, $T_A = 25°C$, Clock Frequency Set for 3 Reading/Sec

		Characteristics	Symbol	Conditions	Min	Typ	Max	Units
ANALOG		**Zero Input Reading**		**$V_{IN} = 0.0V$, Full Scale = 2.000V** **$0° \le T_A \le +70°C$**	**−0.0000**	**±0.0000**	**+0.0000**	**Digital Reading**
ANALOG		**Ratiometric Reading (Note 2)**		$V_{IN} = V_{REF}$, Full Scale = 2.000V $T_A = 25°C$ **$0° \le T_A \le +70°C$**	+0.9998 **+0.9995**	+0.9999 **+0.9999**	+1.0000 **+1.0005**	**Digital Reading**
ANALOG		Linearity over ± Full Scale (error of reading from best straight line)		$-2V \le V_{IN} \le +2V$		0.5	1	Digital Count Error
ANALOG		Differential Linearity (difference between worse case step of adjacent counts and ideal step)		$-2V \le V_{IN} \le +2V$		.01		LSB
ANALOG		Rollover error (Difference in reading for equal positive & negative voltage near full scale)		$-V_{IN} = +V_{IN} \approx 2V$		0.5	1	Digital Count Error
ANALOG	(Note 1) (Note 2)	Noise (P-P value not exceeded 95% of time)	e_n	$V_{IN} = 0V$, Full Scale = 2.000V		15		μV
ANALOG		**Leakage Current at Input**	I_{ILK}	$V_{IN} = 0V$ $T_A = 25°C$ **$0° \le T_A \le +70°C$**		1	10 **250**	pA **pA**
ANALOG		Zero Reading Drift		$V_{IN} = 0V$ $0° \le T_A \le +70°C$		0.5	2	μV/°C
ANALOG		Scale Factor Temperature Coefficient (Note 3)	TC	$V_{IN} = +2V$ $0° \le T_A \le +70°C$ (ext. ref. 0 ppm/°C)		2	5	ppm/°C
INPUTS		Clock In, Run/$\overline{Hold}$	V_{INH} V_{INL} I_{INL} I_{INH}	$0° \le T_A \le +70°C$ $0° \le T_A \le +70°C$ $V_{IN} = 0$ $0° \le T_A \le +70°C$ $V_{IN} = +5V$ $0° \le T_A \le +70°C$	2.8	2.2 1.6 0.02 0.1	 0.8 0.1 10	V V mA μA
DIGITAL	OUTPUTS	All Outputs B_1, B_2, B_4, B_8 D_1, D_2, D_3, D_4, D_5 BUSY, $\overline{STROBE}$ OVER-RANGE, UNDER-RANGE POLARITY	V_{OL} V_{OH} V_{OH}	$I_{OL} = 1.6mA$ $I_{OH} = -1mA$ $I_{OH} = -10\mu A$	 2.4 4.9	0.25 4.2 4.99	0.40	V V V
DIGITAL	SUPPLY	+5V Supply Range	V^+		+4	+5	+6	V
DIGITAL	SUPPLY	−5V Supply Range	V^-		−3	−5	−8	V
DIGITAL	SUPPLY	**+5V Supply Current**	I^+	**$f_c = 0$ $T_A = 25°C$** **$0° \le T_A \le +70°C$**		**1.1**	**2.0** **3.0**	**mA** **mA**
DIGITAL	SUPPLY	**−5V Supply Current**	I^-	**$f_c = 0$ $T_A = 25°C$** **$0° \le T_A \le +70°C$**		**0.8**	**2.0** **3.0**	**mA** **mA**
DIGITAL	SUPPLY	Power Dissipation Capacitance	C_{PD}	(Note 5)		40		pF
CLOCK		Clock Freq. (Note 4)			DC	2000	1200	kHz

Note 1: Tested in 4½ digit (20,000 count) circuit shown in Fig. 1, clock frequency 120kHz.

Note 2: Tested with a low dielectric absorption integrating capacitor. See Component Selection Section.

Note 3: The Temperature range can be extended to +70°C and beyond as long as the auto-zero and reference capacitors are increased to absorb the higher leakage of the ICL7135.

Note 4: This specification relates to the clock frequency range over which the ICL7135 will correctly perform its various functions. See "Clock Frequency" below for limitations on the clock frequency range in a system.

Note 5: +5V Supply current for $f_c \neq 0$ is $I^+ = I^+_{(f_c = 0)} + C_{PD} \times 5V \times f_c$.

Note 6: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil Std 883, Method 3015.1)

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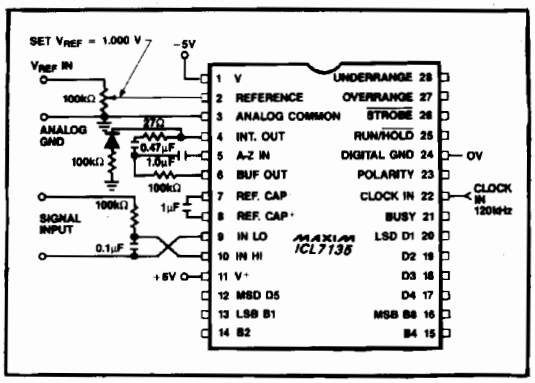

Figure 1. ICL7135 Test Circuit

Detailed Description

General Operation

The ICL7135 is divided into an Analog section and a Digital section. The digital section includes the counters, input and output interfaces, and control logic which controls the timing of each measurement cycle. Each measurement is divided into four phases: 1) auto-zero (AZ), 2) signal integrate (INT), 3) reference deintegrate (DE), and 4) zero integrator (ZI). The digital section controls the operation of the analog section during each of these phases, using counters and the state of the comparator to determine when to start each of the four phases.

Auto-Zero Phase

During auto-zero Input HI and Input LO are disconnected from the input pins and are internally shorted to Analog COMMON. The output of the comparator is connected to the inverting input of the Integrator, and at the same time the non-inverting input of the integrator is connected to the input of the buffer. This feedback loop charges the autozero capacitor, C_{AZ}, to compensate for the offset voltages of the buffer amplifier, integrator, and comparator. Also during auto-zero, the reference capacitor is connected to the voltage reference and is charged to the reference voltage. The auto-zero cycle is a minimum of 9800 clock cycles, except after an over-range reading. After an over-range, the extended zero integrate phase reduces the auto-zero phase to 3800 clock cycles.

Signal Integrate Phase

At the end of the auto-zero phase the auto-zero loop is opened, and the Input High and Input Low are switched to the external pins IN-HI and IN-LO. The analog section integrates the differential voltage between Input High and Input Low. The differential voltage must be within the ICL7135's common mode range. The voltage on the integrator capacitor at the end of signal integrate is directly proportional to the differential voltage between Input High and Input Low, and is also directly proportional to the length of the signal integrate phase. The signal integrate phase lasts precisely 10,000 clock cycles. At the end of this phase the input signal polarity is determined.

De-Integrate Phase

At the end of signal integrate, Input High and Input Low are disconnected from the external pins. The integrator non-inverting input pin is then internally connected to Analog Common and the buffer input is connected to one side of the reference capacitor. The other side of the reference capacitor is connected to Analog Common. The polarity at the output of the integrator (as detected by the comparator at the end of signal integrate phase) determines which terminal of the reference capacitor is connected to the buffer input. The reference capacitor polarity is chosen so that the integrator output will always return towards Analog Common. Since the reference capacitor was charged to the reference voltage during the auto-zero phase, the integrator input voltage is now the reference voltage. The De-Integrate phase lasts for 20,001 counts, or until the comparator detects that the integrator output has crossed zero, whichever occurs first. The time required to return to zero is proportional to the input signal and is inversely proportional to the reference voltage. The number of clock cycles required to return to zero is counted by the digital section and is latched as the measurement result.

$$\text{Displayed reading} = 10{,}000 \times \frac{V_{IN}}{V_{REF}}$$

Zero Integrator Phase

The last of the four phases is the zero integrator phase. The non-inverting input of the integrator is internally shorted to Analog Common and the buffer input is internally connected to the output of the comparator. This closes a loop that forces the integrator output to zero. Normally this phase lasts only 100 to 200 counts, sufficient time to remove the small residual charge on the integrator capacitor caused by the comparator delay and the one count delay created by sampling the comparator output only once per clock cycle. However, an overrange condition will exist when the integrator output does not return to zero by the end of the De-Integrate phase, and can leave a residual voltage on the integrator capacitor. In this case, the Zero Integrator phase is increased to 6200 counts to ensure that the integrator capacitor is fully discharged before the next measurement cycle is started.

Analog Section

Analog COMMON

Analog COMMON is the Analog ground reference for the ICL7135. If Input Low is at a voltage other than Analog

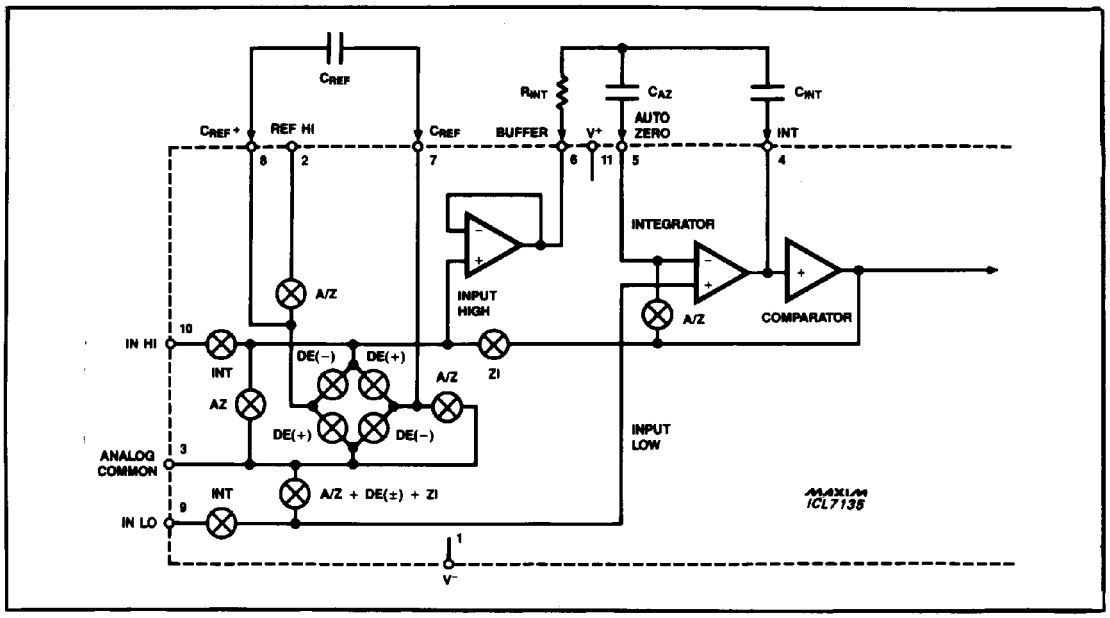

Figure 2. Analog Section of ICL7135

COMMON a common mode voltage will be introduced and, although the ICL7135 has an excellent CMRR, Input Low and Analog COMMON should be connected together whenever possible. Analog COMMON is also the reference point for the reference voltage. The Analog Common voltage is normally connected to the system ground when using ±5V supplies. When the ICL7135 is operated from a single supply voltage the Analog Common should be connected to a voltage source approximately halfway between V+ and ground.

Input Buffer

The ICL7135 input buffer is a CMOS buffer with a common mode input voltage range of approximately V+−1.0V to V−+1.5V. The quiescent current is approximately 100μA and the buffer can deliver up to 40μ of output current with excellent linearity.

Integrator

The integrator amplifier, similar to the buffer amplifier, can deliver 20μA of output current with high linearity while swinging to within 0.3V of either supply rail. The integrator's non-inverting terminal is connected to IN LO during the signal integrate phase, so the voltage on the IN LO terminal sets the starting point for the integrator output during signal integrate. If IN LO is at a voltage other than ground, this will limit the maximum allowable swing at the integrator output, and the value of the integrating capacitor should be increased. (Refer to Component Selection)

Comparator

The comparator monitors the voltage on the integrator capacitor during deintegrate. The digital section samples the comparator output once per clock cycle and terminates the deintegrate cycle when the comparator changes its state as the integrator voltage passes through zero. The offset voltage of the comparator is not critical since the auto-zero phase compensates for the offset. The output of the comparator is the only output from the analog section to the digital section.

Digital Section

As shown in Figure 3, the digital section consists of counters, latches, output multiplexer, and control logic. The control logic monitors the counters and the comparator to determine the start of each phase, and sends control signals to the analog section to drive the analog switches to the proper state for each measurement phase. The control section also responds to the external input, RUN/$\overline{\text{HOLD}}$, and creates the control outputs; OVERRANGE, UNDERRANGE, BUSY, and $\overline{\text{STROBE}}$.

RUN/$\overline{\text{HOLD}}$

When RUN/$\overline{\text{HOLD}}$ is high or open the ICL7135 will continuously perform conversions with each measurement being 40,002 clock cycles long. When RUN/$\overline{\text{HOLD}}$ goes low, the ICL7135 will complete the measurement in progress then remain in the auto-zero cycle, holding the last reading. If RUN/$\overline{\text{HOLD}}$ goes high after the maximum period assigned to deintegrate, a new conversion will start, with a delay of 1 to 10,001 clock cycles between the

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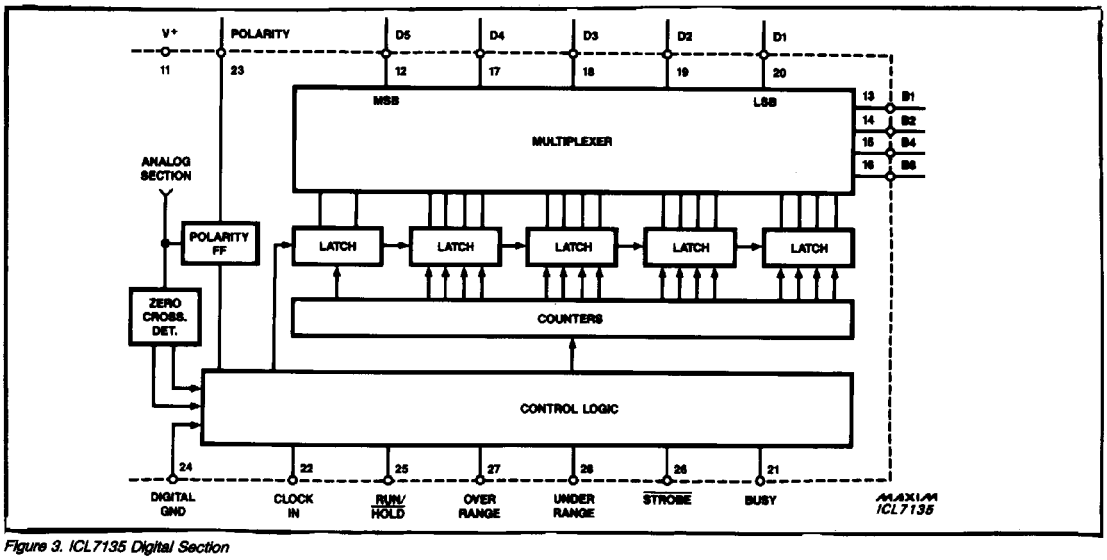

Figure 3. ICL7135 Digital Section

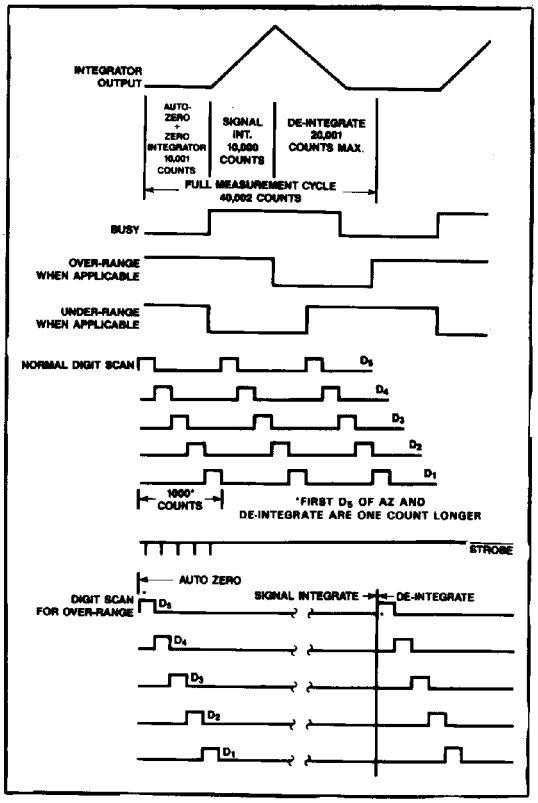

Figure 4. Timing Diagram

rising edge of the RUN/$\overline{\text{HOLD}}$ input and the BUSY output. A RUN/$\overline{\text{HOLD}}$ pulse during the unused portion of deintegrate phase will be ignored, but when in the auto-zero phase a positive pulse of only 300ns (typical) will start the conversion. Figure 5 shows a simple method of obtaining one, and only one, conversion for each measurement request.

BUSY

BUSY is a status output that goes high at the beginning of signal integrate and stays high until the first clock pulse after zero crossing during De-integrate (or end of De-Integrate if overranged). The internal data latches are loaded during the next clock cycle after the falling edge of BUSY. Since BUSY is high for the 10,000 counts of signal integrate + number of counts during De-Integrate + 1 clock cycle, a simple way of sending conversion data down a single pair of wires is to logically 'AND' BUSY with the clock and to subtract 10,001 counts from the number received. Figure 6 shows a system using this method to remotely display data.

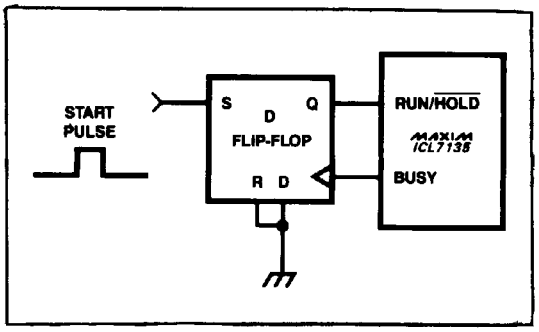

Figure 5. External RUN/HOLD Latch

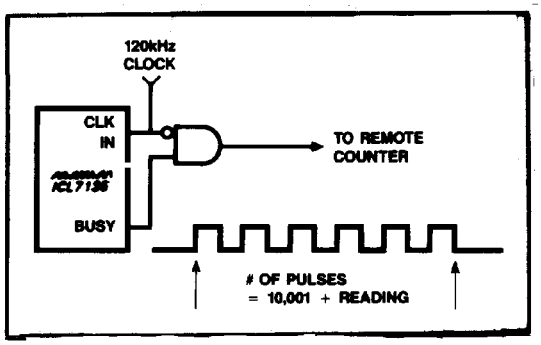

Figure 6. Serial Pulse Stream for Remote Reading

Digit Outputs

The digit outputs go high sequentially, D5 to D1, for a period of 200 clock cycles per digit. The 5 digits are continuously scanned except after an over-range measurement. After an over-range reading the digit scan stops after the strobe sequence, and remains stopped until the start of De-Integrate. For a continuous series of over-range readings, the digits will be scanned for 21,000 counts out of 40,002, resulting in a flashing display as an over-range indicator. D5 is the most significant digit.

BCD Outputs

The 4 BCD output pins are positive logic signals whose BCD data corresponds to the currently active digit strobe. The ICL7135 does not have inter-digit blanking and the BCD data changes simultaneously with the edges of the digit outputs.

$\overline{\text{STROBE}}$

The $\overline{\text{STROBE}}$ output is a negative going pulse that is useful for latching the multiplexed BCD outputs into external BCD latches. Five negative going $\overline{\text{STROBE}}$ pulses occur in the center of the data corresponding to each of the 5 digits of measurement results, once and only once after the end of each conversion (immediately after the falling edge of BUSY). The BCD data is valid at both edges of $\overline{\text{STROBE}}$, and data can be latched in either a level sensitive latch, or an edge triggered latch. Figures 11, 12 and 14 show the use of $\overline{\text{STROBE}}$ to latch the BCD data. $\overline{\text{STROBE}}$ pulse width is 1μs less than ½ clock period.

Over-range and Under-range Outputs

These active high status outputs are set to a high level at the end of BUSY if the measurement result is 1800 or less (Under-range), or greater than 19,999 (Over-range). Under-range is reset at the beginning of the signal integrate phase; over-range is reset at the beginning of the de-integrate phase.

Polarity

The Polarity output is updated at the beginning of each de-integrate phase, and is high for a positive input signal. The Polarity output is valid for all inputs, including ±0 and overrange signals.

Component Selection

The analog component values must be selected with care to achieve optimum performance in each application. Factors that affect the proper values include the reading rate, input common mode voltage, the full scale and reference voltages, and the power supply voltages.

Integrating Resistor

Good linearity is obtained when the integrating resistor value is chosen such that the buffer's maximum output current is between 5 and 40μA. The quiescent current of the buffer is 100μA, and it can supply 20μA of output current with excellent linearity. The buffer's maximum output current occurs with a full scale input voltage, and the integrating resistor value may be calculated as:

$$R_{INT} = \frac{\text{full scale voltage}}{20\mu A}$$

Integrating Capacitor

The maximum swing of the integrator during the signal integrate phase can be calculated as:

$$V_{swing} = \frac{I_{INT} \times T_{INT}}{C_{INT}}$$

Where $I_{INT} = 20\mu A$ if R_{INT} is chosen as described above and $T_{INT} = 10{,}000$ clock periods (83.3ms for 120kHz clock frequency). The integrator swing range should be maximized while avoiding saturation of the integrator output. Normally the integrator will not saturate until its output is within 0.3V of either supply, but for the best integral linearity the integrator's output should remain at least 1V away from either supply. For ±5V supply and Analog Common and IN LO connected to ground, a ±3.5V to ±4V swing range is optimum. Rearranging the above formula and inserting values as described above, C_{INT} may be calculated as:

$$C_{INT} = \frac{20\mu A \times 83.3ms}{3.5V} = 0.47\mu F$$

The integrator swing must be reduced if either Analog Common or IN LO is not grounded, or if the supply voltage is less than ±5V.

The integrating capacitor must have low dielectric absorption to obtain low integral nonlinearity, rollover, and ratiometric errors. The result of measurements with the reference tied to the IN HI is a good indication of the

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amount of dielectric absorption in the integrating capacitor. A good integrating capacitor will result in a reading of 9999, and any deviation from this reading is probably due to dielectric absorption. Polypropylene capacitors have been found to be suitable, as have Teflon capacitors. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

Auto-Zero Capacitor

The size of the auto-zero capacitor will have a significant effect on the overall system noise, with larger auto-zero capacitors resulting in a quieter system. The dielectric absorption of the auto-zero capacitor affects only the speed of settling at power-up or recovery from overload and nearly any capacitor type can be used. The zero integrator phase of the ICL7135 allows the use of large auto-zero capacitors while avoiding the "over-range hangover" and hysteresis effects that occur in A/D converters without the zero integrator phase.

Reference Capacitor

Like the auto-zero capacitor, the reference capacitor's dielectric absorption is rarely critical. Low dielectric absorption reference capacitors are only required where fast settling time is needed in systems with a rapidly changing reference voltage such as ratiometric ohms measurement in multimeters.

The reference capacitor DOES need to be a low leakage capacitor since it must store the reference voltage while floating during both the signal integrate and the reference deintegrate phases. Any leakage or charge loss during these two phases results in an effective change in the scale factor of the ICL7135. Low cost film capacitors such as polyester or polystyrene have been found to be suitable in most applications.

In addition to leakage requirements, another effect that sets a lower limit on the value of the reference capacitor is the "charge suckout" caused by stray capacitance on the reference capacitor terminals. For a negative polarity input signal, the reference capacitor does not shift its common mode voltage, but with a positive polarity input signal it undergoes a negative common mode shift equal to the reference voltage. If there are stray capacitances on the reference capacitor terminals, some of the charge on the reference capacitor will be used to charge these stray capacitances as the reference capacitor makes this common mode voltage shift. This loss of charge reduces the voltage on the reference capacitor, and causes positive polarity signals to have a higher measured result than a corresponding negative voltage. This error can be reduced by minimizing the stray capacitance on the reference capacitor terminals, and by increasing the value of the reference capacitor.

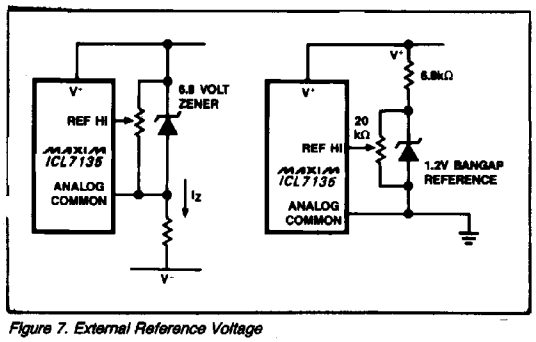


Figure 7. External Reference Voltage

Reference Voltage

The full scale reading of 20,000 will occur when $V_{IN} = 2 \times V_{REF}$. Since the 20,000 count resolution of the ICL7135 is equivalent to a 50ppm resolution, a high stability reference is recommended for high accuracy absolute measurements. Figure 7 shows two suitable methods of generating the reference voltage.

Rollover Resistor and Diode

The ICL7135 is tested for rollover using the circuit of Figure 1, with the 100kΩ resistor and diode in the circuit. The diode is noncritical, and is typically a low cost 1N4148. The resistor value is dependent on many factors including integrator swing, clock frequency, and the amount of rollover error due to "charge suckout" on the reference capacitor. 100kΩ is the optimum value for most circuits and is the value used in testing the ICL7135.

Speedup Resistor

The 27Ω speedup resistor in series with the integrating capacitor adds a pedestal voltage on top of the integrating capacitor voltage. This pedestal voltage causes zero crossing to occur earlier than would occur without the resistor. The effect of the earlier zero crossing is to give the comparator an overdrive voltage, speeding its response and reducing the conversion error due to comparator delay. If the integrator current is changed, the speedup resistor value should be changed so that the $I_{INT} \times R_{SPEEDUP} = 500\mu V$.

Clock Frequency

The clock source should be free of short-term phase and frequency jitter during the conversion period, but long term stability is not critical. The clock frequency is chosen to obtain the desired conversion rate, and to maximize the normal mode rejection of power line frequency interference. The conversion rate is directly proportional to the clock frequency, with each conversion taking 40,002 clock cycles. For maximum normal mode rejec-

tion, the signal integration period should be an integral multiple of the power line cycles.

$$\text{Reading Rate (in readings per second)} = \frac{f_{CLK}}{40{,}002}$$

$$f_{CLK} \text{ for maximum normal mode rejection} = \frac{f_{LINE} \times 10{,}000}{N}$$

Where f_{LINE} is the line frequency, normally 50Hz or 60Hz and N is the number of line cycles that occur during a signal integration period. For maximum normal mode rejection, N should be an integer.

For 60Hz rejection, suitable clock frequencies include 300kHz, 200kHz, 150kHz, 120kHz, 100kHz, and 75kHz. Suitable frequencies for use with 50Hz power include 250kHz, 166⅔kHz, 125kHz, and 100kHz. The two most common clock frequencies are 120kHz (3 readings per second) and 100kHz (2½ readings per second). Note that a 100kHz clock frequency rejects both 50Hz and 60Hz normal mode signals.

The maximum clock rate is limited by the maximum rate at which the digital logic will correctly function (typically 2MHz), and by the speed of response of the comparator. The comparator delay, about 3µs, has the same effect on the measurement result as does an offset voltage with the same polarity of the input signal. At the recommended clock frequency of 120kHz, this small offset is slightly less than ½ count. At higher clock frequencies the value of the speedup resistor in series with the integration capacitor (normally 27Ω) should be increased. At frequencies above 120kHz, ringing on the integrator output may cause nonlinearities in the first few counts.

The minimum clock frequency is limited by the leakage of the auto-zero and reference capacitors. While seldom desired, measurement cycles as long as 10 seconds can be performed with negligible error at room temperature. Figures 8A and 8B show two methods of generating a suitable clock signal for the ICL7135.

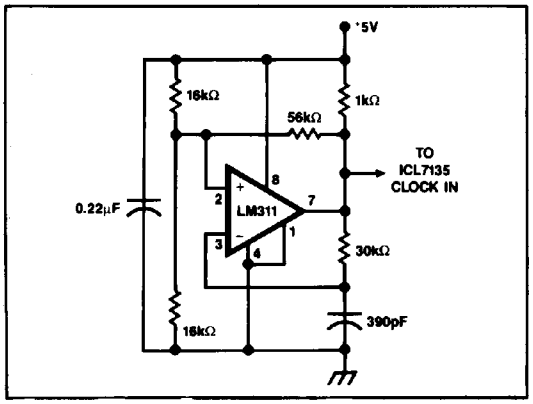


Figure 8A. LM311 Clock Source

Application Hints

Grounds

As with all sensitive analog circuitry, it is important to keep the Digital Ground separate from the analog ground (called Analog Common on the ICL7135) to minimize errors caused by the coupling of noise from the digital circuitry into the sensitive analog section. Analog Common should be connected to Digital Ground at only one point, and return currents from digital loads must not flow through the analog ground lines. Avoid any unnecessary current flow in the analog ground path.

Single 5V Supply Operation

The ICL7135 normally uses ±5V supplies, however, in some applications the negative supply is not needed. Specifically, the negative 5V supply is not required if the input signal can be referenced to the center of the ICL7135's common mode voltage range AND the signal voltage is less than ±1.5V. The integrator swing must be reduced, and there will be a slight increase in system noise and nonlinearity. See Figure 9 for recommended component values.

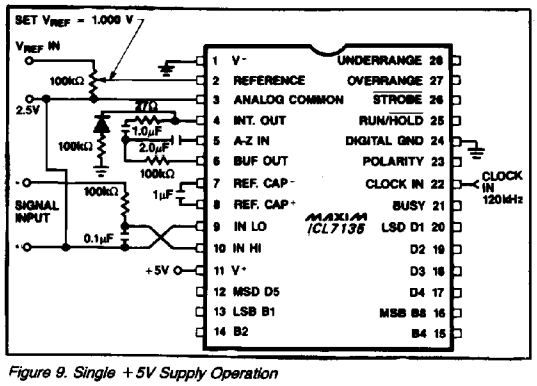


Figure 9. Single +5V Supply Operation

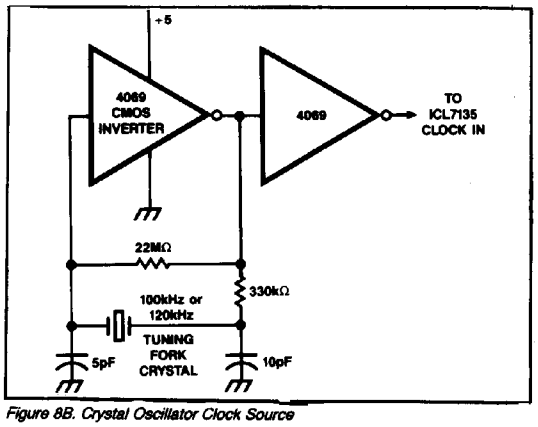


Figure 8B. Crystal Oscillator Clock Source

4½ Digit A/D Converter with Multiplexed BCD Outputs

Generating a Negative Supply from +5V

Figures 10A and 10B show two methods of generating a negative supply for the ICL7135. The Maxim ICL7660 will supply 2mA (the maximum supply current of the ICL7135) at 4.85V drop, while the circuit using the CMOS inverter will deliver approximately −3.5V. If the CMOS inverter is used to generate a minus supply, the integrator swing should be reduced to 2.5 to 3V.

Noise

The normal system noise around zero is about 15μV peak-to-peak (not exceeded 95% of the time). Near full scale, the noise increases to about 30μV. The main noise source is the auto-zero loop, and increasing the value of the auto-zero capacitor will reduce the noise. Other noise sources include the buffer and integrator noise; comparator noise; and stray pickup in the input circuitry, the integrator, and the reference capacitor. The noise caused by stray pickup of interfering signals can be reduced by a tight layout and shielding. If the interfering signal frequency is constant, the effects of stray pickup in the input and integrator can be reduced by choosing a clock frequency such that the signal integration period is an integral multiple of the interfering signal's period. Since the length of the de-integration period depends on the input signal level, no single clock frequency can be chosen to reject interfering signals during the de-integrate phase.

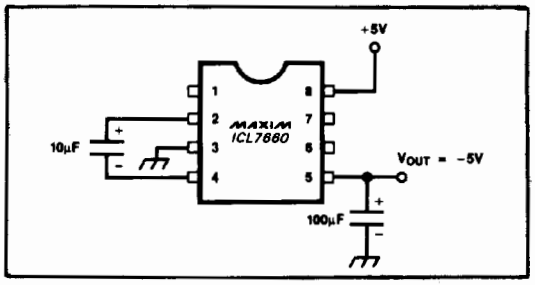


Figure 10A. Generating a Negative Supply

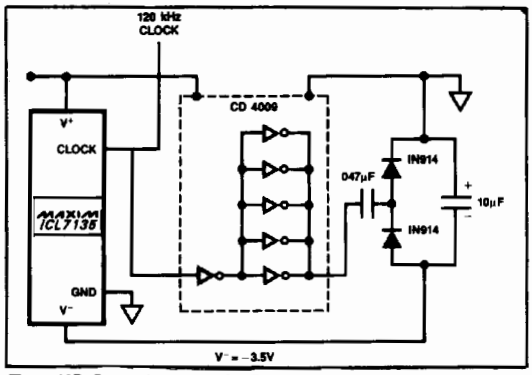


Figure 10B. Generating a Negative Supply

Typical Applications

Figure 11 uses Maxim's ICL7211 LCD display driver to drive 4 digits of LCD display. The backplane signal of the ICL7211 and the CMOS exclusive OR gates are used to drive the ½ digit and the polarity sign. The four AND gates combine the digit outputs with the STROBE output to generate the digit select signals that latch data into the ICL7211. Since the Strobe occurs in the middle of each digit's data there is ample data setup and hold time to ensure that valid data is latched. The OR gates will force the BCD data to all ones when over-range goes high. The ICL7211A will blank the display when all ones (hex F) is loaded.

The typical operating circuit on the first page of this data sheet shows a 4½ digit A/D with LED drive using the Maxim ICL7212 display driver. In this case the polarity and ½ digit segments are driven by D flip-flops that latch polarity and ½ digit data at the end of each measurement. The ICL7135 Overrange output drives the ICM7212 Brightness input, blanking the four least significant digits when the input voltage is greater than full-scale.

Some applications require non-multiplexed, latched BCD outputs. The circuit shown in Figure 12 will demultiplex and latch the ICL7135 output. If only the first rank of latches is used, the data should not be used during the 800 clock cycle update period that takes place at the end of each conversion since during this update period the

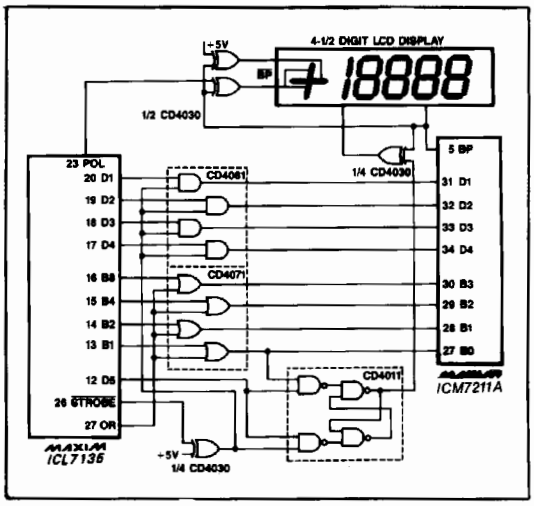


Figure 11. LCD Display with Digit Blanking on Overrange

most significant digit (MSD) data will correspond to the new reading and the least significant digit (LSD) data will be old data from the previous converison. The second rank of latches shown in dotted lines will eliminate this problem by updating all digits simultaneously with the rising edge of D5.

There are many different possible ways of interfacing the ICL7135 to a microprocessor. Figure 13 shows a method that uses only 8 I/O lines. The digit outputs drive a priority encoder, which converts the 1-of-5 format of the digit outputs to a 3 bit binary code. When no digit is active (as in over-range), the binary output code is 0, otherwise the output corresponds to the digit number of the active digit. By sensing BUSY as either an input or as an interrupt, the microprocessor can detect when new data is available.

Another possible interface scheme is to sense only digit D5, then use time delays to choose when to read the other digits' data.

Interfacing With UARTs and Microprocessors

Figure 14 shows a simple interface between a UART and a free running ICL7135. The transmission of the five data words is started by the five STROBE pulses. The digit 5 word is 0000XXXX, digit 4 is 1000XXXX, digit 3 is 0100XXXX, etc. The polarity is transmitted indirectly by using it to drive the Even Parity Enable Pin (EPE). A parity flag at the receiver can be decoded as a positive signal, no flag as negative, if EPE of the receiver is held low. Figure 15 shows a more complex arrangement. DR goes high when the UART receives a byte via the send input, $\overline{RRI}$. Since DR is connected to the ICL7135's RUN/$\overline{HOLD}$ input this starts a new conversion. At the end of the conversion the falling edge of BUSY resets DR via the UART's DRR input. The transmit sequence is again started by STROBE. A quad 2-input multiplexer is used to superimpose polarity, over-range, and under-range onto the D5 word since in this instance it is known that $B_2 = B_4 = B_8 = 0$.

To insure proper operation, it is necessary that the UART clock be fast enough that each word is transmitted before the next STROBE pulse arrives.

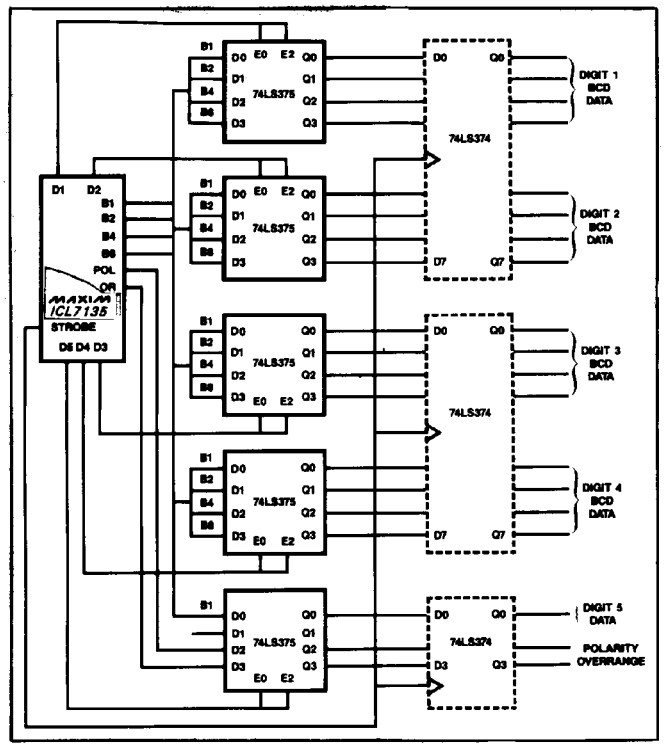


Figure 12. Non-Multiplexed, Latched BCD Output

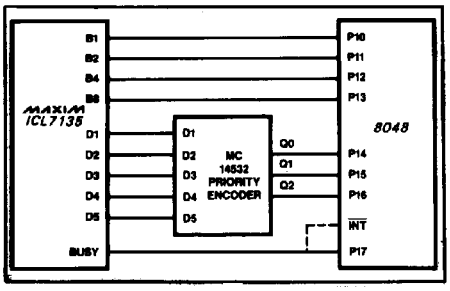


Figure 13. µP Interface

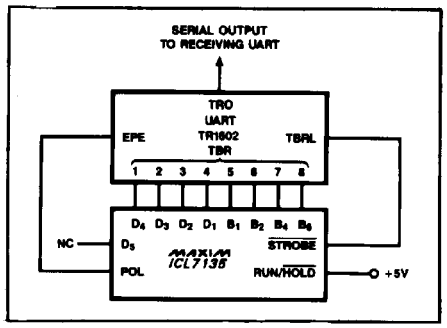


Figure 14. ICL7135 to UART Interface

4½ Digit A/D Converter with Multiplexed BCD Outputs

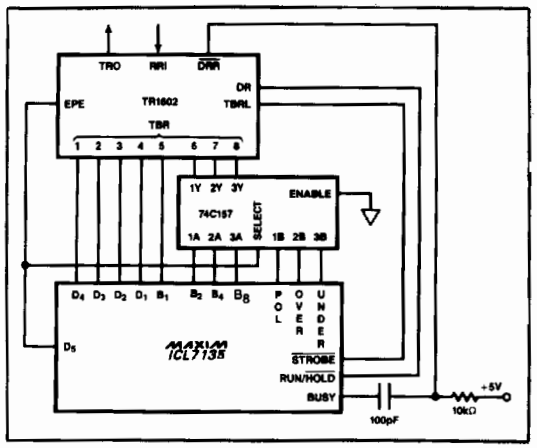
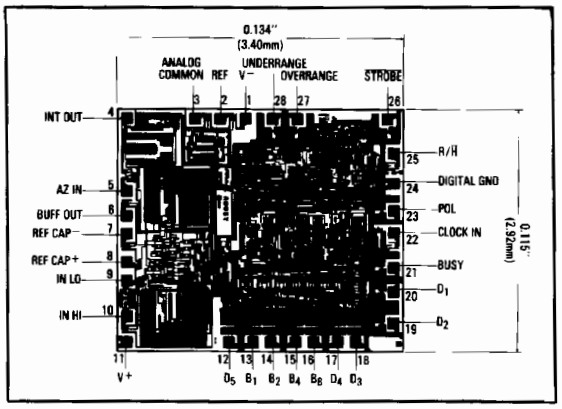
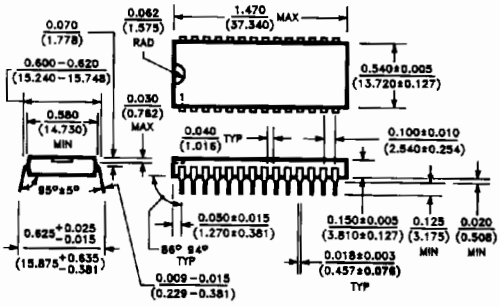


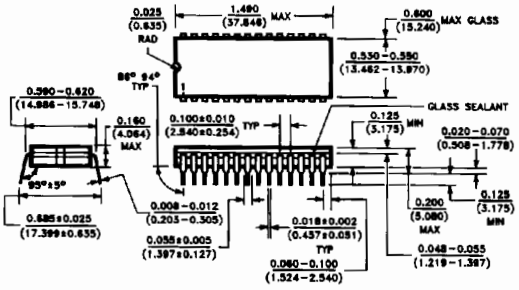
Figure 15. Complex ICL7135 to UART Interface

Chip Topography

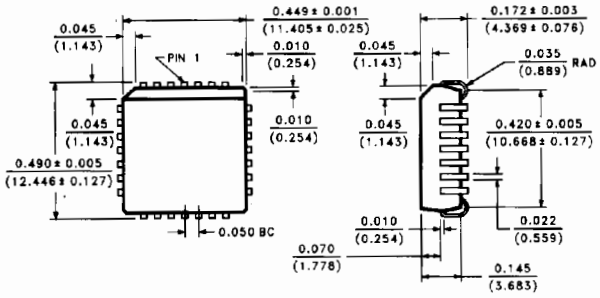




28 Lead Plastic (PI)
θ_{JA} = 110°C/W, θ_{JC} = 50°C/W



28 Lead Cerdip (JI)
θ_{JA} = 55°C/W



28 Lead Plastic Chip Carrier (Quad Pak) (Q)

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