UT165
Advanced USB2.0 Flash Drive Controller

Datasheet

Rev. 2.2

Jan. 29, 2008

AFA TECHNOLOGIES, INC.

http://www.afatech.com

Revision History

Date	Rev	Description
Sep. 26, 2007	1.0	Initial release
Dec. 10, 2007	1.1	Update “Chapter 7 Electrical Characteristics” data based on lab measurement data
Jan. 17, 2008	2.0	Update company name and logo Update dual channel mode with 4CE flash supported on 48pin packages
Jan. 29, 2008	2.2	Update flash chip enable.

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1 Overview

1.1 Description

UT165 is an Advanced Hi-speed USB Flash Disk Controller intended for supporting new introduced 4KB page flash memories, which need enhanced error correction engine supported devices.

UT165 had been designed as pin-to-pin compatible with UT168/UT166/UT161/UT163. With flexible firmware code design, all of the comprehensive flash technologies can be supported, including Single Level Cell (SLC), Mutli-Level Cell (MLC) NAND Flash, AG-AND, and ORNAND flash memory. It allows the manufacturers to improve device performance or power consumption via maximized flexibility in flash selection.

UT165 is a highly integrated single chip solution for USB2.0 Flash Disk controller, including USB2.0 Transceiver Macrocell Interface (UTMI), the Serial Interface Engine (SIE), one cycle 8032 compatible 8-bit micro-controller, 8/14-bit ECC engine and voltage regulators. The highly integration reduces overall cost by minimizing component amount. Employed leading 0.16um CMOS technology, UT165 is the most cost and power efficient solution for manufacture.

There are hardware and software write-protect capability embedded into UT165 design to prevent writing data into flash memory unexpectedly. One LED indicator pin to show access status by three operation modes, Busy, Waiting and OFF. The embedded Auto-Run function enables comprehensive driver free applications. With provided utility and mass production tool, some best value-added functions can be supported by UT165 controller, such as customized VID/PID/Serial Number, disk partitions, boot function, and the security function to protect the data against forbid access with password identification.

Complied with USB specification rev. 2.0, UT165 can be supported without additional driver on Windows ME/2000/XP/Vista, Mac OS 9.x above and Linux Kernel 2.4 above. With device driver installed, it can be supported on Windows 98/98SE as well. UT165 is available in 64, 48 and 46pin packages, and 16/6/4 “CE” pins available respectively.

1.2 Product Information

Part No	Description	Package Type
UT165-L64	Enhanced USB2.0 Flash Drive Controller NAND flash single/dual channel access Green Process without special specify	64Pin LQFP 7x7x1.4 mm
UT165-T64		64Pin TQFP 7x7x1.0 mm
UT165-L48		48Pin LQFP 7x7x1.4 mm
UT165-T48		48Pin TQFP 7x7x1.0 mm
UT165-Q46		46Pin QFN 6.5x4.5x0.8 mm
UT165-D1		Die form

2 Features

- **Flash support**
  - Supports 4KB and 2KB page flashes, including SLC/MLC NAND, AG-AND and ORNAND flashes
  - Integrated ECC circuits for **8-bit/512Bytes and 14-bit/512Bytes BCH error correction**
  - Support NAND flash word and byte access for both 3.3V and 1.8V flashes
  - Dual-channel, interleave and multi-plane mode support to achieve best performance
  - Supports flash chip up to 16 “CE” pins
  - Embedded “Dynamic Wear-Leveling” algorithm to have flash data WRITE to be evenly distributed over the storage area and the end product life time will be extended
- **8032 8-bit Micro-controller with one clock per instruction cycle design**
- **USB Interface**
  - High-speed USB 2.0 interface; backward compatible with USB 1.1
  - Integrated USB 2.0 Transceiver Macrocell Interface (UTMI) and Serial Interface Engine (SIE)
- **Software patch free to implement “User Mode” protocol**
- **Multi-Partition feature**
  - One Read-Only partition is designated for Auto-Run feature
  - One or two public partitions with our without security partition
  - One public partition plus Auto-Run feature with or without security partition
  - Security partition can be protected by password
  - Capacity configuration of each partition can be done while factory initialization or by companion utility
- **Hardware Write-Protect switch for security purpose**
- **LED indicator to show three different access status, Busy, Waiting, and Off**
- **Integrated 5V to 3.3V/1.8V voltage regulator to provide 3.3V for pad and 1.8 V for core operation**
- **Companion user friendly utilities**
- **Customized VID/PID and serial number**
- **Supports Windows 98SE/ME/2000/XP/Vista, Mac 9.x above and Linux kernel 2.4 above**

3 Application Notes

■UT165 L64/T64/L48/T48/Q46 packages are backward compatible with UT163

UT163 Package Type	UT165 Package Type	Notes
UT163-L6	UT165-L64	64Pin LQFP 7x7x1.4 mm
UT163-T6	UT165-T64	64Pin TQFP 7x7x1.0 mm
UT163-L4	**TBD***	48Pin LQFP 7x7x1.4 mm
UT163-T4	**TBD***	48Pin TQFP 7x7x1.0 mm
UT163-LQ4	UT165-L48	48Pin LQFP 7x7x1.4 mm
UT163-TQ4	UT165-T48	48Pin LQFP 7x7x1.0 mm
UT163-Q4	**TBD***	46Pin QFN 6.5x4.5x**0.7** mm
UT163-QF4	UT165-Q46	46Pin QFN 6.5x4.5x**0.8** mm
UT163-LH	**TBD**	80Pin LQFP 10x10x1.4 mm

* : Recommend to stay at UT163 for continuous service.

■UT165 with 16CE support will be 64pin package default setting. All the other packages are the same as UT163

■4CE flash at dual channel mode will be supported on UT165-L48/T48 as well as UT163/165 64pin packages

Package Type	Flash Access Channel	Available CE Pins	Notes
L64/T64	Single	CH0: CE0, CE2, CE4, CE6, GPIO0, GPIO2, GPIO4, GPIO6	Support 4CE flash
	Dual	CH0: CE0, CE2, CE4, CE6, GPIO0, GPIO2, GPIO4, GPIO6 CH1: CE1, CE3, CE5, CE7, GPIO1, GPIO3, GPIO5, GPIO7	Support 4CE flash
Q46	Single	CH0: CE0, CE2	
	Dual	CH0: CE0, CE2 CH1: CE1, CE3	
L48/T48*	Single	CH0: CE0, CE2, CE4, CE6	For 4CE flash only
	Dual	CH0: CE0, CE2, CE4, CE6 CH1: CE0, CE2, CE4, CE6	
L48/T48	Single	CH0: CE0, CE2	For 1CE or 2CE flash
	Dual	CH0: CE0, CE2 CH1: CE1, CE3	

*This solution is designed for 4CE flash.

■Package vs. CE pin vs. applicable flash type table

Part Number	Total CE Pin Number		Max. Support Flash Number					
			Single Channel Application			Dual Channel Application		
	CH0	CH1	4 CE	2 CE	1 CE	4 CE	2 CE	1 CE
UT165-L64/T64	8	8	2	4	8	4	8	16
UT165-L48/T48	4	2	1*	2	4	2*	2	4
UT165-Q46	2	2	0	1	2	0	2	4

* Please refer to your Afa Technologies FAE for 4CE flash selection.

■4KB per page flash support status

Part Number	SLC		MLC		Notes
	Dual Channel	Single Channel	Dual Channel	Single Channel	
UT165	V	V	V	V	
UT163-A1B	V	V	NA	V	
UT163-Q0A	NA	NA	NA	NA	

4 Block Diagram

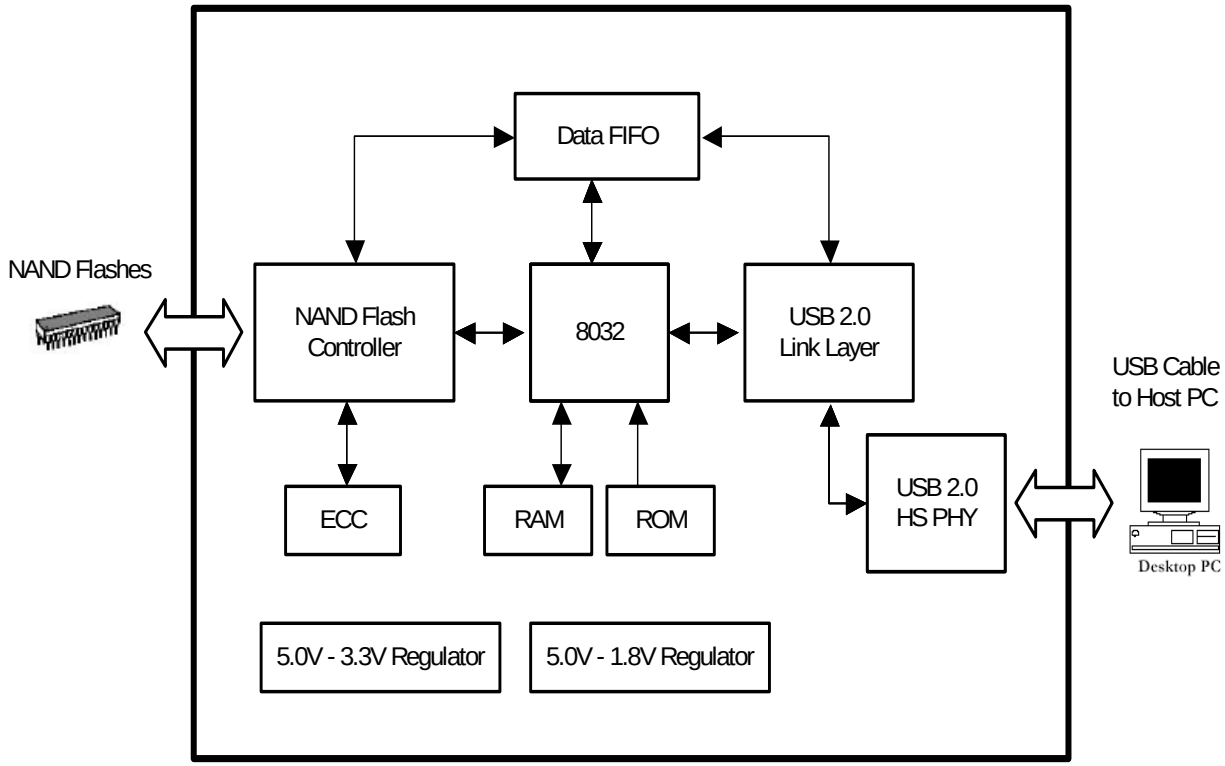
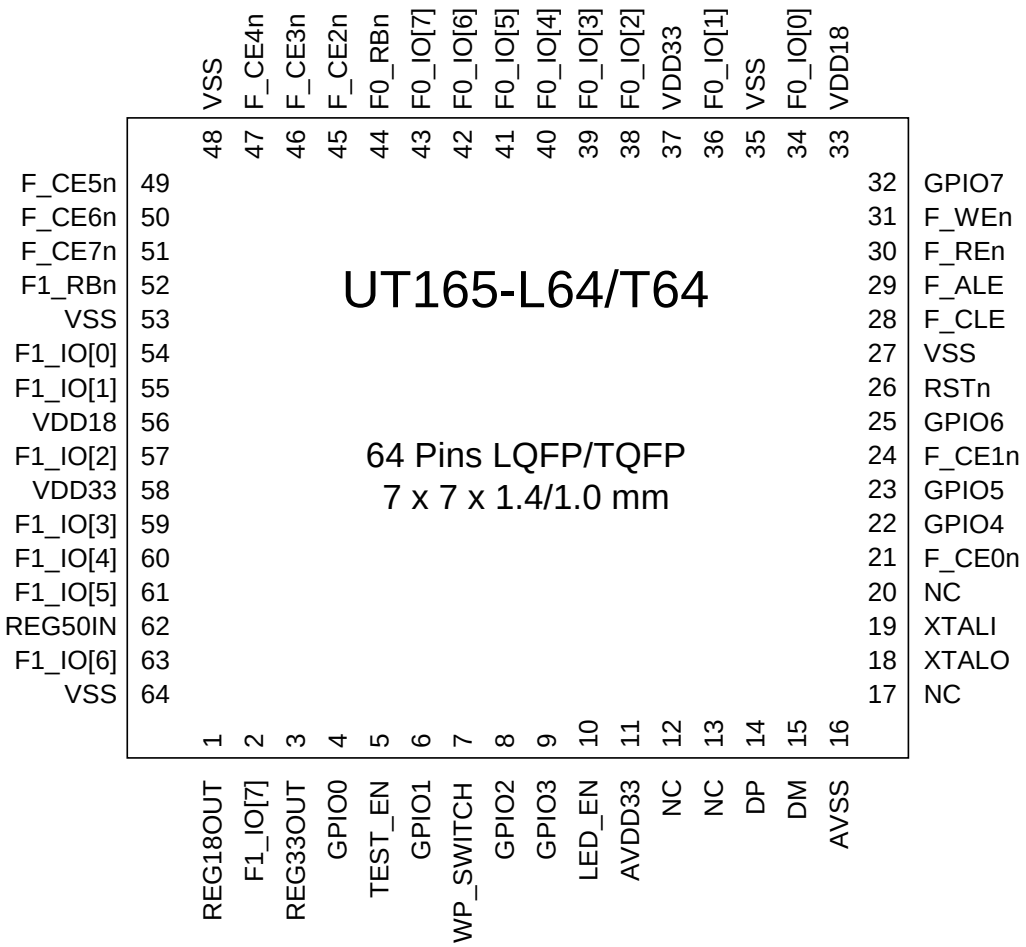


Figure 1 Block Diagram

5 Pin Assignment

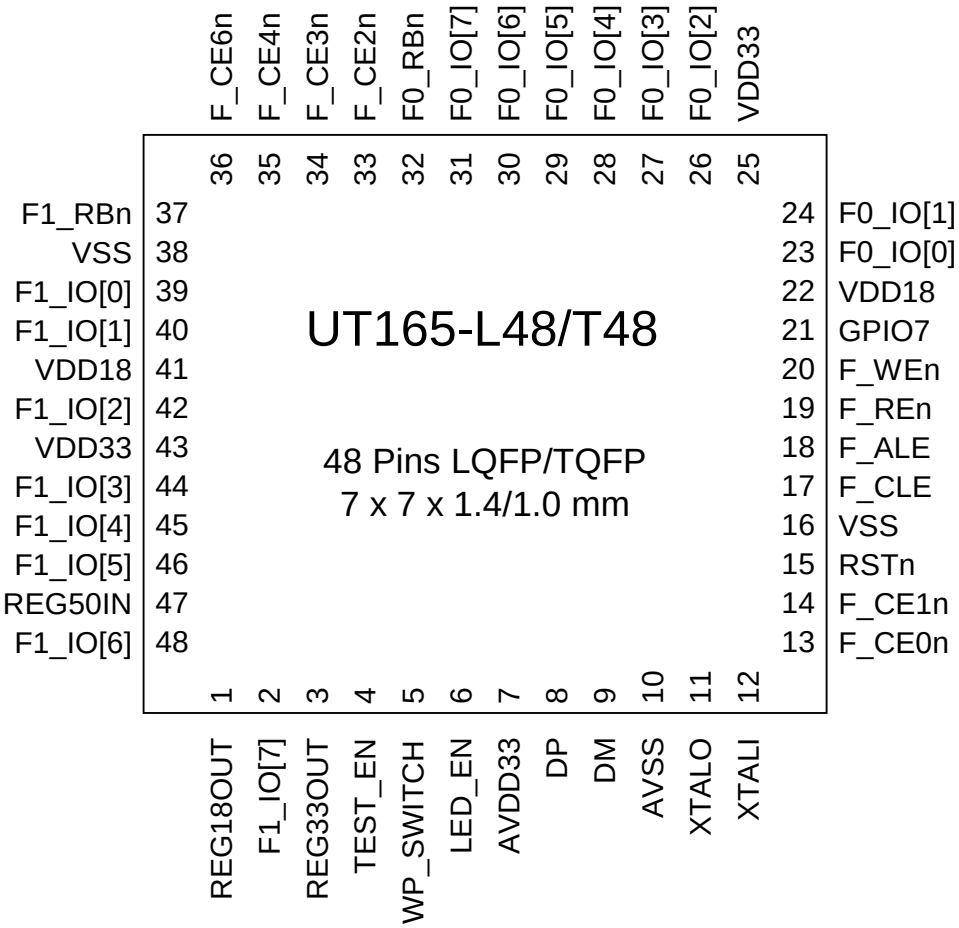
5.1 UT165-L64/T64 64Pin LQFP/TQFP Pin Assignment

Figure 2 UT165-L64/T64 Pin Assignment



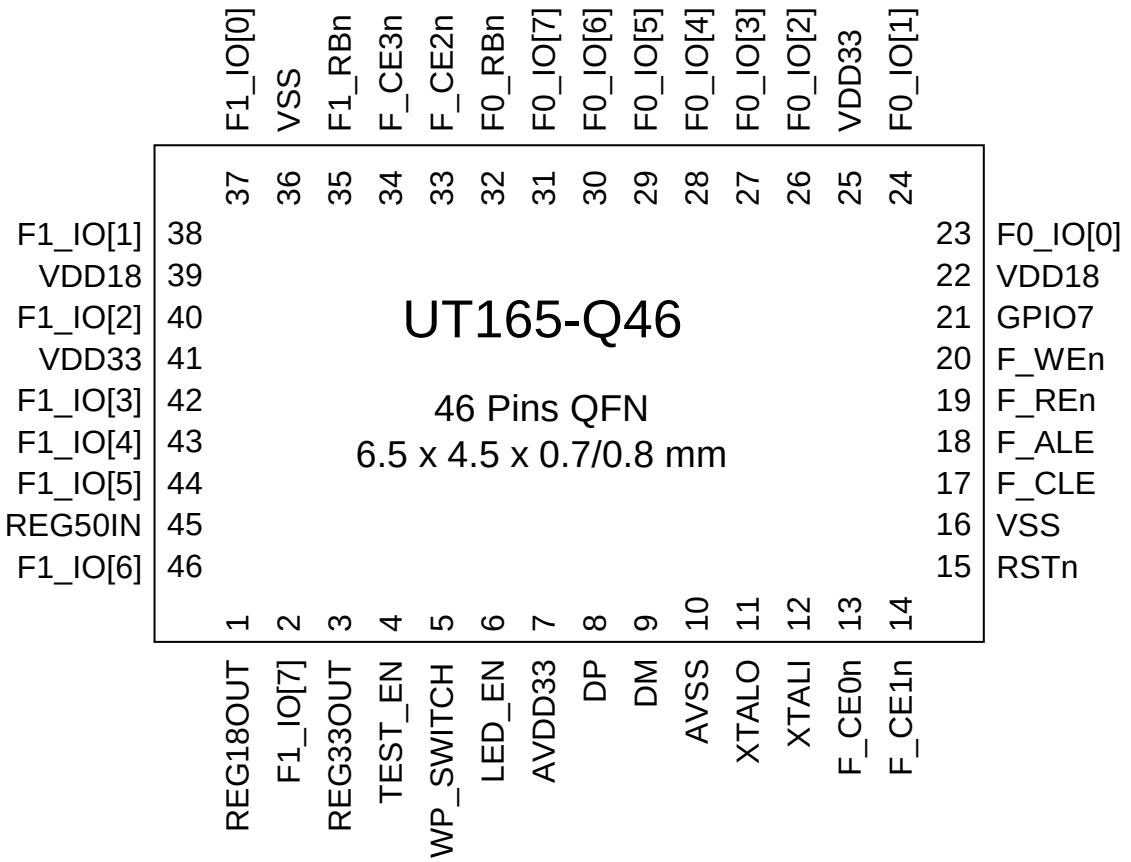
5.2 UT165-L48/T48 48Pin LQFP/TQFP Pin Assignment

Figure 3 UT165-L48/T48 Pin Assignment



5.3 UT165-Q46 46Pin QFN Pin Assignment

Figure 4 UT165-Q46 Pin Assignment



6 Pin Description

Brief UT165 pin functions are shown in the following tables.

I : Input signal

O : Output signal

I/O : Bi-direction signal

P : Power or ground signal

- : Not available

6.1 UT165-L64/T64 Pin Description

TABLE 1 UT165-L64/T64 PIN DESCRIPTION

Pin No.	Pin Name	Type	Description
1	REG18OUT	P	Regulator 1.8V Power Out (Connect External Capacitor (10 || 0.1 uF) to Ground)
2	F1_IO[7]	I/O	Group 1 Flash Data Bus - bit 7 or GPIO Bus – Port 1 bit 7
3	REG33OUT	P	Regulator 3.3V Power Out (Connect External Capacitor (10 || 0.1 uF) to Ground)
4	GPIO0	I/O	GPIO Bus – Port 3 bit 0
5	TEST_EN	I	Test Mode Enable Pin
6	GPIO1	I/O	GPIO Bus – Port 3 bit 1
7	WP_SWITCH	I	Write Protect Switch Input (active low)
8	GPIO2	I/O	GPIO Bus – Port 3 bit 2
9	GPIO3	I/O	GPIO Bus – Port 3 bit 3
10	LED_EN	O	LED Indication
11	AVDD33	P	Analog 3.3V Power
12	NC	-	NC
13	NC	-	NC
14	DP	I/O	USB Data Positive Pin
15	DM	I/O	USB Data Negative Pin
16	AVSS	P	Analog Ground
17	NC	-	NC
18	XTALO	O	Crystal Output
19	XTALI	I	Crystal Input (12 MHz)
20	NC	-	NC
21	F_CE0n	O	Flash Chip Enable - Chip 0 (active low)
22	GPIO4	I/O	GPIO Bus – Port 3 bit 4

Pin No.	Pin Name	Type	Description
23	GPIO5	I/O	GPIO Bus – Port 3 bit 5
24	F_CE1n	O	Flash Chip Enable - Chip 1 (active low)
25	GPIO6	I/O	GPIO Bus – Port 3 bit 6
26	F_WPn RSTn	O I	Flash Write Protect (active low) External Reset Pin (active low)
27	VSS	P	Logic Ground
28	F_CLE	O	Flash Command Latch Enable
29	F_ALE	O	Flash Address Latch Enable
30	F_REn	O	Flash Read Enable (active low)
31	F_WEn	O	Flash Write Enable (active low)
32	GPIO7	I/O	GPIO Bus – Port 3 bit 7
33	VDD18	P	Logic 1.8V Power
34	F0_IO[0]	I/O	Group 0 Flash Data Bus - bit 0
35	VSS	P	Logic Ground
36	F0_IO[1]	I/O	Group 0 Flash Data Bus - bit 1
37	VDD33	P	Logic 3.3V Power
38	F0_IO[2]	I/O	Group 0 Flash Data Bus - bit 2
39	F0_IO[3]	I/O	Group 0 Flash Data Bus - bit 3
40	F0_IO[4]	I/O	Group 0 Flash Data Bus - bit 4
41	F0_IO[5]	I/O	Group 0 Flash Data Bus - bit 5
42	F0_IO[6]	I/O	Group 0 Flash Data Bus - bit 6
43	F0_IO[7]	I/O	Group 0 Flash Data Bus - bit 7
44	F0_RBn	I	Group 0 Flash Ready_Busy (active low)
45	F_CE2n	O	Flash Chip Enable - Chip 2 (active low)
46	F_CE3n	O	Flash Chip Enable - Chip 3 (active low)
47	F_CE4n	O	Flash Chip Enable - Chip 4 (active low)
48	VSS	P	Logic Ground
49	F_CE5n	O	Flash Chip Enable - Chip 5 (active low)
50	F_CE6n	O	Flash Chip Enable - Chip 6 (active low)
51	F_CE7n	O	Flash Chip Enable - Chip 7 (active low)
52	F1_RBn	I	Group 1 Flash Ready_Busy (active low)
53	VSS	P	Logic Ground
54	F1_IO[0]	I/O	Group 1 Flash Data Bus - bit 0 or GPIO Bus – Port 1 bit 0
55	F1_IO[1]	I/O	Group 1 Flash Data Bus - bit 1 or

Pin No.	Pin Name	Type	Description
			GPIO Bus – Port 1 bit 1
56	VDD18	P	Logic 1.8V Power
57	F1_IO[2]	I/O	Group 1 Flash Data Bus - bit 2 or GPIO Bus – Port 1 bit 2
58	VDD33	P	Logic 3.3V Power
59	F1_IO[3]	I/O	Group 1 Flash Data Bus - bit 3 or GPIO Bus – Port 1 bit 3
60	F1_IO[4]	I/O	Group 1 Flash Data Bus - bit 4 or GPIO Bus – Port 1 bit 4
61	F1_IO[5]	I/O	Group 1 Flash Data Bus - bit 5 or GPIO Bus – Port 1 bit 5
62	REG50IN	P	Regulator 5.0V Power In
63	F1_IO[6]	I/O	Group 1 Flash Data Bus - bit 6 or GPIO Bus – Port 1 bit 6
64	VSS	P	Logic Ground

6.2 UT165-L48/T48 Pin Description

TABLE 2 UT165-L48/T48 PIN DESCRIPTION

Pin No.	Pin Name	Type	Description
1	REG18OUT	P	Regulator 1.8V Power Out (Connect External Capacitor (10 || 0.1 uF) to Ground)
2	F1_IO[7]	I/O	Group 1 Flash Data Bus - bit 7
3	REG33OUT	P	Regulator 3.3V Power Out (Connect External Capacitor (10 || 0.1 uF) to Ground)
4	TEST_EN	I	Test Mode Enable Pin
5	WP_SWITCH	I	Write Protect Switch Input (active low)
6	LED_EN	O	LED Indication
7	AVDD33	P	Analog 3.3V Power
8	DP	I/O	USB Data Positive Pin
9	DM	I/O	USB Data Negative Pin
10	AVSS	P	Analog Ground
11	XTALO	O	Crystal Output
12	XTALI	I	Crystal Input (12 MHz)
13	F_CE0n	O	Flash Chip Enable - Chip 0 (active low)
14	F_CE1n	O	Flash Chip Enable - Chip 1 (active low)

Pin No.	Pin Name	Type	Description
15	F_WPn	O	Flash Write Protect (active low)
	RSTn	I	External Reset Pin (active low)
16	VSS	P	Logic Ground
17	F_CLE	O	Flash Command Latch Enable
18	F_ALE	O	Flash Address Latch Enable
19	F_REn	O	Flash Read Enable (active low)
20	F_WEn	O	Flash Write Enable (active low)
21	GPIO7	I/O	GPIO Bus – Port 3 bit 7
22	VDD18	P	Logic 1.8V Power
23	F0_IO[0]	I/O	Group 0 Flash Data Bus - bit 0
24	F0_IO[1]	I/O	Group 0 Flash Data Bus - bit 1
25	VDD33	P	Logic 3.3V Power
26	F0_IO[2]	I/O	Group 0 Flash Data Bus - bit 2
27	F0_IO[3]	I/O	Group 0 Flash Data Bus - bit 3
28	F0_IO[4]	I/O	Group 0 Flash Data Bus - bit 4
29	F0_IO[5]	I/O	Group 0 Flash Data Bus - bit 5
30	F0_IO[6]	I/O	Group 0 Flash Data Bus - bit 6
31	F0_IO[7]	I/O	Group 0 Flash Data Bus - bit 7
32	F0_RBn	I	Group 0 Flash Ready_Busy (active low)
33	F_CE2n	O	Flash Chip Enable - Chip 2 (active low)
34	F_CE3n	O	Flash Chip Enable - Chip 3 (active low)
35	F_CE4n	O	Flash Chip Enable - Chip 4 (active low)
36	F_CE6n	O	Flash Chip Enable - Chip 6 (active low)
37	F1_RBn	I	Group 1 Flash Ready_Busy (active low)
38	VSS	P	Logic Ground
39	F1_IO[0]	I/O	Group 1 Flash Data Bus - bit 0
40	F1_IO[1]	I/O	Group 1 Flash Data Bus - bit 1
41	VDD18	P	Logic 1.8V Power
42	F1_IO[2]	I/O	Group 1 Flash Data Bus - bit 2
43	VDD33	P	Logic 3.3V Power
44	F1_IO[3]	I/O	Group 1 Flash Data Bus - bit 3
45	F1_IO[4]	I/O	Group 1 Flash Data Bus - bit 4
46	F1_IO[5]	I/O	Group 1 Flash Data Bus - bit 5
47	REG50IN	P	Regulator 5.0V Power In
48	F1_IO[6]	I/O	Group 1 Flash Data Bus - bit 6

6.3 UT165-Q46 Pin Description

TABLE 3 UT165-Q46 PIN DESCRIPTION

Pin No.	Pin Name	Type	Description
1	REG18OUT	P	Regulator 1.8V Power Out (Connect External Capacitor (10 || 0.1 uF) to Ground)
2	F1_IO[7]	I/O	Group 1 Flash Data Bus - bit 7
3	REG33OUT	P	Regulator 3.3V Power Out (Connect External Capacitor (10 || 0.1 uF) to Ground)
4	TEST_EN	I	Test Mode Enable Pin
5	WP_SWITCH	I	Write Protect Switch Input (active low)
6	LED_EN	O	LED Indication
7	AVDD33	P	Analog 3.3V Power
8	DP	I/O	USB Data Positive Pin
9	DM	I/O	USB Data Negative Pin
10	AVSS	P	Analog Ground
11	XTALO	O	Crystal Output
12	XTALI	I	Crystal Input (12 MHz)
13	F_CE0n	O	Flash Chip Enable - Chip 0 (active low)
14	F_CE1n	O	Flash Chip Enable - Chip 1 (active low)
15	F_WPn RSTn	O I	Flash Write Protect (active low) External Reset Pin (active low)
16	VSS	P	Logic Ground
17	F_CLE	O	Flash Command Latch Enable
18	F_ALE	O	Flash Address Latch Enable
19	F_REn	O	Flash Read Enable (active low)
20	F_WEn	O	Flash Write Enable (active low)
21	GPIO7	I/O	GPIO Bus – Port 3 bit 7
22	VDD18	P	Logic 1.8V Power
23	F0_IO[0]	I/O	Group 0 Flash Data Bus - bit 0
24	F0_IO[1]	I/O	Group 0 Flash Data Bus - bit 1
25	VDD33	P	Logic 3.3V Power
26	F0_IO[2]	I/O	Group 0 Flash Data Bus - bit 2
27	F0_IO[3]	I/O	Group 0 Flash Data Bus - bit 3
28	F0_IO[4]	I/O	Group 0 Flash Data Bus - bit 4
29	F0_IO[5]	I/O	Group 0 Flash Data Bus - bit 5

Pin No.	Pin Name	Type	Description
30	F0_IO[6]	I/O	Group 0 Flash Data Bus - bit 6
31	F0_IO[7]	I/O	Group 0 Flash Data Bus - bit 7
32	F0_RBn	I	Group 0 Flash Ready_Busy (active low)
33	F_CE2n	O	Flash Chip Enable - Chip 2 (active low)
34	F_CE3n	O	Flash Chip Enable - Chip 3 (active low)
35	F1_RBn	I	Group 1 Flash Ready_Busy (active low)
36	VSS	P	Logic Ground
37	F1_IO[0]	I/O	Group 1 Flash Data Bus - bit 0
38	F1_IO[1]	I/O	Group 1 Flash Data Bus - bit 1
39	VDD18	P	Logic 1.8V Power
40	F1_IO[2]	I/O	Group 1 Flash Data Bus - bit 2
41	VDD33	P	Logic 3.3V Power
42	F1_IO[3]	I/O	Group 1 Flash Data Bus - bit 3
43	F1_IO[4]	I/O	Group 1 Flash Data Bus - bit 4
44	F1_IO[5]	I/O	Group 1 Flash Data Bus - bit 5
45	REG50IN	P	Regulator 5.0V Power In
46	F1_IO[6]	I/O	Group 1 Flash Data Bus - bit 6

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Extended exposure to the maximum ratings might degrade device reliability. Although UT165 has protective circuitry to resist damage from electrostatic discharge (ESD), precautions should always be taken to avoid high voltage or electric field.

TABLE 4 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit	Notes
Tstorage	Storage Temperature	-40	85	°C	
Ta	Ambient Operating Temperature	0	75	°C	
REG33OUT	3.3V Supply Voltage	-0.3	3.6	V	
REG18OUT	1.8V Supply Voltage	-0.3	2	V	
VDD33	3.3V Buffer Input Voltage	-0.3	3.6	V	
REG50IN	3.3V/5V Buffer Input Voltage	-0.3	5.5	V	
VDD18	1.8V Buffer Input Voltage	-0.3	2	V	

7.2 Operating Conditions

TABLE 5 OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
REG50IN	USB 5V Supply Voltage	3.2	5.5	V
REG33OUT	3.3V Supply Voltage	3.0	3.6	V
REG18OUT	1.8V Supply Voltage	1.6	2	V

7.3 DC Characteristics

Unless otherwise noted, all test conditions are as follows:

VSS=0V, VDD33=3.3V±5%, VDD18=1.8V±5%

TABLE 6 DC CHARACTERISTICS OF I/O INTERFACE

Symbol	Parameter	Min	Max	Unit
V_{IH_TTL}	TTL Input High Voltage	2	VDD33+0.3	V
V_{IL_TTL}	TTL Input Low Voltage	-0.3	0.8	V
V_{OH_TTL}	TTL Output High Voltage	0.9VDD33		V

Symbol	Parameter	Min	Max	Unit
V_{OL_TTL}	TTL Output Low Voltage		0.45	V
I_{OH_TTL}	TTL Output High Current	-4		mA
I_{OL_TTL}	TTL Output Low Current		4	mA
V_{IH_USB}	USB Input High Voltage for Low-/full-speed	2.0		V
V_{IL_USB}	USB Input Low Voltage for Low-/full-speed		0.8	V
$V_{I\_USB\_DIFF}$	Differential Input Sensitivity for Low-/full-speed	TBD		V
$V_{I\_USB\_CM}$	Differential Common Mode Input Range for Low-/full-speed	0.8	2.5	V
$V_{I\_USB\_HSSQ}$	USB High-speed squelch Input detection threshold	0.1	0.15	V
$V_{I\_USB\_HSDSC}$	USB High-speed disconnect Input detection threshold	0.525	0.625	V
$V_{I\_USB\_HSCM}$	USB High-speed Signaling Common Mode Range	-0.05	0.5	V
V_{OH_USB}	USB Output High Voltage for Low-/full-speed	2.8	3.6	V
V_{OL_USB}	USB Output Low Voltage for Low-/full-speed	0	0.3	V
$V_{OH\_USB\_HS}$	USB Output High Voltage for High-speed	0.36	0.44	V
$V_{OL\_USB\_HS}$	USB Output Low Voltage for High-speed	-0.01	0.01	V
I_{OH_USB}	USB Output High Current for Low-/full-speed	-10		mA
I_{OL_USB}	USB Output Low Current for Low-/full-speed		10	mA
$I_{OH\_USB\_HS}$	USB Output High Current for High-speed	-40		mA
$I_{OL\_USB\_HS}$	USB Output Low Current for High-speed		40	mA

7.4 AC Characteristics

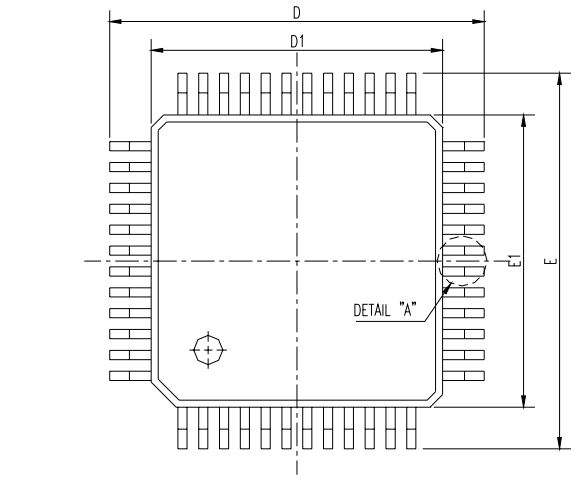
TABLE 7 AC CHARACTERISTICS OF I/O INTERFACE

Symbol	Parameter	Min.	Typ.	Max.	Unit
TP_{ILH}	Input Rising Delay	0.61 (0.8pF)	0.72 (2.4pF)	0.92 (4.8pF)	ns
TP_{IHL}	Input falling Delay	0.88 (0.8pF)	1.03 (2.4pF)	1.24 (4.8pF)	ns
TP_{OLH}	Output Rising Delay	2.40 (10pF)	3.42 (30pF)	4.88 (60pF)	ns
TP_{OHL}	Output falling Delay	2.61 (10pF)	3.62 (30pF)	5.03 (60pF)	ns
TR	Output Rising Time	2.26 (10pF)	4.45 (30pF)	7.83 (60pF)	ns
TF	Output falling Time	1.90 (10pF)	3.63 (30pF)	6.23 (60pF)	ns

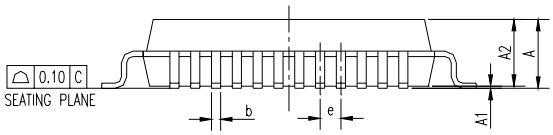
8 Mechanical Dimensions

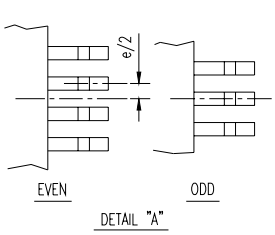
8.1 UT165-L64 64Pin LQFP Package Outline Dimension

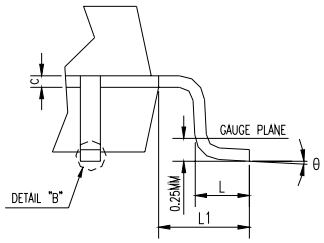
DOC No.: 0064-LQ 7.0X7.0-01-A

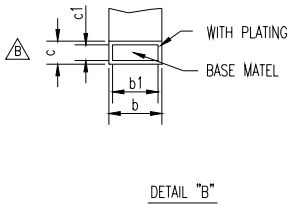


SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	8.90	9.00	9.10	0.350	0.354	0.358
D1	6.90	7.00	7.10	0.272	0.276	0.280
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	6.90	7.00	7.10	0.272	0.276	0.280
B c	0.178 TYP.			0.007 TYP.		
c1	0.127 TYP.			0.005 TYP.		
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	1.00 REF.			0.039 REF.		
θ	0	3.5	7	0	3.5	7
JEDEC						







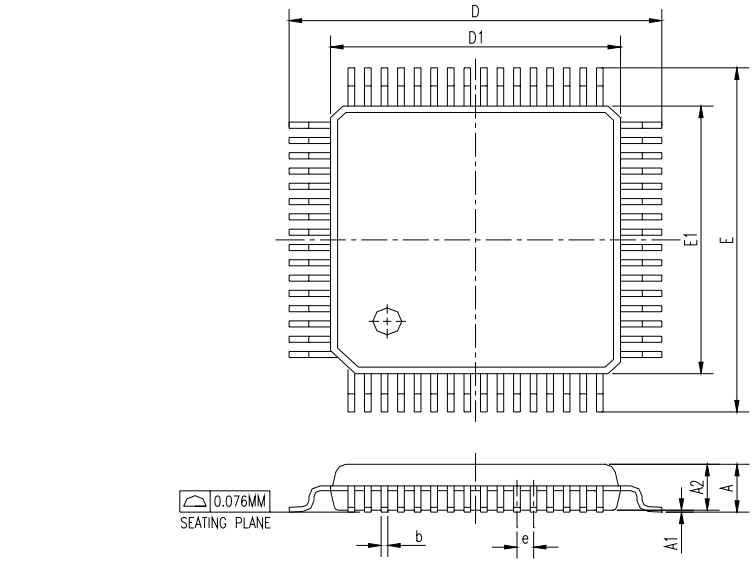


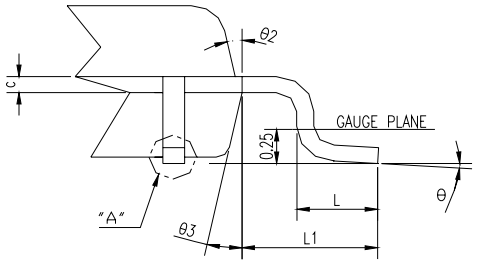
	b (MM)			b1 (MM)			e (MM)			JEDEC
N	MIN.	NOM	MAX.	MIN.	NOM	MAX.	MIN.	NOM	MAX.	
48L	0.19	0.22	0.25	0.17	0.20	0.23		0.50 BSC.		
64L	0.13	0.16	0.19	0.13	0.16	0.19		0.40 BSC.		

Figure 5 64 Pin LQFP 7.0x7.0x1.4 mm Package Outline Dimension

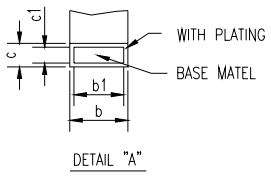
8.2 UT165-T64 64Pin TQFP Package Outline Dimension

DOC No.: 0064-TQ 7.0X7.0-01-A





SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.156			0.046
A1	0.05		0.15	0.002		0.006
A2	0.94	1.00	1.06	0.037	0.039	0.042
c	0.119		0.185	0.005		0.007
c1	0.127 TYP.			0.005 TYP.		
D	8.90	9.00	9.10	0.350	0.354	0.358
D1	6.95	7.00	7.05	0.273	0.276	0.278
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	6.95	7.00	7.05	0.273	0.276	0.278
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	1.00 REF.			0.039 REF.		
θ	1.5	3.5	5.5	1.5	3.5	5.5
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13

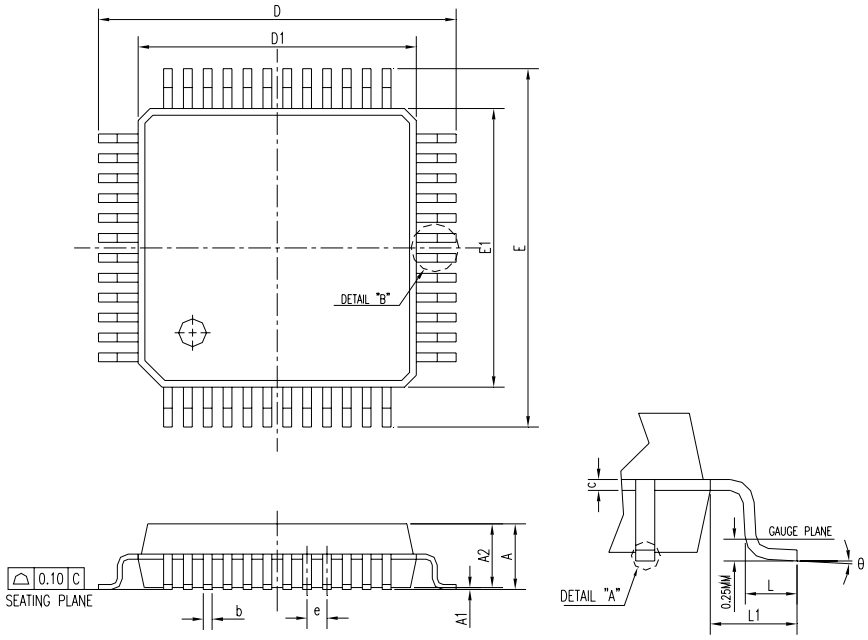


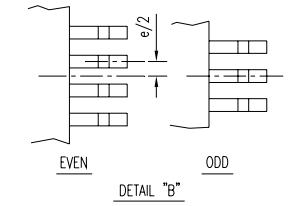
	MIN.	NOM.	MAX.	NOM.	MIN.	MAX.	NOM.	MIN.	MAX.
b	0.34		0.45	0.15		0.26	0.15		0.26
b1	0.34	0.37	0.40	0.15	0.18	0.21	0.15	0.18	0.21
e	0.80BSC.			0.50BSC.			0.40BSC.		
N	32			48			64		
JEDEC	MS-026 ABA			MS-026 ABC			MS-026 ABD		

Figure 6 64 Pin TQFP 7.0x7.0x1.0 mm Package Outline Dimension

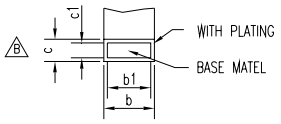
8.3 UT165-L48 48Pin LQFP Package Outline Dimension

DOC No.: 0048-LQ 7.0X7.0-01-A





SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	8.90	9.00	9.10	0.350	0.354	0.358
D1	6.90	7.00	7.10	0.272	0.276	0.280
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	6.90	7.00	7.10	0.272	0.276	0.280
B c	0.178 TYP.			0.007 TYP.		
c1	0.127 TYP.			0.005 TYP.		
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	1.00 REF.			0.039 REF.		
θ	0	3.5	7	0	3.5	7
JEDEC						



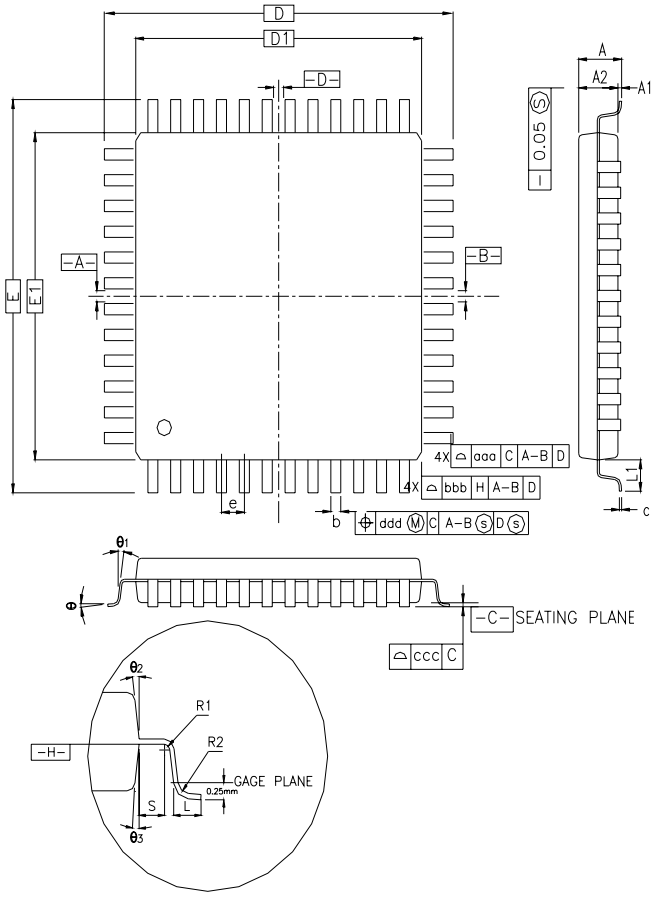
	b (MM)			b1 (MM)			e (MM)			JEDEC
N	MIN.	NOM	MAX.	MIN.	NOM	MAX.	MIN.	NOM	MAX.	
48L	0.19	0.22	0.25	0.17	0.20	0.23	0.50 BSC.			

DETAIL "A"

Figure 7 48 Pin LQFP 7.0x7.0x1.4 mm Package Outline Dimension

8.4 UT165-T48 48Pin TQFP Package Outline Dimension

DOC No.: 0048-TQ7.0X7.0-01-A



SYMBOL	48L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.17	0.22	0.27	0.007	0.009	0.011
e	0.50 BSC.			0.020 BSC.		
	TOLERANCES OF FORM AND POSITION					
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

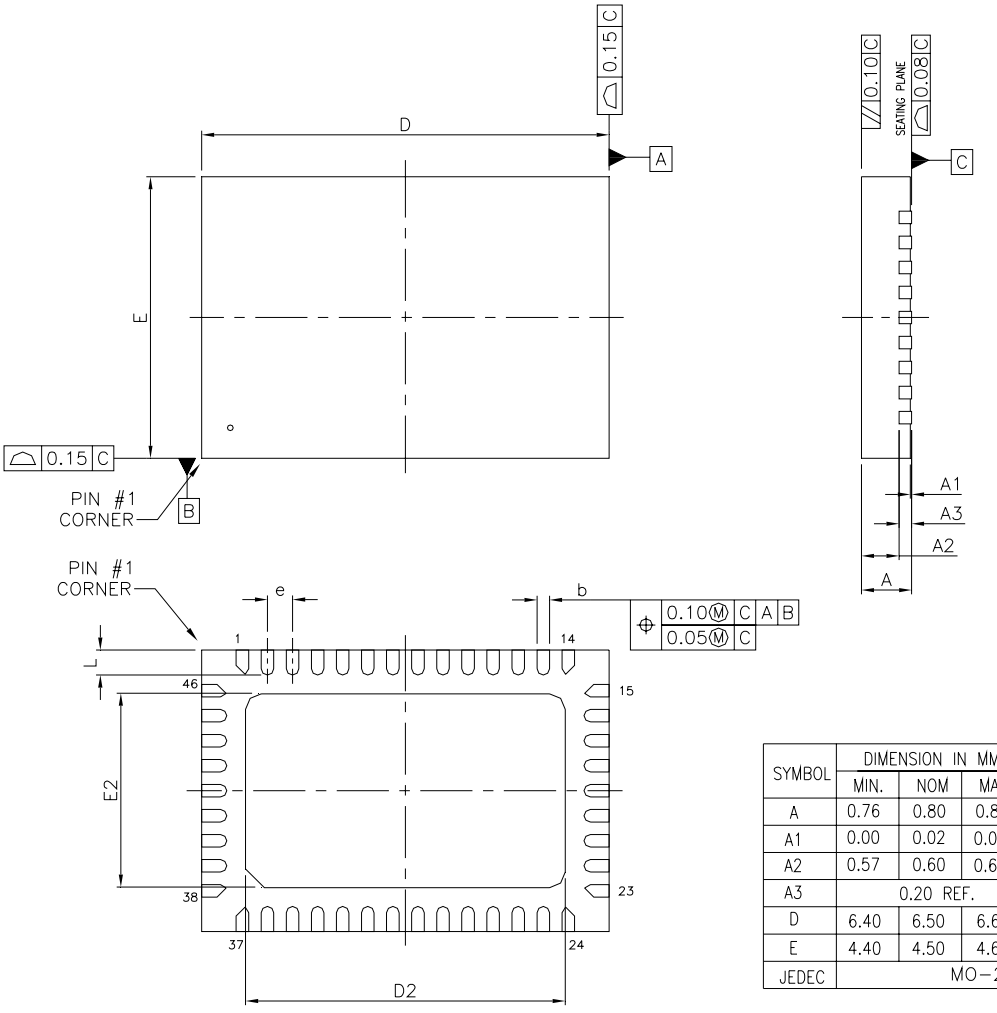
COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A_1	0.05	—	0.15	0.002	—	0.006
A_2	0.95	1.00	1.05	0.037	0.039	0.041
D	9.00 BSC.			0.354 BSC.		
D_1	7.00 BSC.			0.276 BSC.		
E	9.00 BSC.			0.354 BSC.		
E_1	7.00 BSC.			0.276 BSC.		
R_2	0.08	—	0.20	0.003	—	0.008
R_1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

Figure 8 48 Pin TQFP 7.0x7.0x1.0 mm Package Outline Dimension

8.5 UT165-Q46 46Pin QFN Package Outline Dimension

DOC No.: 0046-QF 6.5X4.5-02-A



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	0.76	0.80	0.84	0.030	0.031	0.033
A1	0.00	0.02	0.04	0.0000	0.0008	0.0015
A2	0.57	0.60	0.63	0.022	0.024	0.025
A3	0.20 REF.			0.008 REF.		
D	6.40	6.50	6.60	0.252	0.256	0.260
E	4.40	4.50	4.60	0.173	0.177	0.181
JEDEC	MO-220 (REF.)					

N	b			D2			E2			e	L			JEDEC
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
46L	0.13	0.20	0.25	5.00	5.10	5.20	3.00	3.10	3.20	0.400 BSC	0.30	0.40	0.50	MO-220

Figure 9 46 Pin QFN 6.5 x 4.5 x 0.8 mm Package Outline Dimension

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