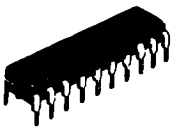
HM6267P-35,HM6267P-45

Preliminary

16384-word x 1-bit High Speed Static CMOS RAM

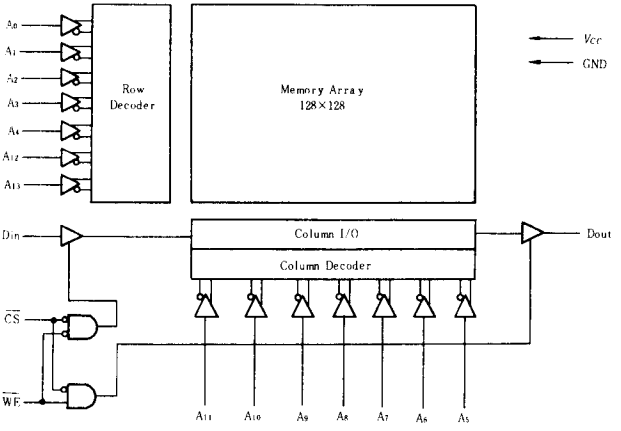
■ FEATURES

- High Speed: Fast Access Time 35/45ns (max.)
- Low Power Standby and Low Power Operation
  Standby: 0.1mW (typ.), Operation: 200mW (typ.)
- Single 5V Supply and High Density 20 Pin Package
- Completely Static Memory ..... No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- Directly TTL Compatible: All Input and Output

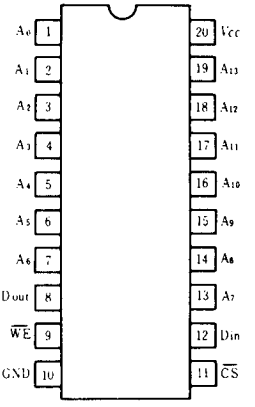


(DP-20)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin*	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

* with respect to GND. V_T min = −3.5V (Pulse width 20ns)

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−3.0*	–	0.8	V

* Pulse Width 20ns, DC: V_{IL} min = −0.5V

Note: The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	High-Z	Write Cycle

■ DC AND OPERATING CHARACTERISTICS(1) (V_{CC} = 5V ±10%(2), GND = 0V, T_a = 0 to +70°C)

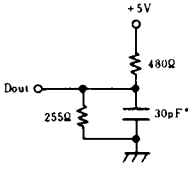
Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{CC} = 5.5V, V_{in} = GND to V_{CC}	–	–	10	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}$ = V_{IH}, V_{out} = GND to V_{CC}	–	–	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, Output Open	–	40	80(3)	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}	–	10	20	mA
	I_{SB1}	$\overline{CS} \geq V_{CC}$-0.2V, $V_{IN} \leq$0.2V or $V_{IN} \geq V_{CC}$-0.2V	–	0.02	2	mA
Output Voltage	V_{OL}	I_{OL} = 8mA	–	–	0.4	V
	V_{OH}	I_{OH} = –4mA	2.4	–	–	V

Notes) 1. Typical limits are at V_{CC} = 5V, T_a = 25°C and specified loading.
2. V_{CC} = 5V±5% for 35ns version.
3. 100mA max. for 35ns version.

■ AC TEST CONDITIONS

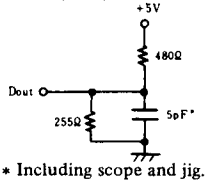
Input pulse levels: GND to 3.0V
Input rise and fall times: 5ns
Input and Output timing reference levels: 1.5V
Output load: See Figure

Output Load A



* Including scope and jig.

Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



* Including scope and jig.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	typ.	max	Unit	Conditions
Input Capacitance	C_{IN}	3	5	pF	V_{IN}=0V
Output Capacitance	C_{OUT}	5	7	pF	V_{OUT}=0V

Note) This parameter is sampled and not 100% tested.

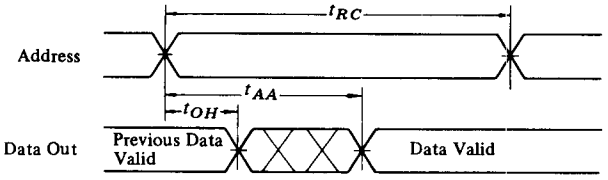
■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%*, T_a = 0 to 70°C, unless otherwise noted.)

● READ CYCLE

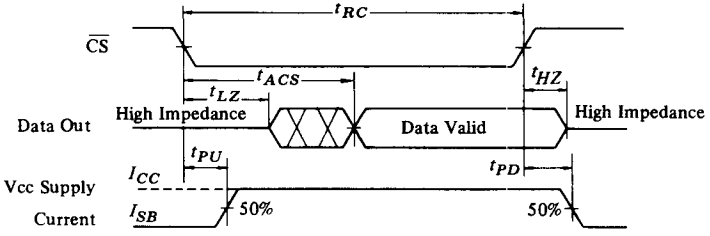
Item	Symbol	HM6267P-35		HM6267P-45		Unit	Notes
		min	max	min	max		
Read Cycle Time	t_{RC}	35	–	45	–	ns	1
Address Access Time	t_{AA}	–	35	–	45	ns	
Chip Select Access Time	t_{ACS}	–	35	–	45	ns	
Output Hold from Address Change	t_{OH}	5	–	5	–	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	ns	2, 3, 7
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	30	ns	2, 3, 7
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	ns	
Chip Deselection to Power Down Time	t_{PD}	–	20	–	30	ns	

* V_{CC} = 5V ± 5% for 35ns version.

● TIMING WAVEFORM OF READ CYCLE NO. 1 [4) 5)]



● TIMING WAVEFORM OF READ CYCLE NO. 2 [4) 6)]

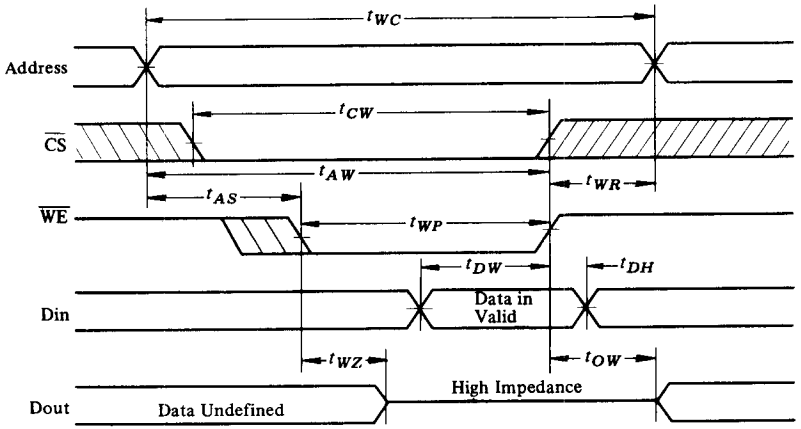


NOTES:
1. All Read Cylce timing are referenced from last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. $\overline{WE}$ is High for READ cycle.
5. Device is continuously selected, $\overline{CS} = V_{IL}$.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.

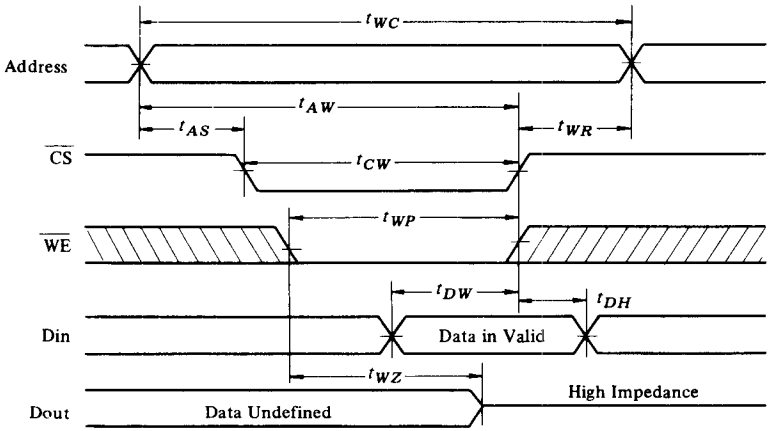
● WRITE CYCLE

Item	Symbol	HM6267P-35		HM6267P-45		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	35	–	45	–	ns	2
Chip Selection to End of Write	t_{CW}	30	–	40	–	ns	
Address Valid to End of Write	t_{AW}	30	–	40	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	ns	
Write Pulse Width	t_{WP}	20	–	25	–	ns	
Write Recovery Time	t_{WR}	0	–	0	–	ns	
Data Valid to End of Write	t_{DW}	20	–	25	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	ns	
Write Enabled to Output in High Z	t_{WZ}	0	20	0	25	ns	3, 4
Output Active from End of Write	t_{OW}	0	–	0	–	ns	3, 4

- **TIMING WAVEFORM OF WRITE CYCLE NO. 1** ($\overline{WE}$ Controlled)



- **TIMING WAVEFORM OF WRITE CYCLE NO. 2** ($\overline{CS}$ Controlled)



NOTES: 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance states.
2. All Write Cycle timings are referenced from the last valid address to the first transitions address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.