

High Current FET Driver

FEATURES

- Totem Pole Output with 6A Source/Sink Drive
- 3ns Delay
- 20ns Rise and Fall Time into 2.2nF
- 8ns Rise and Fall Time into 30nF
- 4.7V to 18V Operation
- Inverting and Non-Inverting Outputs
- Under-Voltage Lockout with Hysteresis
- Thermal Shutdown Protection
- MINIDIP and Power Packages

DESCRIPTION

The UC1710 family of FET drivers is made with a high-speed Schottky process to interface between low-level control functions and very high-power switching devices-particularly power MOSFET's. These devices accept low-current digital inputs to activate a high-current, totem pole output which can source or sink a minimum of 6A.

Supply voltages for both V_{IN} and V_C can independently range from 4.7V to 18V. These devices also feature under-voltage lockout with hysteresis.

The UC1710 is packaged in an 8-pin hermetically sealed dual in-line package for -55°C to $+125^{\circ}\text{C}$ operation. The UC2710 and UC3710 are specified for a temperature range of -40°C to $+85^{\circ}\text{C}$ and 0°C to $+70^{\circ}\text{C}$ respectively and are available in either an 8-pin plastic dual in-line or a 5-pin, TO-220 package. Surface mount devices are also available.

TRUTH TABLE

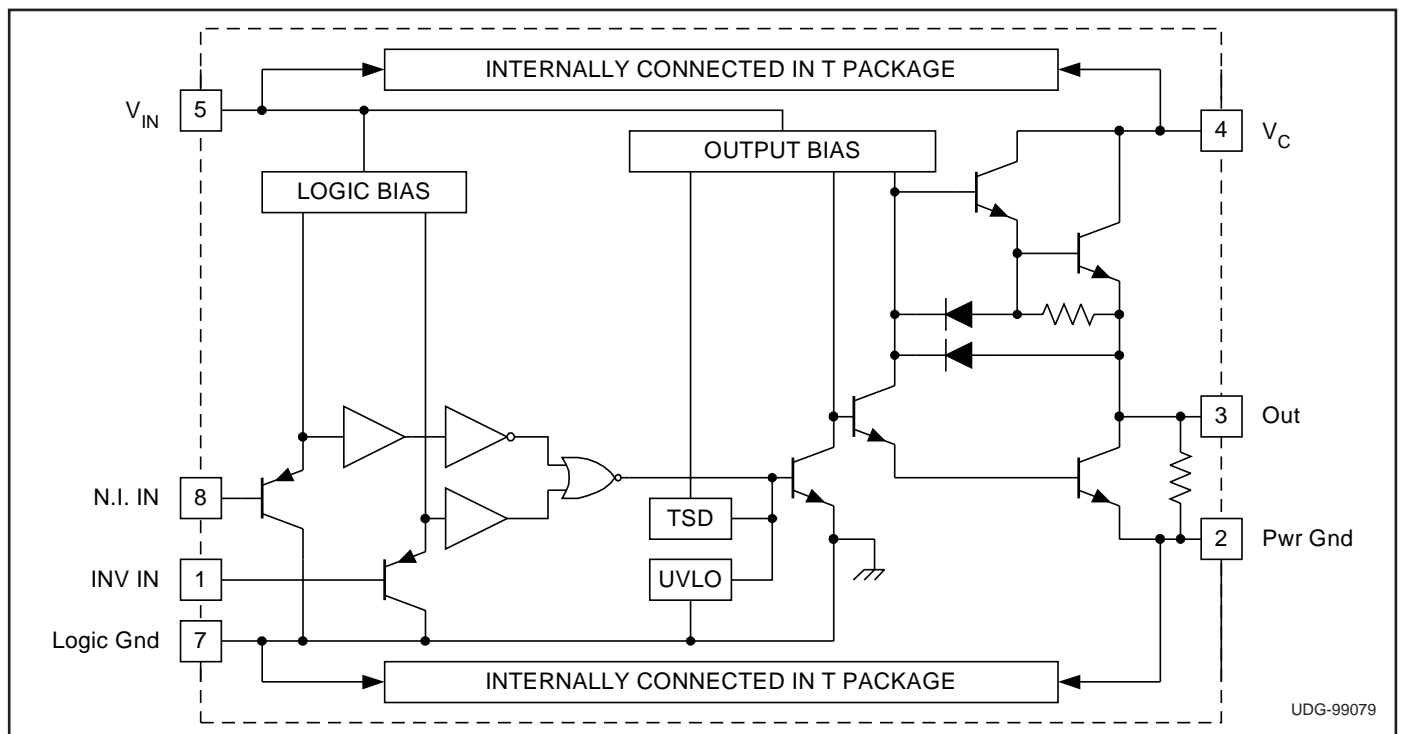
| INV | N.I. | Out |
|-----|------|-----|
| H | H | L |
| L | H | H |
| H | L | L |
| L | L | L |

$\overline{\text{OUT}} = \overline{\text{INV}}$ and $\overline{\text{N.I.}}$
 $\overline{\text{OUT}} = \text{INV}$ or $\overline{\text{N.I.}}$

ORDERING INFORMATION

| | TEMPERATURE RANGE | PACKAGE |
|----------|---|------------------|
| UC1710J | -55°C to $+125^{\circ}\text{C}$ | 8 pin CDIP |
| UC2710DW | -40°C to $+85^{\circ}\text{C}$ | 16 pin SOIC-wide |
| UC2710J | | 8 pin CDIP |
| UC2710N | | 8 pin PDIP |
| UC2710T | | 5 pin TO220 |
| UC3710DW | 0°C to $+70^{\circ}\text{C}$ | 16 pin SOIC-wide |
| UC3710N | | 8 pin PDIP |
| UC3710T | | 5 pin TO220 |

BLOCK DIAGRAM



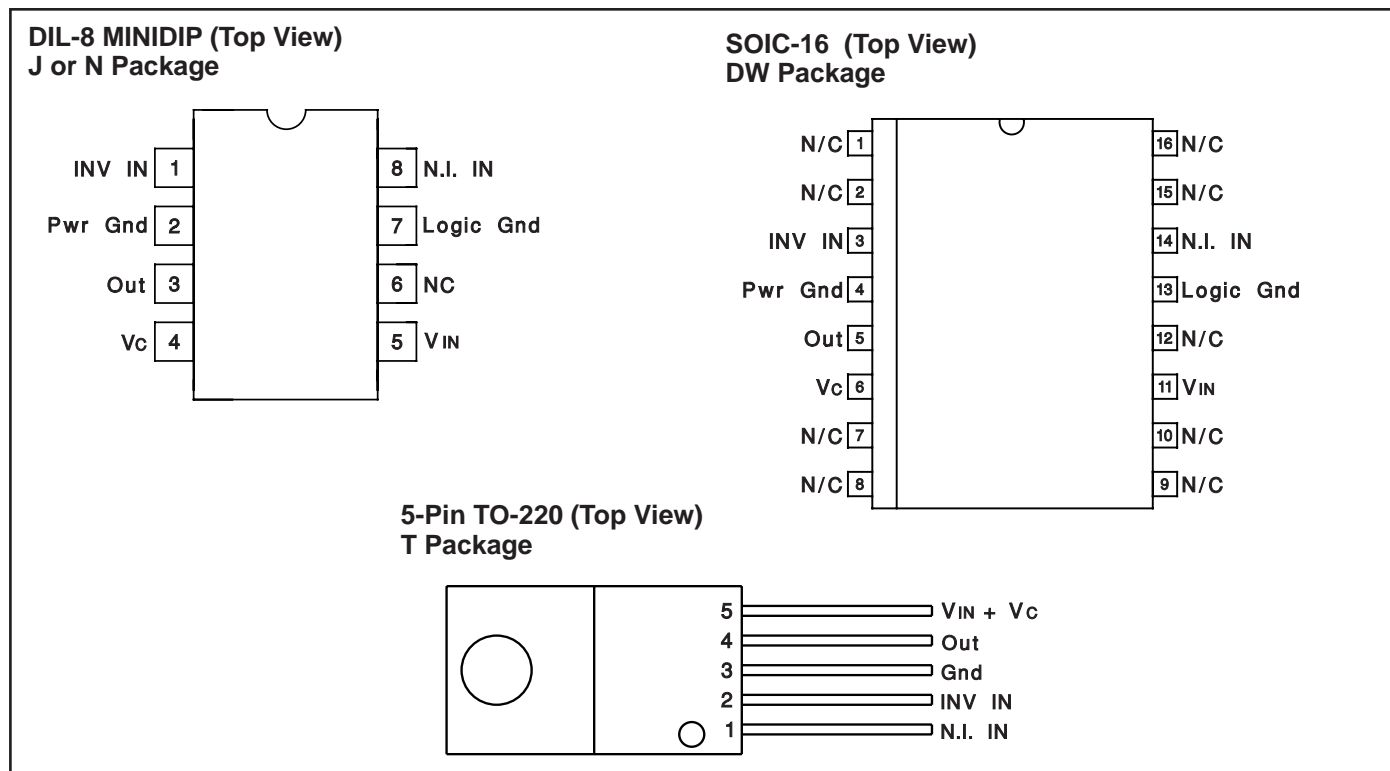
ABSOLUTE MAXIMUM RATINGS

| | N-Package | J-Package | T-Package |
|--|---|---|---|
| Supply Voltage, V_{IN} | 20V | 20V | 20V |
| Collector Supply Voltage, V_C | 20V | 20V | 20V |
| Operating Voltage | 18V | 18V | 18V |
| Output Current (Source or Sink) | | | |
| Steady-State | $\pm 500\text{mA}$ | $\pm 500\text{mA}$ | $\pm 1\text{A}$ |
| Digital Inputs | $-0.3\text{V} - V_{IN}$ | $-0.3\text{V} - V_{IN}$ | $-0.3\text{V} - V_{IN}$ |
| Power Dissipation at $T_a=25^\circ\text{C}$ | 1W | 1W | 3W |
| Power Dissipation at T (Case) = 25°C | 2W | 2W | 25W |
| Operating Junction Temperature | -55°C to $+150^\circ\text{C}$ | -55°C to $+150^\circ\text{C}$ | -55°C to $+150^\circ\text{C}$ |
| Storage Temperature | -65°C to $+150^\circ\text{C}$ | -65°C to $+150^\circ\text{C}$ | -65°C to $+150^\circ\text{C}$ |
| Lead Temperature (Soldering, 10 seconds) | 300°C | 300°C | 300°C |

Note 1: All currents are positive into, negative out of the specified terminal.

Note 2: Consult Unitorde Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

CONNECTION DIAGRAMS



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for $V_{IN} = V_C = 15\text{V}$, No load, $T_A = T_J$.

| PARAMETERS | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------|--|-----|-----|-----|-------|
| V_{IN} Supply Current | $V_{IN}=18\text{V}$, $V_C=18\text{V}$, Output Low | | 26 | 35 | mA |
| | $V_{IN}=18\text{V}$, $V_C=18\text{V}$, Output High | | 21 | 30 | mA |
| V_C Supply Current | $V_{IN}=18\text{V}$, $V_C=18\text{V}$, Output Low | | 1.5 | 5.0 | mA |
| | $V_{IN}=18\text{V}$, $V_C=18\text{V}$, Output High | | 5.0 | 8 | mA |
| UVLO Threshold | V_{IN} High to Low | 3.8 | 4.1 | 4.4 | V |
| | V_{IN} Low to High | 4.1 | 4.4 | 4.8 | V |

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for $V_{IN} = V_C = 15V$, No load,

$T_A = T_J$.

| PARAMETERS | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-------------------------------------|-----|------|-----|-------------|
| UVLO Threshold Hysteresis | | 0.1 | 0.3 | 0.5 | V |
| Digital Input Low Level | | | | 0.8 | V |
| Digital Input High Level | | 2.0 | | | V |
| Digital Input Current | Digital Input = 0.0V | -70 | -4.0 | | μA |
| Output High Sat., $V_C - V_O$ | $I_O = -100mA$ | | 1.35 | 2.2 | V |
| | $I_O = -6A$ | | 3.2 | 4.5 | V |
| Output Low Sat., V_O | $I_O = 100mA$ | | 0.25 | 0.6 | V |
| | $I_O = 6A$ | | 3.4 | 4.5 | V |
| Thermal Shutdown | | | 165 | | $^{\circ}C$ |
| From Inv., Input to Output (Note 3, 4): | | | | | |
| Rise Time Delay | CL = 0 | | 35 | 70 | ns |
| | CL = 2.2nF | | 35 | 70 | ns |
| | CL = 30nF | | 35 | 70 | ns |
| 10% to 90% Rise | CL = 0 | | 20 | 40 | ns |
| | CL = 2.2nF | | 25 | 40 | ns |
| | CL = 30nF | | 85 | 150 | ns |
| Fall Time Delay | CL = 0 | | 35 | 70 | ns |
| | CL = 2.2nF | | 35 | 70 | ns |
| | CL = 30nF | | 35 | 80 | ns |
| 90% to 10% Fall | CL = 0 | | 15 | 40 | ns |
| | CL = 2.2nF | | 20 | 40 | ns |
| | CL = 30nF | | 85 | 150 | ns |
| From N.I. Input to Output (Note 3,4): | | | | | |
| Rise Time Delay | CL = 0 | | 35 | 70 | ns |
| | CL = 2.2nF | | 35 | 70 | ns |
| | CL = 30nF | | 35 | 70 | ns |
| 10% to 90% Rise | CL = 0 | | 20 | 40 | ns |
| | CL = 2.2nF | | 25 | 40 | ns |
| | CL = 30nF | | 85 | 150 | ns |
| Fall Time Delay | CL = 0 | | 35 | 70 | ns |
| | CL = 2.2nF | | 35 | 70 | ns |
| | CL = 30nF | | 35 | 80 | ns |
| 90% to 10% Fall | CL = 0 | | 15 | 40 | ns |
| | CL = 2.2nF | | 20 | 50 | ns |
| | CL = 30nF | | 85 | 150 | ns |
| Total Supply Current at 200kHz Input Switching Frequency | $T_A = 25^{\circ}C$ (Note 5) CL = 0 | | 30 | 40 | mA |

Note: 3. Delay measured from 50% input change to 10% output change.

Note: 4. Those parameters with CL = 30nF are not tested in production.

Note: 5. Inv. Input pulsed at 50% duty cycle with N.I. Input = 3V. or N.I. Input pulsed at 50% duty cycle with Inv. Input = 0V.

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