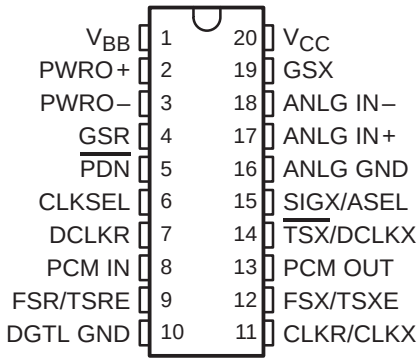
- **Combined ADC, DAC, and Filters**
- **Extended Variable Frequency Operation**
  - **Master Clock Up to 4.096 MHz**
  - **Sample Rates Up to 16 kHz**
  - **Passband Up to 6 kHz**
- **Reliable Silicon-Gate CMOS Technology**
- **Low Power Consumption**
  - **Operating Mode . . . 80 mW Typical**
  - **Power-Down Mode . . . 5 mW Typical**
- **Excellent Power-Supply Rejection Ratio Over Frequency Range of 0 to 50 kHz**
- **No External Components Needed for Sample, Hold, and Autozero Functions**
- **Precision Internal Voltage References**
- **μ-law and A-law Coding**

DW OR N PACKAGE
(TOP VIEW)



description

The TCM29C23 and TCM129C23 are single-chip PCM codecs (pulse-code-modulated encoders and decoders) and PCM lines filters. These devices provide all the functions required to interface a full-duplex (4-wire) voice telephone circuit with a TDM (time-division-multiplexed) system. Primary applications include digital encryption systems, digital voice-band data storage systems, digital signal processing, and mobile telephones.

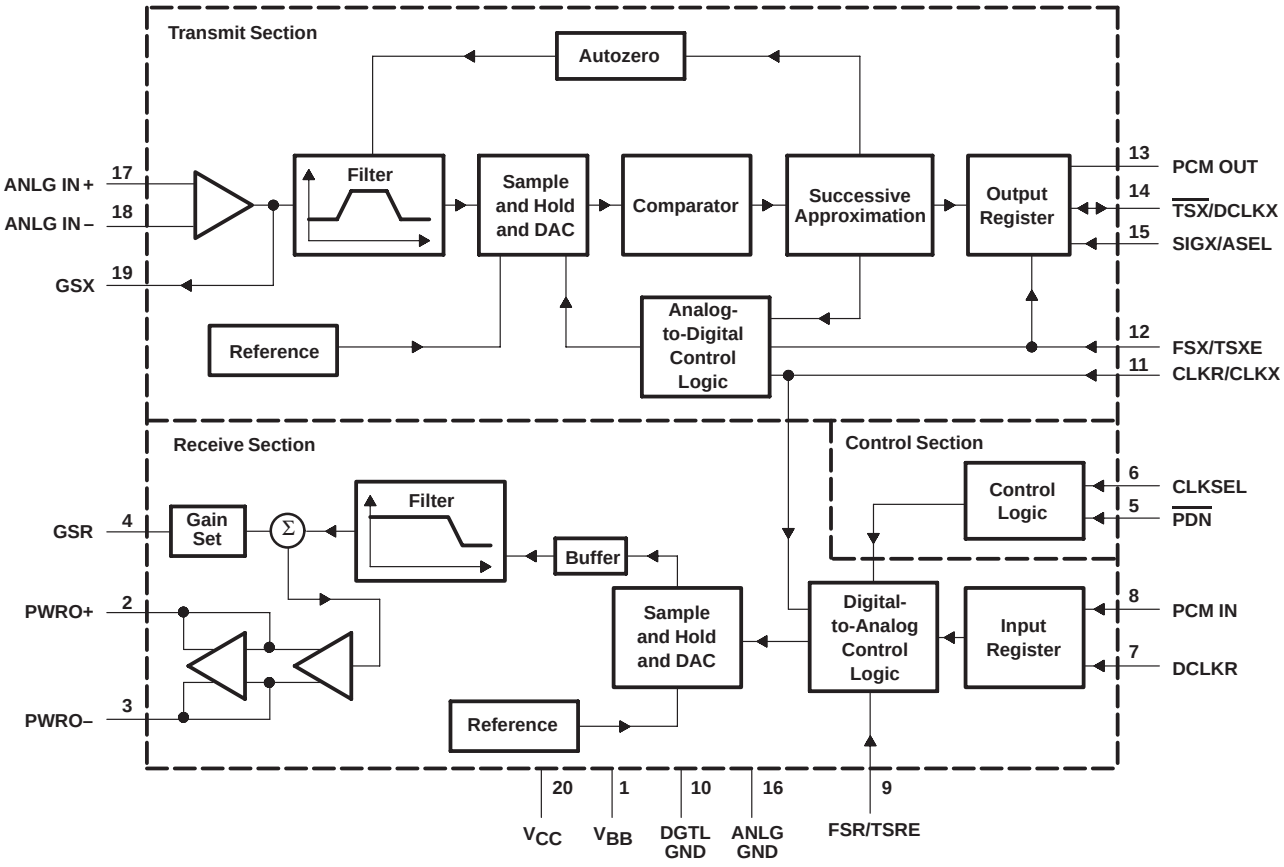
These devices are designed to perform the transmit encoding (A/D conversion) and receive decoding (D/A conversion) as well as the transmit and receive filtering functions in a pulse-code-modulated system. They are intended to be used at the analog termination of a PCM line or trunk.

The TCM29C23 and TCM129C23 provide the band-pass filtering of the analog signals prior to encoding and after decoding. These combination devices perform the encoding and decoding of voice and call progress tones as well as the signaling supervision information.

The TCM29C23 is characterized for operation from 0°C to 70°C. The TCM129C23 is characterized for operation from –40°C to 85°C.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ANLG GND	16		Analog ground return for all internal voice circuits. Not internally connected to DGTL GND.
ANLG IN+	17	I	Noninverting analog input to uncommitted transmit operational amplifier.
ANLG IN–	18	I	Inverting analog input to uncommitted transmit operational amplifier.
CLKR	11	I	Receive master clock and data clock for the fixed-data-rate mode. Receive master clock only for variable-data-rate mode. CLKR and CLKX are internally connected together.
CLKSEL	6	I	Clock frequency selection. Input must be connected to V_{BB}, V_{CC}, or ground to reflect the master clock frequency.
CLKX	11	I	Transmit master clock and data clock for the fixed-data-rate mode. Transmit master clock only for variable-data-rate mode. CLKR and CLKX are internally connected.
DCLKR	7	I	Selects fixed- or variable-data-rate operation. When connected to V_{BB}, the device operates in the fixed-data-rate mode. When DCLKR is not connected to V_{BB}, the device operates in the variable-data-rate mode and DCLKR becomes the receive data clock, which operates at frequencies from 64 kHz to 4.096 MHz.
DGTL GND	10		Digital ground for all internal logic circuits. Not internally connected to ANLG GND.
FSR/TSRE	9	I	Frame-synchronization clock input/time-slot enable for receive channel. In the fixed-data-rate mode, FSR distinguishes between signaling and nonsignaling frames by a double- or single-length pulse, respectively. In the variable-data-rate mode, this signal must remain high for the duration of the slot. The receive channel enters the standby state when FSR is TTL low for 300 ms.
FSX/TSXE	12	I	Frame-synchronization clock input/time-slot enable for the transmit channel. Operates independently of, but in an analogous manner to, FSR/TSRE. The transmit channel enters the standby state when FSX is low for 300 ms.
GSR	4	I	Input to the gain-setting network on the output power amplifier. Transmission level can be adjusted over a 12-dB range depending upon the voltage at GSR.
GSX	19	O	Output terminal of internal uncommitted operational amplifier. Internally, this is the voice signal input to the transmit filter.
PCM IN	8	I	Receive PCM input. PCM data is clocked in on this pin on eight consecutive negative transition of the receive data clock, which is CLKR in fixed-data-rate timing and DCLKR in variable-data-rate timing.
PCM OUT	13	O	Transmit PCM output. PCM data is clocked out of this output on eight consecutive positive transition of the transmit data clock, which is CLKX in fixed-data-rate timing and DCLKX in variable-data-rate timing.
$\overline{\text{PDN}}$	5	I	Power-down select. This device is inactive with a TTL low-level input to this terminal and active with a TTL high-level input to this terminal.
PWRO+	2	O	Noninverting output of power amplifier. Can drive transformer hybrids or high-impedance loads directly in either a differential or single-ended configuration.
PWRO–	3	O	Inverting output of power amplifier; functionally identical to but complementary to PWRO+.
SIGX/ASEL	15	I	A-law and μ-law operation select. When connected to V_{BB}, A-law is selected. When connected to V_{CC} or ground, μ-law is selected.
$\overline{\text{TSX}}$/DCLKX	12	I/O	Transmit channel time slot strobe (output) or data clock (input) for the transmit channel. In the fixed-data-rate mode, this is an open-drain output to be used as an enable signal for a 3-state output buffer. In the variable-data-rate mode, DCLKX becomes the transmit data clock, which operates at TTL levels from 64 kHz to 2.048 MHz.
V_{BB}	1		Most negative supply voltage; input is –5 V ±5%.
V_{CC}	16		Most positive supply voltage; input is 5 V ±5%.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.3 V to 15 V
Output voltage range, V_O . . . . . –0.3 V to 15 V
Input voltage range, V_I . . . . . –0.3 V to 15 V
Digital ground voltage range . . . . . –0.3 V to 15 V
Operating free-air temperature range, T_A: TCM29C23 . . . . . 0°C to70°C
TCM129C23 . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values for maximum ratings are with respect to V_{BB}.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 3)		4.75	5	5.25	V
V_{BB}	Supply voltage		–4.75	–5	–5.25	V
	DGTL GND voltage with respect to ANLG GND			0		V
V_{IH}	High-level input voltage, all inputs except CLKSEL		2.2			V
V_{IL}	Low-level input voltage, all inputs except CLKSEL				0.8	V
	CLKSEL input voltage	For 2.048 MHz	V_{BB}		V_{BB} +0.5	V
		For 1.544 MHz	0		0.5	
		For 1.536 Mhz	V_{CC} –0.5		V_{CC}	
R_L	Load resistance	At GSX	10			kΩ
		At PWRO+ and/or PWRO–	300			Ω
C_L	Load capacitance	At GSX			50	pF
		At PWRO+ and/or PWRO–			100	
T_A	Operating free-air temperature	TCM29C23	0		70	°C
		TCM129C23	–40		85	

NOTES: 2. To avoid possible damage to these CMOS devices and resulting reliability problems, the power-up procedure described in the device power-up sequence paragraphs later in this document should be followed.
3. Voltages at analog inputs and outputs, V_{CC} and V_{BB}, are with respect to ANLG GND. All other voltages are referenced to DGTL GND unless otherwise noted.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

supply current, f_{DCLK} = 4.096 MHz, outputs not loaded

PARAMETER			TEST CONDITIONS	TCM29C23			TCM129C23			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{CC}	Supply current from V_{CC}	Operating			7	9		8	13	mA
		Standby	FSX, or FSR at V_{IL} after 300 ms		0.5	1		0.7	1.5	
		Power down	$\overline{PDN}$ at V_{IL} after 10 µs		0.3	0.8		0.4	1	
I_{BB}	Supply current from V_{BB}	Operating			–7	–9		–8	–13	mA
		Standby	FSX or FSR at V_{IL} after 300 ms		–0.5	–1		–0.7	–1.5	
		Power down	$\overline{PDN}$ at V_{IL} after 10 µs		–0.3	–0.8		–0.4	–1	
P_D	Power dissipation	Operating			70	90		80	130	mW
		Standby	FSX or FSR at V_{IL} after 300 ms		5	10		7	15	
		Power down	$\overline{PDN}$ at V_{IL} after 10 µs		3	8		4	10	

† All typical values are at V_{BB} = –5 V, V_{CC} = 5 V, and T_A = 25°C.

digital interface

PARAMETER			TEST CONDITIONS	TMC29C23			TMC129C23			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	PCM OUT	I_{OH} = –9.6 mA	2.4			2.4			V
V_{OL}	Low-level output voltage at PCM OUT, TSX, SIG		I_{OL} = 3.2 mA			0.4			0.5	V
I_{IH}	High-level input current, any digital input		V_I = 2.2 V to V_{CC}			10			12	µA
I_{IL}	Low-level input current, any digital input		V_I = 0 to 0.8 V			10			12	µA
C_i	Input capacitance				5	10		5	10	pF
C_o	Output capacitance				5			5		pF

† All typical values are at V_{BB} = –5 V, V_{CC} = 5 V, and T_A = 25°C.

transmit amplifier input

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input current at ANLG IN+, ANLG IN–	V_I = –2.17 V to 2.17 V			±200	nA
Input offset voltage at ANLG IN +, ANLG IN–				±25	mV
Common-mode rejection at ANLG IN+, ANLG IN–		55			dB
Open-loop voltage amplification at GSX		5000			
Open-loop unity-gain bandwidth at GSX			1		MHz
Input resistance at ANLG IN+, ANLG IN–		10			MΩ

† All typical values are at V_{BB} = –5 V, V_{CC} = 5 V, and T_A = 25°C.

receive filter output

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output offset voltage at PWRO+, PWRO– (single ended)	Relative to ANLG GND		80		mV
Output resistance at PWRO+, PWRO–			1		Ω

† All typical values are at V_{BB} = –5 V, V_{CC} = 5 V, and T_A = 25°C.

gain and dynamic range, V_{CC} = 5 V, V_{BB} = –5 V, T_A = 25°C (unless otherwise noted) (see Notes 4, 5, and 6)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Encoder milliwatt response (transmit gain tolerance)		Signal input = 1.064 Vrms for μ-law		±0.5	±1	dBm0
		Signal input = 1.068 Vrms for A-law				
Encoder milliwatt response (nominal supplies and temperature)		T_A = 0°C to 70°C, Supply voltages = 5 V ±5%			± 0.15	dB
Digital milliwatt response (receive tolerance gain) relative to zero-transmission level point		Signal input per CCITT G.711, Output signal = 1 kHz		±0.5	±1	dBm0
Digital milliwatt response variation with temperature and supplies		T_A = 0°C to 70°C, Supply voltages = 5 V ±5%			± 0.15	dB
Zero-transmission-level point, transmit channel (0 dBm0)	μ-law	R_L = 600 Ω		2.76		dBm
	A-law			2.79		
	μ-law	R_L = 900 Ω		1		
	A-law			1.03		
Zero-transmission-level point, receive channel (0 dBm0)	μ-law	R_L = 600 Ω		5.76		dBm
	A-law			5.79		
	μ-law	R_L = 900 Ω		4		
	A-law			4.03		

NOTES: 4. Unless otherwise noted, the analog input is a 0-dBm0, 1020-Hz sine wave, where 0 dBm0 is defined as the zero-reference point of the channel under test. This corresponds to an analog signal input of 1.064 Vrms or an output of 1.503 Vrms.
5. The input amplifier is set for noninverting unity gain. The digital input is a PCM bit stream generated by passing a 0-dBm0, 1020-Hz sine wave through an ideal encoder.
6. Receive output is measured single ended in the maximum gain configuration. To set the output amplifier for maximum gain, GSR is connected to PWRO– and the output is taken at PWRO+. All output levels are (sin x)/x corrected.

gain tracking over recommended ranges of supply voltage and operating free-air temperature, reference level = –10 dBm0

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit gain-tracking error, sinusoidal input	3 ≥ input level ≥ –40 dBm0		±0.5	dB
	–40 > input level ≥ –50 dBm0		±1.5	
Receive gain-tracking error, sinusoidal input	3 ≥ input level ≥ –40 dBm0		±0.5	dB
	–40 > input level ≥ –50 dBm0		±1.5	

noise over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit noise, C-message weighted	ANLG IN+ = ANLG GND, ANLG IN– = GSX		18	dBrnC0
Transmit noise, psophometrically weighted	ANLG IN+ = ANLG GND, ANLG IN– = GSX		–72	dBm0p
Receive noise, C-message-weighted quiet code	PCM IN = 11111111 (μ-law), PCM IN = 10101010 (A-law), Measured at PWRO+		11	dBrnC0
Receive noise, psophometrically weighted	PCM = lowest positive decode level		–79	dBm0p

power-supply rejection and crosstalk attenuation over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{CC} supply-voltage rejection ratio, transmit channel	0 ≤ f < 30 kHz	Idle channel, Supply signal = 200 mV peak to peak, f measured at PCM OUT		–30		dB
	30 ≤ f < 50 kHz			–45		
V_{BB} supply-voltage rejection ratio, transmit channel	0 ≤ f < 30 kHz	Idle channel, Supply signal = 200 mV peak to peak, f measured at PCM OUT		–30		dB
	30 ≤ f < 50 kHz			–55		
V_{CC} supply-voltage rejection ratio, receive channel (single ended)	0 ≤ f < 30 kHz	Idle channel, Supply signal = 200 mV peak to peak, f measured at PWRO+		–20		dB
	30 ≤ f < 50 kHz			–45		
V_{BB} supply-voltage rejection ratio, receive channel (single ended)	0 ≤ f < 30 kHz	Idle channel, Supply signal = 200 mV peak to peak, Narrow-band, f measured at PWRO+		–20		dB
	30 ≤ f < 50 kHz			–45		
Crosstalk attenuation, transmit to receive (single ended)		ANLG IN+ = 0 dBm0, f = 1.02 kHz, Unity gain, PCM IN = lowest decode level, Measured at PWRO+	68			dB
Crosstalk attenuation, receive to transmit (single ended)		PCM IN = 0 dBm0, f = 1.02 kHz, Measured at PCM OUT	68			dB

† All typical values are at V_{BB} = –5 V, V_{CC} = 5 V, and T_A = 25°C.

distortion over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit signal-to-distortion ratio, sinusoidal input (CCITT G.712 – Method 2)	0 ≥ ANLG IN+ ≥ –30 dBm0	33			dB
	–30 > ANLG IN+ ≥ –40 dBm0	28			
	–40 > ANLG IN+ ≥ –45 dBm0	23			
Receive signal-to-distortion ratio, sinusoidal input (CCITT G.712 – Method 2)	0 ≥ ANLG IN+ ≥ –30 dBm0	33			dB
	–30 > ANLG IN+ ≥ –40 dBm0	28			
	–40 > ANLG IN+ ≥ –45 dBm0	23			
Transmit single-frequency distortion products	AT&T Advisory #64 (3.8), Input signal = 0 dBm0			–40	dBm0
Receive single-frequency distortion products	AT&T Advisory #64 (3.8), Input signal = 0 dBm0			–46	dBm0

† All typical values are at V_{BB} = –5 V, V_{CC} = 5 V, and T_A = 25°C.

transmit filter transfer over recommended ranges of supply voltage and operating free-air temperature, f_{DCLK} = 4.096 MHz, FSX/FSR = 16 kHz (see Figure 1)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1.02 kHz	Input amplifier set for unity gain, Noninverting maximum gain output, Input signal at ANLG IN+ is 0 dBm0	50 Hz	–10	0	dB
		200 Hz	–1	0.5	
		300 Hz to 6 kHz	–0.5	0.5	
		6.5 kHz	–4	0.3	
		6.8 kHz	–6	0	
		8 kHz		–12	
		9 kHz and above		–30	

receive filter transfer over recommended ranges of supply voltage and operating free-air temperature (see Figure 2)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1.02 kHz	Input signal at PCM IN is 0 dBm0	Below 200 Hz	–2	0.5	dB
		200 Hz	–1	0.5	
		300 Hz to 6 kHz	–0.5	0.5	
		6.6 kHz	–4	0.3	
		6.8 kHz	–6	0	
		8 kHz		–12	
		9.2 kHz and above		–30	

timing requirements

clock timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figure 3)

		MIN	TYP†	MAX	UNIT
$t_{c(CLK)}$	Clock period, for CLKX, CLKR (2.048-MHz systems)	244			ns
t_r, t_f	Rise and fall times for CLKX and CLKR	5		20	ns
$t_{w(CLK)}$	Pulse duration for CLKX and CLKR (see Note 7)	110			ns
$t_{w(DCLK)}$	Pulse duration, DCLK (f_{DCLK} = 64 kHz to 2.048 MHz) (see Note 7)	110			ns
	Clock duty cycle, $[t_{w(CLK)}/t_{c(CLK)}]$ for CLKX and CLKR	45%	50%	55%	

† All typical values are at V_{BB} = –5 V, V_{CC} = 5 V, and T_A = 25°C.
NOTE 7: FSX CLK must be phase locked with CLKX. FSR CLK must be phase locked with CLKR.

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 3)

PARAMETER		MIN	MAX	UNIT
$t_{d(FSX)}$	Frame-sync delay time	60	$t_{c(CLK)}$ – 60	ns

receive timing requirements over recommended ranges of supply voltages and operating free-air temperature, fixed-data-rate mode (see Figure 4)

PARAMETER		MIN	MAX	UNIT
$t_{d(FSR)}$	Frame-sync delay time	60	$t_{c(CLK)}$–60	ns

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see Figure 5)

PARAMETER		MIN	MAX	UNIT
$t_{d(TSDX)}$	Time-slot delay time from DCLKX	60	$t_{d(DCLKX)}$–60	ns
$t_{d(FSX)}$	Frame-sync delay time	60	$t_{c(CLK)}$–60	ns
$t_{c(DCLKX)}$	Clock period for DCLKX	244	15620	ns

receive timing requirements over recommended ranges of supply voltages and operating free-air temperature, variable-data-rate mode (see Figure 6)

PARAMETER		MIN	MAX	UNIT
$t_{d(TSDR)}$	Time-slot delay time from DCLKR	60	$t_{d(DCLKR)}-140$	ns
$t_{d(FSR)}$	Frame-sync delay time	60	$t_{c(CLK)}-60$	ns
$t_{su(PCM\ IN)}$	Setup time before bit 7 falling edge	10		ns
$t_{h(PCM\ IN)}$	Hold time after bit 8 falling edge	60		ns
$t_{c(DCLKR)}$	Data clock frequency	244	15620	ns
t_{SER}	Time-slot end receive time	0		ns

switching characteristics

propagation delay times over recommended ranges of operating conditions, fixed-data-rate mode (see Figure 3)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd1}	From rising edge of transmit clock to bit 1 data valid at PCM OUT (data enable time on time-slot entry) (see Note 8)	C_L = 0 to 100 pF	0	90	ns
t_{pd2}	From rising edge of transmit clock bit n to bit data valid at PCM OUT (data valid time)	C_L = 0 to 100 pF	0	90	ns
t_{pd3}	From falling edge of transmit clock bit 8 to bit 8 Hi-Z at PCM OUT (data float time on time-slot exit) (see Note 8)	C_L = 0	60	215	ns
t_{pd4}	From rising edge of transmit clock bit 1 to TSX active (low) (time slot enable time)	C_L = 0 to 100 pF	0	90	ns
t_{pd5}	From falling edge of transmit clock bit 8 to TSX inactive (high) (time-slot disable time) (see Note 8)	C_L = 0	60	190	ns

NOTE 8: Timing parameters t_{pd1}, t_{pd3}, and t_{pd5} are referenced to the high-impedance state.

propagation delay times over recommended ranges of operating conditions, variable-data-rate mode (see Note 9 and Figure 5)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd7}	Data delay time from DCLKX	C_L = 0 to 100 pF	0	90	ns
t_{pd8}	Data delay from time-slot enable to PCM OUT		0	50	ns
t_{pd9}	Data delay from time-slot disable to PCM OUT		0	80	ns
t_{pd10}	Data delay time from FSX	$t_{d(TSDX)}$ = 80 ns	0	90	ns

NOTE 9: Timing parameters t_{pd8} and t_{pd9} are referenced to the high-impedance state.

PARAMETER MEASUREMENT INFORMATION

CLK, CLKR, and CLKX selection requirements for DSP-based applications

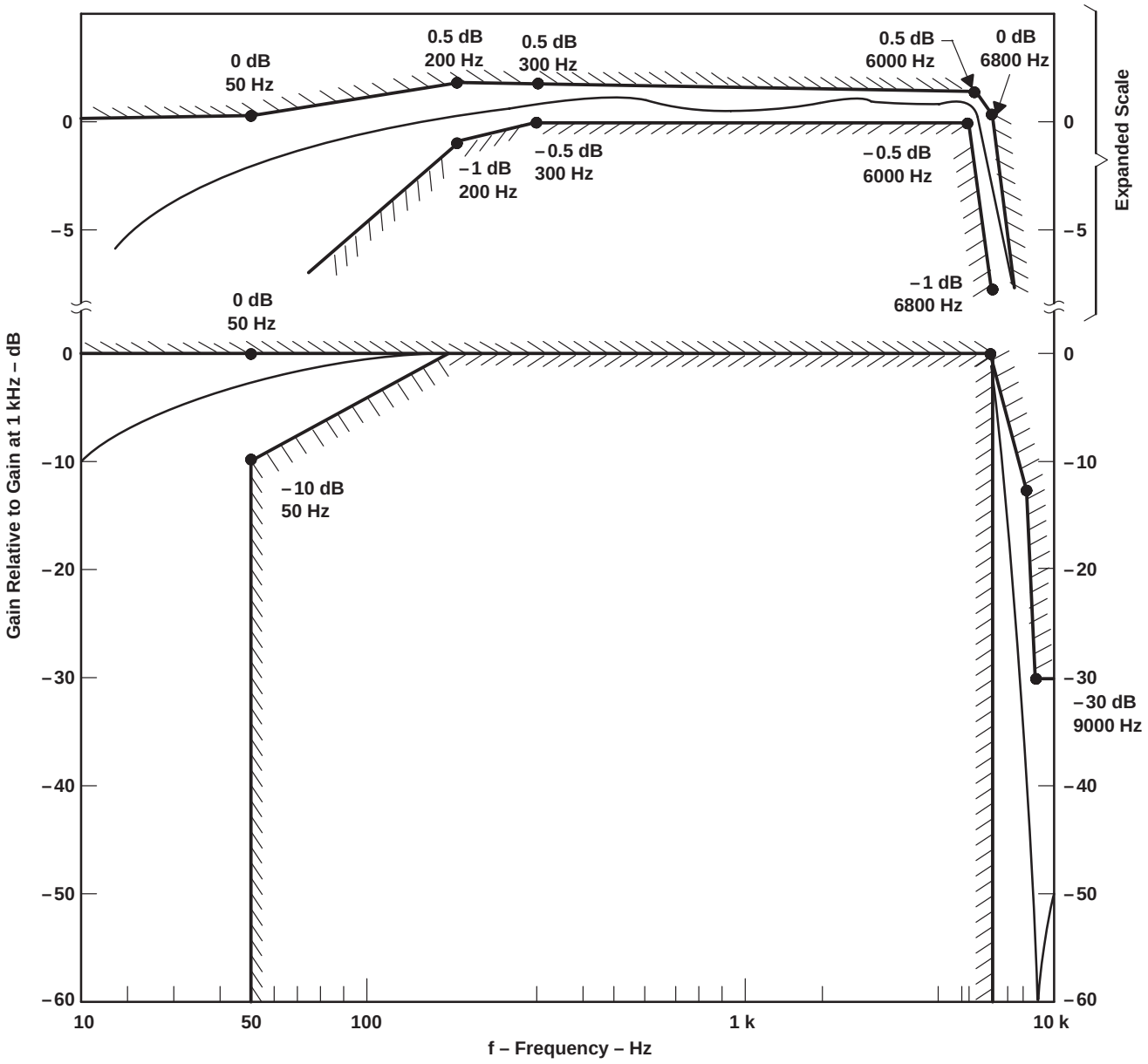
CLK, CLKR, and CLKX must be selected as follows:

CLKSEL PIN	CLK, CLKR, CLKX (BETWEEN 1 MHz to 3 MHz)
–5 V	= (256) × (frame-sync frequency)
0 V	= (193) × (frame-sync frequency)
5 V	= (192) × (frame-sync frequency)

e.g., for frame-sync frequency = 16 kHz

CLKSEL PIN	CLK, CLKR, CLKX (BETWEEN 1 MHz to 3 MHz)
–5 V	= 4.096 MHz
0 V	= 3.088 MHz
5 V	= 3.072 MHz

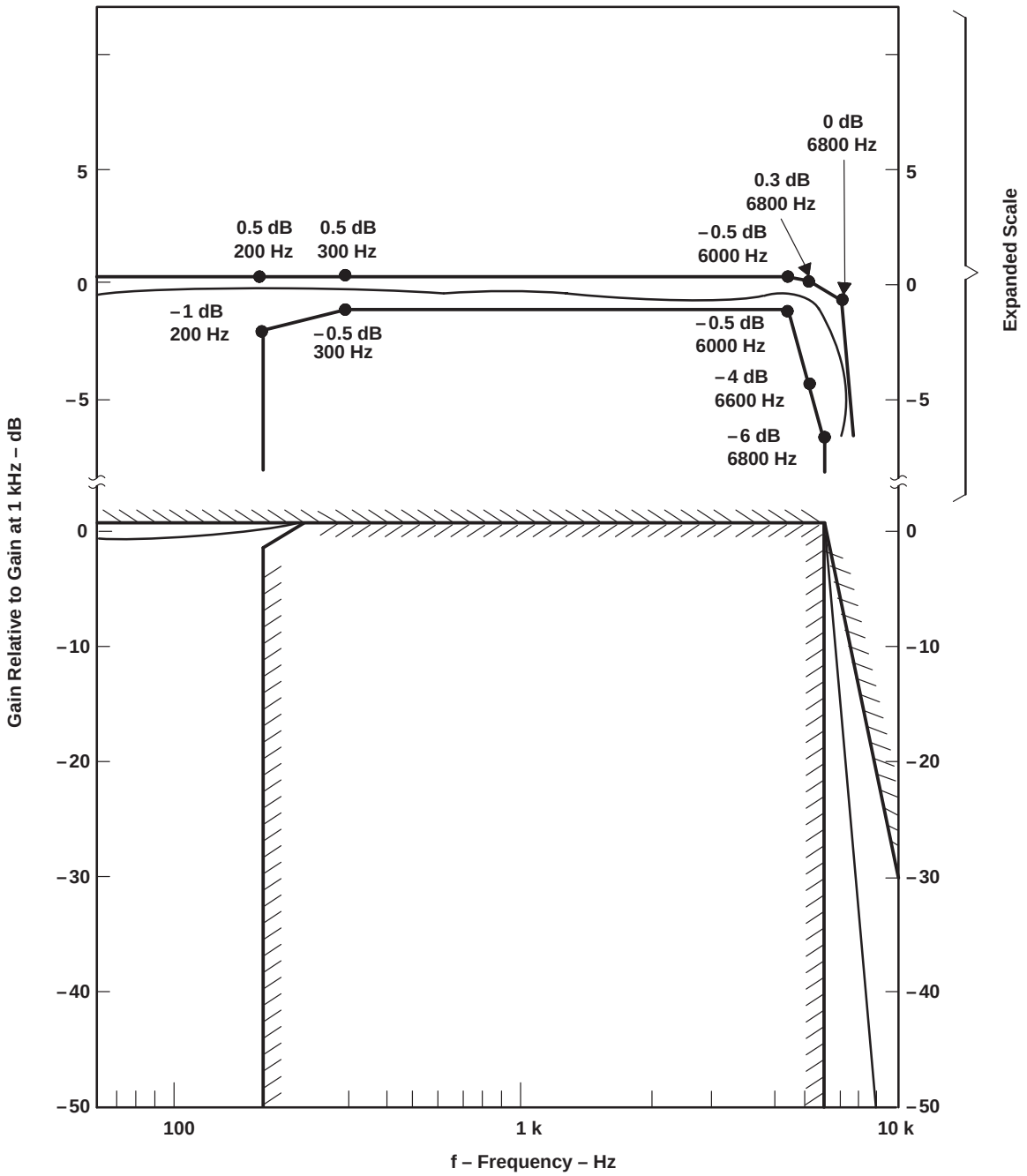
PARAMETER MEASUREMENT INFORMATION



NOTE A: CLKR/CLKX = 4.096 MHz

Figure 1. Transfer Characteristics of the Transmit Filter

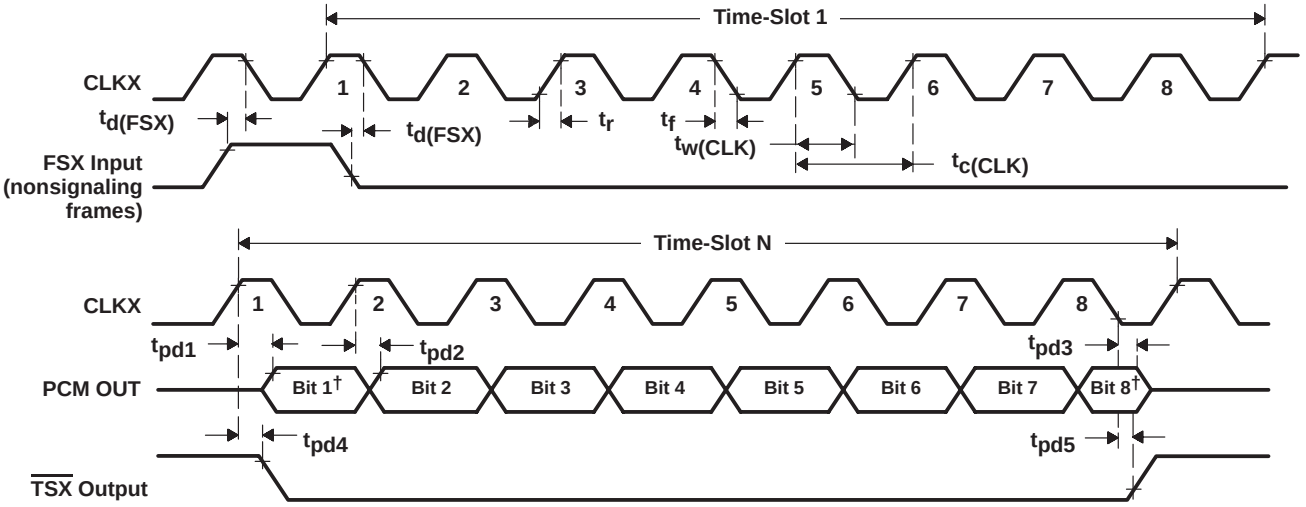
PARAMETER MEASUREMENT INFORMATION



NOTE A: CLKR/CLKX = 4.096 MHz

Figure 2. Transfer Characteristics of the Receive Filter

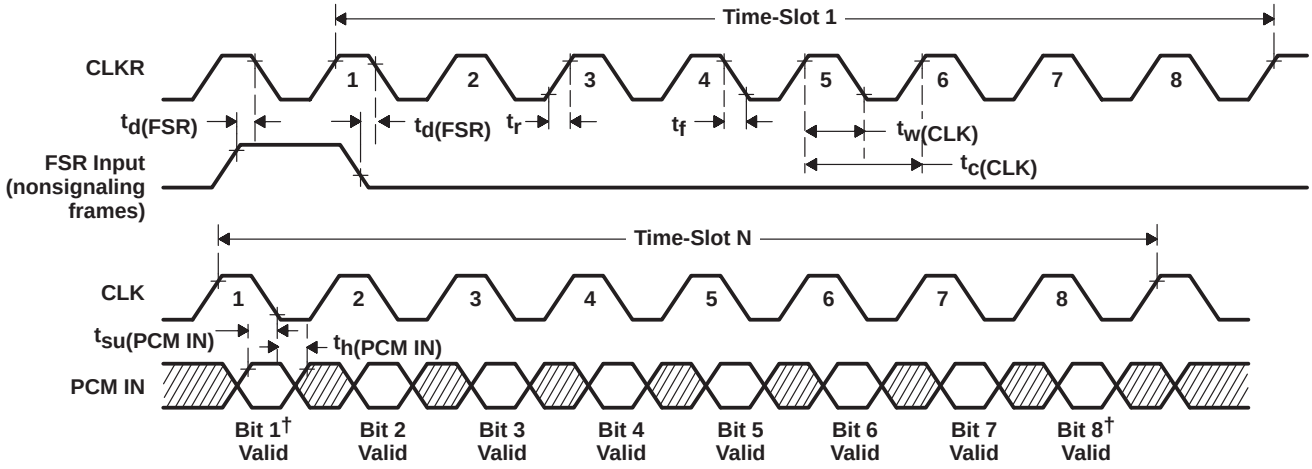
PARAMETER MEASUREMENT INFORMATION



† Bit 1 = MSB = sign bit and locked in first on PCM IN or clocked out first on PCM OUT. Bit 8 = LSB = least significant bit and is clocked in last on PCM IN or is clocked out last on PCM OUT.

NOTE A: Inputs are driven from 0.45 V to 2.4 V. Time intervals are referenced to 2 V if the high level is indicated and 0.8 V if the low level is indicated.

Figure 3. Transmit Timing (Fixed-Data Rate)

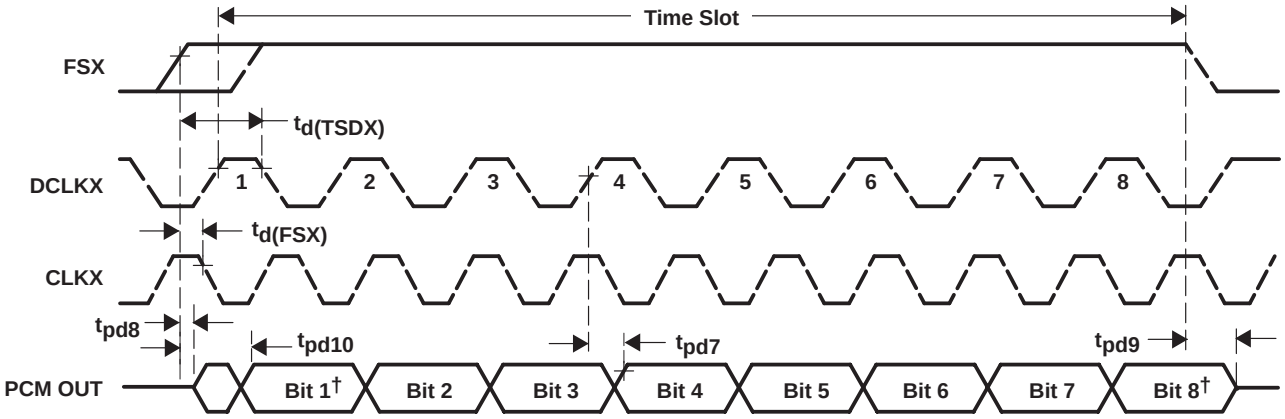


† Bit 1 = MSB = sign bit and locked in first on PCM IN or clocked out first on PCM OUT. Bit 8 = LSB = least significant bit and is clocked in last on PCM IN or is clocked out last on PCM OUT.

NOTE A: Inputs are driven from 0.45 V to 2.4 V. Time intervals are referenced to 2 V if the high level is indicated and 0.8 V if the low level is indicated.

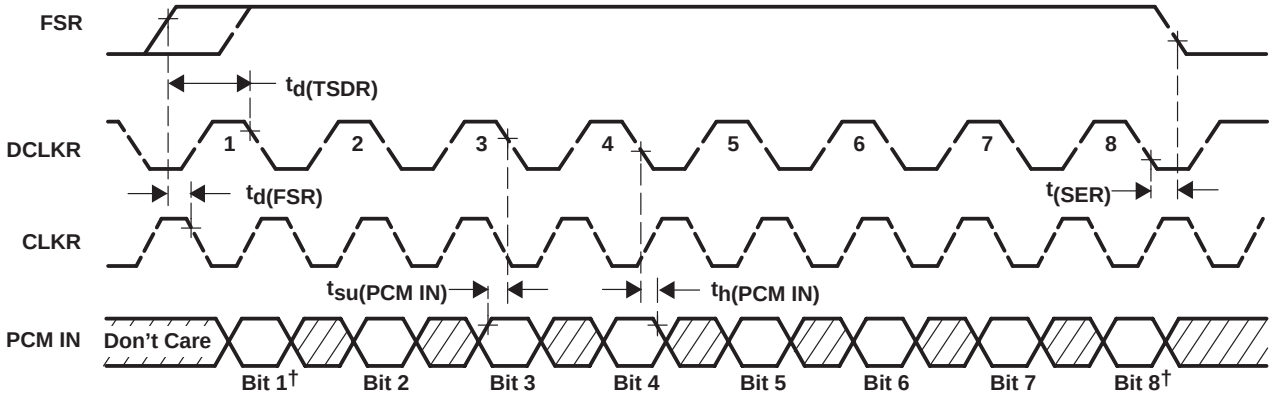
Figure 4. Receive Timing (Fixed-Data Rate)

PARAMETER MEASUREMENT INFORMATION



† Bit 1 = MSB = sign bit and locked in first on the PCM IN or clocked out first on PCM OUT. Bit 8 = LSB = least significant bit and is clocked in last on PCM IN or is clocked out last on PCM OUT.
NOTE A: IAll timing parameters referenced to V_{IH} and V_{IL} except t_{pd7} and t_{pd8}, which reference the high-impedance state.

Figure 5. Transmit Timing (Variable-Data-Rate)



† Bit 1 = MSB = sign bit and locked in first on the PCM IN or clocked out first on PCM OUT. Bit 8 = LSB = least significant bit and is clocked in last on PCM IN or is clocked out last on PCM OUT.
NOTE A: All timing parameters referenced to V_{IH} and V_{IL} except t_{pd7} and t_{pd8}, which reference the high-impedance state.

Figure 6. Receive Timing (Variable-Data-Rate)

PRINCIPLES OF OPERATION

system reliability and design considerations

TCM29C23, TCM129C23 system reliability and design considerations are described in the following paragraphs.

latch-up

Latch-up is possible in all CMOS devices. It is caused by the firing of a parasitic SCR that is present due to the inherent nature of CMOS. When a latch-up occurs, the device draws excessive amounts of current and will continue to draw heavy current until power is removed. Latch-up can result in permanent damage to the device if supply current to the device is not limited.

Even though the TCM29C23 and TCM129C23 are heavily protected against latch-up, it is still possible to cause latch-up under certain conditions in which excess current is forced into or out of one or more terminals. Latch-up can occur when the positive supply voltage drops momentarily below ground, when the negative supply voltage rises momentarily above ground, or possibly if a signal is applied to a terminal after power has been applied but before the ground is connected. This can happen if the device is hot-inserted into a card with the power applied, or if the device is mounted on a card that has an edge connector and the card is hot-inserted into a system with the power on.

To help ensure that latch-up does not occur, it is considered good design practice to connect a reverse-biased Schottky diode (with a forward voltage drop of less than or equal to 0.4 V – 1N5711 or equivalent) between the power supply and GND (see Figure 7). If it is possible that a TCM29C23- or TCM129C23-equipped card that has an edge connector could be hot-inserted into a powered-up system, it is also important to ensure that the ground edge connector traces are longer than the power and signal traces so that the card ground is always the first to make contact.

device power-up sequence

Latch-up can also occur if a signal source is connected without the device being properly grounded. A signal applied to one terminal could then find a ground through another signal terminal on the device. To ensure proper operation of the device and as a safeguard against this sort of latch-up, it is recommended that the following power-up sequence always be used:

1. Ensure that no signals are applied to the device before the power-up sequence is complete.
2. Connect GND.
3. Apply V_{BB} (most negative voltage).
4. Apply V_{CC} (most positive voltage).
5. Force a power down condition in the device.
6. Connect clocks.
7. Release the power down condition.
8. Apply FS synchronization pulses.
9. Apply the signal inputs.

When powering down the device, this procedure should be followed in the reverse order.

PRINCIPLES OF OPERATION

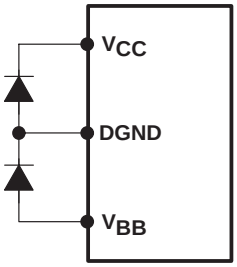


Figure 7. Latch-Up Protection Diode Connection

internal sequencing

On the transmit channel, digital outputs PCM OUT and $\overline{TSX}$ are held in the high-impedance state for approximately four frames (500 μs) after power up or application of V_{BB} or V_{CC}. After this delay, PCM OUT, $\overline{TSX}$, and signaling are functional and occur in the proper time slot. The analog circuits on the transmit side require approximately 60 ms to reach their equilibrium value due to the autozero circuit settling time. Thus valid digital information, such as on/off hook detection, is available almost immediately while analog information is available after some delay. To further enhance system reliability, PCM OUT and $\overline{TSX}$ are placed in the high-impedance state approximately 20 μs after an interruption of CLKX.

power-down and standby operations

To minimize power consumption, a power-down mode and three standby modes are provided.

For power down, an external low signal is applied to $\overline{PDN}$. In the absence of a signal, PDN is interally pulled up to a high logic level and the device remains active. In the power-down mode, the average power consumption is reduced to 5 mW.

Three standby modes give the user the options of placing the entire device on standby, placing only the transmit channel on standby, or placing only the receive channel on standby. to place the entire device on standby, both FSX and FSR are held low. For transmit-only operation (receive channel on standby), FSX is high and FSR is held low. For receive-only operation (transmit section on standby), FSR is high and FSX is held low. When the entire device is in standby mode, power consumption is reduced to an average of 3 mW. See Table 1 for power-down and standby procedures.

Table 1. Power-Down and Standby Procedures

DEVICE STATUS	PROCEDURE	TYPICAL POWER CONSUMPTION	DIGITAL OUTPUT STATUS
Power down	$\overline{PDN}$ low	3 mW	$\overline{TSX}$ and PCM OUT are in the high-impedance state; SIGR goes to low within 10 μs.
Entire device on standby	FSX and FSR are low	3 mW	$\overline{TSX}$ and PCM OUT are in the high-impedance state; SIGR goes to low within 300 ms.
Only transmit on standby	FSX is low, FSR is high	40 mW	$\overline{TSX}$ and PCM OUT are placed in the high-impedance state within 300 ms.
Only receive on standby	FSR is low, FSX is high	30 mW	SIGR is placed in the high-impedance state within 300 ms.

PRINCIPLES OF OPERATION

fixed-data-rate timing

Fixed-data-rate timing is selected by connecting DCLKR to V_{BB}. It uses master clocks CLKX and CLKR, frame-synchronizer clocks FSX and FSR, and output $\overline{TSX}$. FSX and FSR are inputs that set the sampling frequency. Data is transmitted on PCM OUT on the first eight positive transitions of CLKX following the rising edge of FSX. Data is received on PCM IN on the first eight falling edges of CLKR following FSX. A digital-to-analog (D/A) conversion is performed on the received digital word and the resulting analog sample is held on an internal sample-and-hold capacitor until transferred to the receive filter.

variable-data-rate timing

Variable-data-rate timing is selected by connecting DCLKR to the bit clock for the receive PCM highway rather than to V_{BB}. It uses master clocks CLKX and CLKR, bit clocks DCLKX and DCLKR, and frame-synchronization clocks FSX and FSR.

Variable-data-rate timing allows for a flexible data frequency. The frequency of the bit clocks can be varied from 64 kHz to 4.096 MHz. The bit clocks must be asynchronous.

When the FSX/TSXE input is high, PCM data is transmitted from PCM OUT onto the highway on the next eight consecutive positive transitions of DCLKX. Similarly, while the FSR/TSRE input is high, the PCM word is received from the highway by PCM IN on the next eight consecutive negative transitions of DCLKR.

The transmitted PCM word will be repeated in all remaining time slots in the frame as long as DCLKX is pulsed and FSX is held high. This feature, which allows the PCM word to be transmitted to the PCM highway more than once per frame if desired, is available only with variable-data-rate timing. Signaling is allowed only in the fixed-data-rate mode because the variable-data-rate mode provides no means with which to specify a signaling frame.

asynchronous operation

In order to avoid crosstalk problems associated with special interrupt circuits, the design includes separate digital-to-analog converters and voltage references on the transmit and receive sides to allow completely independent operation of the two channels. In either timing mode, the master clock, data clock, and time-slot strobe must be synchronized at the beginning of each frame. Specifically, in the variable-rate mode, the falling edge of CLKX must occur within $t_{d(FSX)}$ ns after the rise of FSX and the falling edge of DCLKX must occur within t_{TSDX} ns after the rise of FSX. CLKX and DCLKX are synchronized once per frame but may be of different frequencies. The receive channel operates in a similar manner and is completely independent of the transmit timing (see Figure 6). This approach requires the provision of two separate master clocks but avoids the use of a synchronizer, which can cause intermittent data conversion errors.

precision voltage references

Voltage references that determine the gain and dynamic range characteristics of the device are generated internally. No external components are required to provide the voltage references. A difference in subsurface charge density between two suitably implanted MOS devices is used to derive a temperature- and bias-stable reference voltage, which are calibrated during the manufacturing process. Separate references are supplied to the transmit and receive sections, and each is calibrated independently. Each reference value is then further trimmed in the gain-setting operational amplifiers to a final precision value. Manufacturing tolerances of typically ±0.04 dB in absolute gain can be achieved for each half channel, providing the user a significant margin to compensate for error in other system components.

PRINCIPLES OF OPERATION

conversion laws

The TCM29C23 and TCM129C23 provide pin-selectable A-law or μ-law operation as specified by the CCITT G.711 recommendation. A-law operation is selected when ASEL is connected to V_{BB}. Signaling is not allowed during A-law operation. μ-law operation is selected by connecting ASEL to V_{CC} or GND.

transmit operation

transmit filter

The input section provides gain adjustment in the pass band by means of an on-chip uncommitted operational amplifier. The load impedance to ground (ANLG GND) at the amplifier output (GSX) must be greater than 10 kΩ in parallel with less than 50 pF. The input signal on ANLG IN+ can be either ac or dc coupled. The input operational amplifier can also be used in the inverting mode or differential amplifier mode.

A low-pass antialiasing section is included on the device. This section provides 35-dB attenuation at the sampling frequency. No external components are required to provide the necessary antialiasing function for the switched-capacitor section of the transmit filter.

encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample-and-hold capacitor. The encoder performs an analog-to-digital conversion on a switched-capacitor array. Digital data representing the sample is transmitted on the first eight data clock bits of the next frame.

The autozero circuit corrects for dc offset on the input signal to the encoder using the sign bit averaging technique. The sign bit from the encoder output is long-term averaged and subtracted from the input to the encoder. All dc offset is removed from the encoder input waveform.

receive operation

decoding

The serial PCM word is received at PCM IN on the first eight data clock bits of the frame. Digital-to-analog conversion is performed, and the corresponding analog sample is held on an internal sample-and-hold capacitor. This sample is transferred to the receive filter.

receive filter

The receive section of the filter provides pass-band flatness and stop-band rejection that fulfills both the AT&T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin x)/x response of such decoders.

receive output power amplifiers

A balanced output amplifier is provided to allow maximum flexibility in output configuration. Either of the two outputs can be used single ended (i.e., referenced to ANLG GND) to drive single-ended loads. Alternatively, the differential output directly drives a bridged load. The output stage is capable of driving loads as low as 300 Ω single ended to a level of 12 dBm or 600 Ω differentially to a level of 15 dBm.

The receive channel transmission level may be adjusted between specified limits by manipulating of the GSR input. GSR is internally connected to an analog gain-setting network. When GSR is connected to PWRO+, the level is minimum. The output transmission level between 0 and –12 dB as GSR is adjusted (with an adjustable resistor) between PWRO+ and PWRO–.

Transmission levels are specified relative to the receive channel output under digital milliwatt conditions (i.e., when the digital input at PCM IN is the eight-code sequence specified in CCITT recommendation G.711).

APPLICATION INFORMATION

output gain-set design considerations (see Figure 7)

PWRO+ and PWRO– are low-impedance complementary outputs. The voltages at the nodes are:

V_{O+} at PWRO+
V_{O-} at PWRO–
$V_O = V_{O+} - V_{O-}$ (total differential response)

R1 and R2 are a gain-setting resistor network with the center tap to the GSR input.

A value greater than 10 kΩ and less than 100 kΩ for R1 + R2 is recommended because of the following:

The parallel combination of R1 + R2 and R_L sets the total loading.
The total capacitance at the GSR input and the parallel combination of R1 and R2 define a time constant that has to be minimized to avoid inaccuracies.

V_{AD} represents the maximum available digital milliwatt output response (V_A = 3.06 V rms).

$$V_{OD} = A \bullet V_{AD}$$

$$\text{where } A = \frac{1 + (R1/R2)}{4 + (R1/R2)}$$

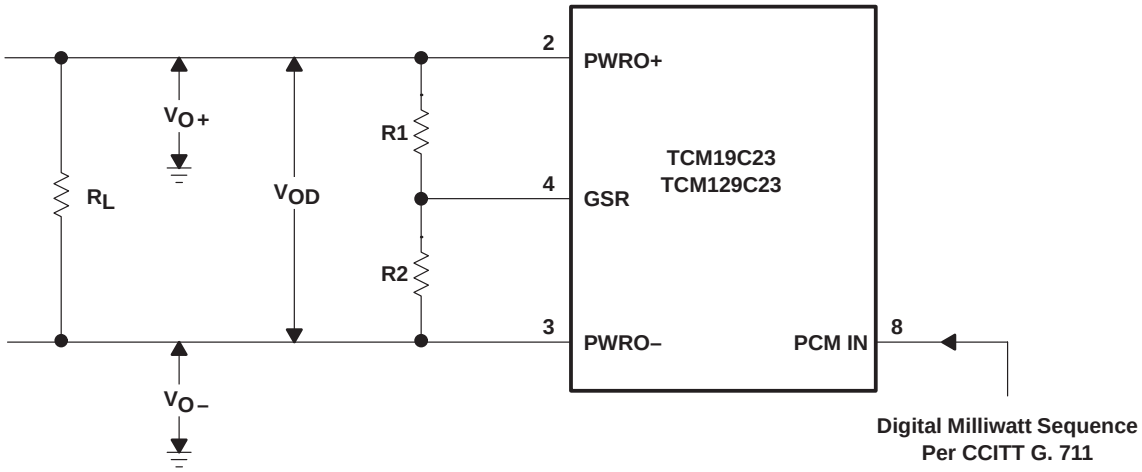


Figure 8. Gain-Setting Configuration

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TCM129C23DW - http://www.ti.com/product/tcm129c23dw?HQS=TI-null-null-dscatalog-df-pf-null-wwe

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