

MP7510DI, MP7511DI, MP7512DI**CMOS QUAD SPST ANALOG SWITCHES (MP7510DI, MP7511DI)****CMOS DUAL SPDT ANALOG SWITCH (MP7512DI)****FEATURES**

- Latch-Proof
- Overvoltage Protected
- Low R_{ON} : 75 Ω
- Low Dissipation: 3 mW
- TTL/CMOS Direct Interface
- Silicon-Nitride Passivated
- Monolithic Dielectrically-Isolated CMOS

GENERAL DESCRIPTION

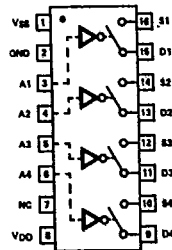
The MP7510DI, MP7511DI and MP7512DI are a family of latch proof dielectrically isolated CMOS switches featuring overvoltage protection up to $\pm 25V$ above the power supplies. These benefits are obtained without sacrificing the low "ON" resistance (75 Ω) or low leakage current (400pA), the main features of an analog switch.

The MP7510DI and MP7511DI consist of four independent SPST analog switches packaged in a 16-pin DIP. They differ only in that the digital control logic is inverted. The MP7512DI has two independent SPDT switches packaged in a 14-pin DIP.

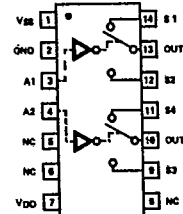
Very low power dissipation, overvoltage protection and TTL/CMOS direct interfacing are achieved by combining a unique circuit design and a dielectrically isolated CMOS process. Silicon nitride passivation ensures long term stability while monolithic construction provides reliability.

PIN CONFIGURATIONS

(TOP VIEW)



MP7510DI
MP7511DI



MP7512DI

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CONTROL LOGIC

MP7510DI: Switch "ON" for Address "HIGH"

MP7511DI: Switch "ON" for Address "LOW"

MP7512DI: Address "HIGH" makes S1 to Out-1 and S3 to Out-2

See Section 7 for Ordering Information

MP7510DI, MP7511DI, MP7512DISPECIFICATIONS ($V_{DD} = +15V$, $V_{SS} = -15V$ unless otherwise noted)

COMMERCIAL VERSIONS (J, K)

PARAMETER ⁴	MODEL	VERSION	25°C	0°C to 70°C (N) -25°C to +85°C (D)		UNITS	TEST CONDITIONS
				MIN	MAX		
ANALOG SWITCH							
R_{ON} ¹	All	J, K	100 max		175	Ω	$-10V \leq V_D \leq +10V$ $I_{DS} = 1.0 \text{ mA}$
R_{ON} vs V_D (V_S)	All	J, K	20 typ			%	
R_{ON} Drift	All	J, K	+0.5 typ			%/°C	
R_{ON} Match	All	J, K	1 typ			%	$V_D = 0, I_{DS} = 1.0 \text{ mA}$
R_{ON} Drift Match	All	J, K	0.01 typ			%/°C	
I_D (I _S)OFF ¹	All	J, K	5 max		500	nA	$V_D = -10V, V_S = +10V$ and $V_D = +10V, V_S = -10V$
I_D (I _S)ON ²	All	J, K	10 max			nA	$V_S = V_D = +10V$ $V_S = V_D = -10V$
I_{OUT} ¹	MP7512DI	J, K	15 max		1500	nA	$V_{S1} = V_{OUT} = \pm 10V, V_{S2} = \mp 10V$ and $V_{S2} = V_{OUT} = \pm 10V, V_{S1} = \mp 10V$
DIGITAL CONTROL							
V_{INL} ¹	All	J, K			0.8	V	
V_{INH} ¹	All	K		2.4		V	
C_{IN}	All	J, K	3 typ			pF	
I_{INH} ¹	All	J, K	10 max			nA	$V_{IN} = V_{DD}$
I_{INL} ¹	All	J, K	10 max			nA	$V_{IN} = 0$
DYNAMIC CHARACTERISTICS							
t_{ON}	MP7510DI MP7511DI	J, K J, K	180 typ 350 typ			ns	$V_{IN} = 0$ to +3.0V
t_{OFF}	MP7510DI MP7511DI	J, K J, K	350 typ 180 typ			ns	
$t_{TRANSITION}$	MP7512DI	J, K	300 typ			ns	
C_S (C _D)OFF	All	J, K	8 typ			pF	
C_S (C _D)ON	All	J, K	17 typ			pF	
C_{DS} (C _S -OUT)	All	J, K	1 typ			pF	V_D (V_S) = 0V
C_{DD} (C _{SS})	All	J, K	0.5 typ			pF	
C_{OUT}	MP7512DI	J, K	17 typ			pF	
Q_{INJ}	All	J, K	30 typ			pC	Measured at S or D terminal. $C_L = 1000 \text{ pF}, V_{IN} = 0$ to 3V, V_D (V_S) = +10V to -10V
POWER SUPPLY							
I_{DD} ¹	All	J, K	800 max		800	μA	All digital inputs = V_{INH}
I_{SS} ¹	All	J, K	800 max		800	μA	
I_{DD} ¹	All	J, K	500 max		500	μA	All digital inputs = V_{INL}
I_{SS} ¹	All	J, K	500 max		500	μA	

Notes

- ¹ 100% tested.
- ² Guaranteed, not production tested.
- ³ A pullup resistor, typically 1-2 k Ω is required to make "J" versions TTL compatible.
- ⁴ Specifications subject to change without notice.

CAUTION: The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high electrostatic fields. Keep unused units in conductive foam at all times. Prior to pulling the devices from the conductive foam, ground the foam to deplete any accumulated charge.

MP7510DI, MP7511DI, MP7512DI

SPECIFICATIONS ($V_{DD} = +15V$, $V_{SS} = -15V$ unless otherwise noted)

MILITARY VERSIONS (S, T)

PARAMETER ⁴	MODEL	VERSION	25°C MAX	-55°C to +125°C		UNITS	TEST CONDITIONS
				MIN	MAX		
ANALOG SWITCH R_{ON}^1	All	S, T	100		175	Ω	$-10V \leq V_D \leq +10V$ $I_{DS} = 1 \text{ mA}$
$I_D (I_S)_{OFF}^1$	All	S, T	3		200	nA	$V_D = -10V, V_S = +10V$ and $V_D = +10V, V_S = -10V$
$I_D (I_S)_{ON}^2$	All	S, T	10		600	nA	$V_S = V_D = +10V$ and $V_S = V_D = -10V$
I_{OUT}^1	MP7512DI	S, T	9		600	nA	$V_{S1} = V_{OUT} = \pm 10V$ $V_{S2} = \mp 10V$ and $V_{S2} = V_{OUT} = \pm 10V$ $V_{S1} = \mp 10V$
DIGITAL CONTROL V_{INL}^1	All	S, T			0.8	V	
$V_{INH}^{1,3}$	MP7510DI	S		2.4		V	
	MP7511DI	T		2.4		V	
	MP7512DI						
	MP7511DI MP7512DI	S		3.0		V	
I_{INH}^1	All	S, T	10			nA	$V_{IN} = V_{DD}$
I_{INL}^1	All	S, T	10			nA	$V_{IN} = 0$
DYNAMIC CHARACTERISTICS							
t_{ON}^2	MP7510DI MP7511DI	S, T	1.0			μs	$V_{IN} = 0 \text{ to } +3V$
t_{OFF}^2	MP7510DI MP7511DI	S, T	1.0			μs	
$t_{TRANSITION}^2$	MP7512DI	S, T	1.0			μs	
POWER SUPPLY							
I_{DD}^1	All	S, T			800	μA	All digital inputs = V_{INH}
I_{SS}^1	All	S, T			800	μA	
I_{DD}^1	All	S, T			500	μA	All digital inputs = V_{INL}
I_{SS}^1	All	S, T			500	μA	

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ABSOLUTE MAXIMUM RATINGS

V_{DD} to Gnd. +17V
 V_{SS} to Gnd -17V
 Overvoltage at $V_D (V_S)$
 (1 second surge) $V_{DD}+25V$
 or $V_{SS}-25V$
 (Continuous) $V_{DD}+20V$
 or $V_{SS}-20V$
 Switch Current (I_{DS} , Continuous) 50 mA
 Switch Current (I_{DS} , Surge)
 1 ms Duration, 10% Duty Cycle 150 mA

Digital Input Voltage Range 0V to V_{DD}
 Power Dissipation (Package)
 Up to +75°C 450 mW
 Derates above +75°C by 6 mW/°C
 Storage Temperature -65°C to +150°C
 Operating Temperature
 Plastic (J, K Versions) 0°C to +70°C
 Ceramic (J, K Versions) -25°C to +85°C
 Ceramic (S, T Versions) -55°C to +125°C

Notes

- 1 100% tested.
- 2 Guaranteed, not production tested.
- 3 A pullup resistor, typically 1-2 k Ω is required to make the MP7511DISD and MP7512DISD TTL compatible.
- 4 Specifications subject to change without notice.