HDL Synthesis Design with LeonardoSpectrum: CPLD Flow

This tutorial shows you how to use LeonardoSpectrum from within ispLEVER® to synthesize a Verilog design and generate an EDIF file for a Lattice CPLD device.

***Note**: If you want to learn how to use LeonardoSpectrum in standalone mode or understand more about its advanced features, please see the third-party manuals online by choosing **Help > ispLEVER Documentation Library** from the ispLEVER Project Navigator.*

Learning Objectives

When you have completed this tutorial, you should be able to do the following:

- Create a new EDIF project in the ispLEVER system and target a device.
- Start LeonardoSpectrum from within the Project Navigator, synthesize your Verilog design, and generate an EDIF netlist file.
- Import the EDIF file into the ispLEVER system, fit the design, generate a JEDEC file, and view the Fitter report.
- Perform static timing analysis using the Performance Analyst and view the results.

Time to Complete This Tutorial

The time to complete this tutorial is about 20 minutes.

System Requirements

One of the following software configurations is required to complete the tutorial:

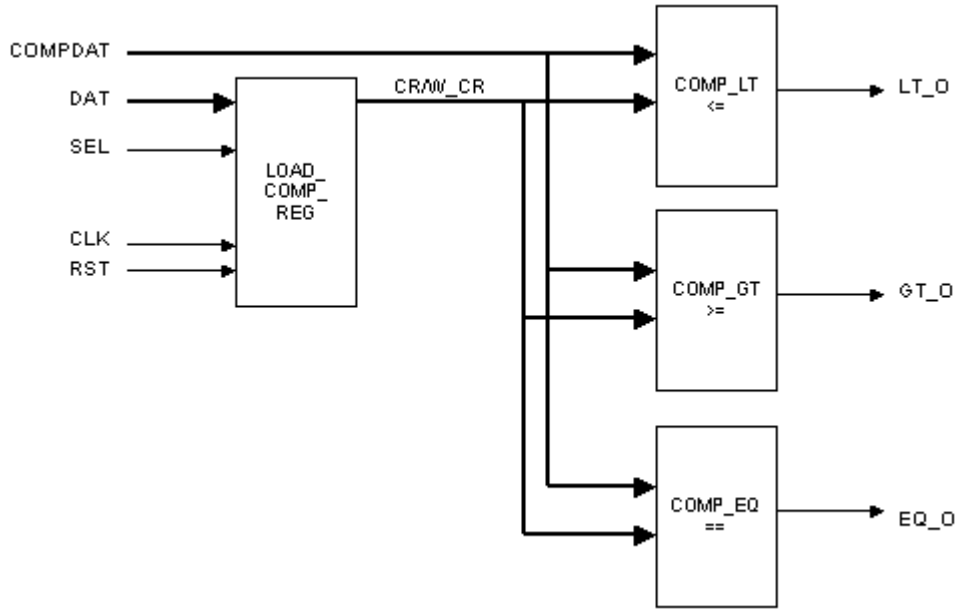
- IspLEVER Starter
- ispLEVER Base
- ispLEVER Advanced
- ispLEVER Advanced System with active Mentor Graphics LeonardoSpectrum license

Accessing Online Help

You can find online help information on any tool included in the tutorial at any time by pressing the F1 key.

About the Tutorial Design

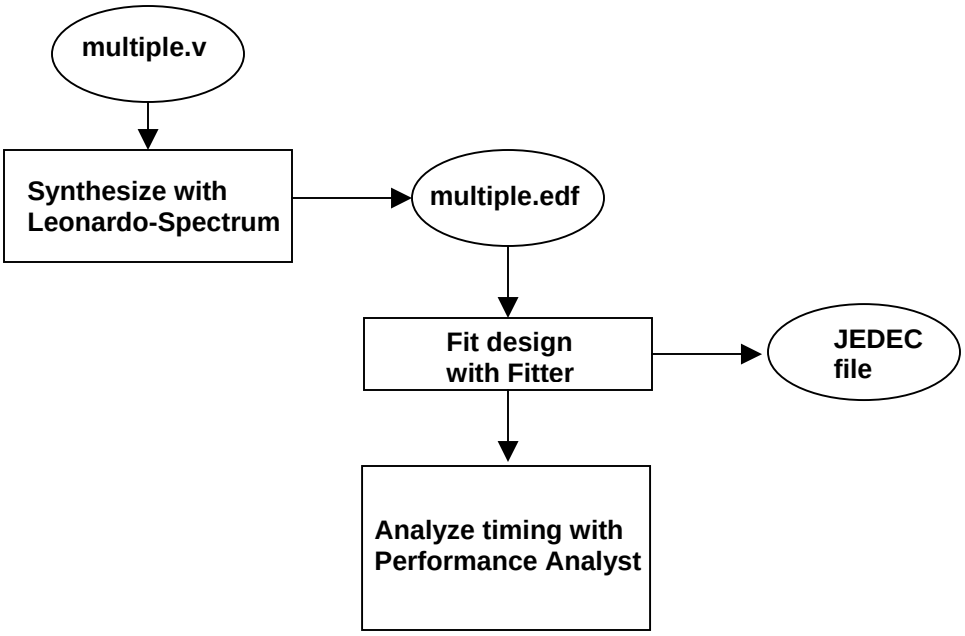
The tutorial design consists of a simple set of equal-to, greater-than, and less-than data comparators, as shown in the following figure:



This tutorial first directs you to create an EDIF project in the Project Navigator, then select the target device in which the design will be implemented. The tutorial assumes that functional simulation has already been performed. Next, you start LeonardoSpectrum and open a new LeonardoSpectrum project. After you import the VHDL source files and set the implementation options, the tool synthesizes the design into the target device and generates an EDIF netlist.You then import the EDIF netlist into the Project Navigator project and perform mapping, placing, and routing. Finally, you perform a static timing analysis and examine the results.

About the Tutorial Data Flow

The following figure illustrates the design flow that the tutorial takes.You may find it helpful to refer to this diagram as you move through the tutorial tasks.


multiple.v
Synthesize with Leonardo-Spectrum
multiple.edf
Fit design with Fitter
JEDEC file
Analyze timing with Performance Analyst