

# MB81C4256-70/-80/-10/-12

## CMOS 1,048,576 BIT FAST PAGE MODE DYNAMIC RAM

### CMOS 256 x 4 Bits Fast Page Mode DRAM

The Fujitsu MB81C4256 is a CMOS, fully decoded dynamic RAM organized as 262,144 words x 4 bits. The MB81C4256 has been designed for mainframe memories, buffer memories, and video image memories requiring high speed and high bandwidth output with low power dissipation.

Fujitsu's advanced three-dimensional stacked capacitor cell technology gives the MB81C4256 high  $\alpha$ -ray soft error immunity. CMOS technology is used in the peripheral circuits to provide low power dissipation and high speed operation.

This specification applies to the BC die revision that was developed to realize faster access time. Faster speed versions (70 and 80 ns) are available on this chip.

### Features

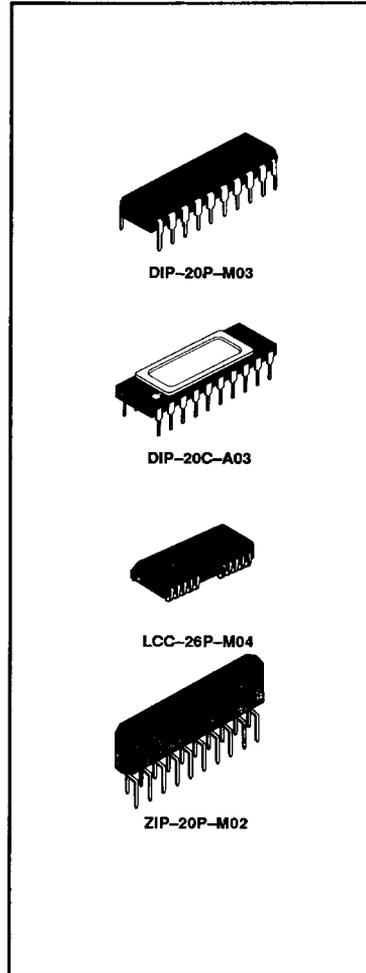
Parameter	MB81C4256 -70	MB81C4256 -80	MB81C4256 -10	MB81C4256 -12
RAS Access Time	70 ns max.	80 ns max.	100 ns max.	120 ns max.
Random Cycle Time	140 ns min.	155 ns min.	180 ns min.	210 ns min.
Address Access Time	43 ns max.	45 ns max.	50 ns max.	60 ns max.
CAS Access Time	25 ns max.	25 ns max.	25 ns max.	35 ns max.
Fast Page Mode Cycle Time	53 ns min.	55 ns min.	60 ns min.	70 ns min.
Low Power Dissipation • Operating Current	413 mW max.	385 mW max.	330 mW max.	275 mW max.
• Standby Current	11 mW max. (TTL level)/5.5 mW max. (CMOS level)			

- 262,144 words x 4 bits organization
- Silicon gate, CMOS, 3D-Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 8.2 ms
- Early write or OE controlled write capability
- RAS only, CAS-before-RAS, or Hidden Refresh
- Fast Page Mode, Read-Modify-Write capability
- On-chip substrate bias generator for high performance

### Absolute Maximum Ratings (See Note)

Parameter	Symbol	Value	Unit
Voltage at any pin relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-1 to +7	V
Voltage of $V_{CC}$ supply relative to $V_{SS}$	$V_{CC}$	-1 to +7	V
Power Dissipation	PD	1.0	W
Short Circuit Output Current	—	50	mA
Storage Temperature	Ceramic	-55 to +150	°C
	Plastic		

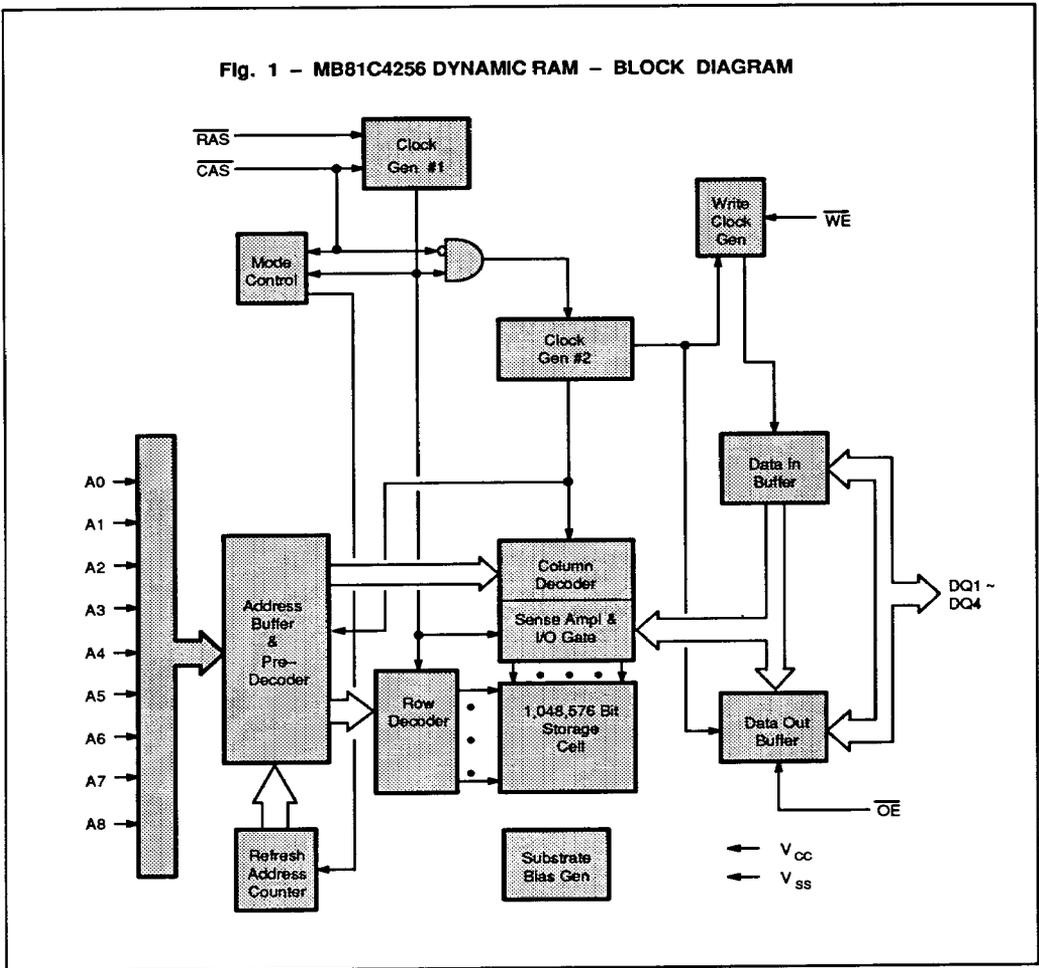
**Note:** Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this impedance circuit.

MB81C4256-70  
 MB81C4256-80  
 MB81C4256-10  
 MB81C4256-12

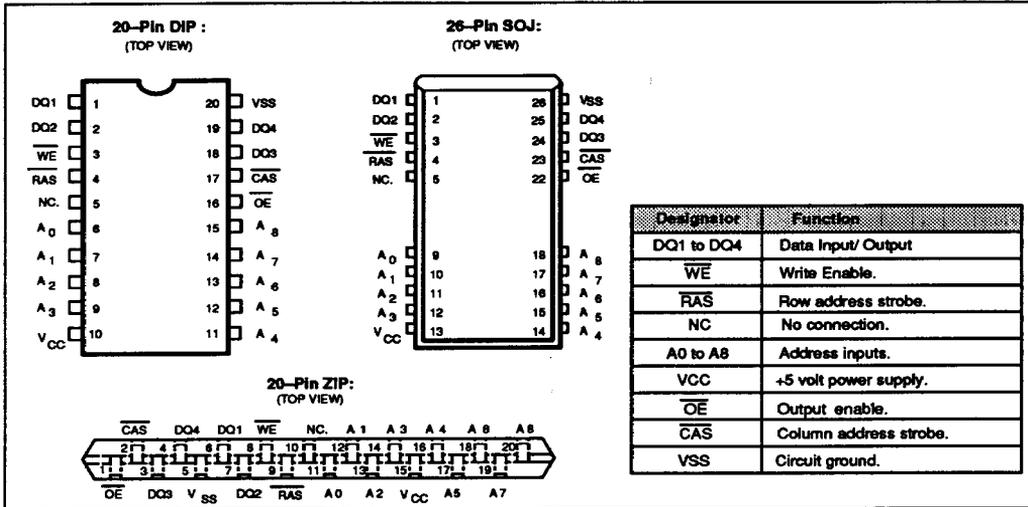
2



**CAPACITANCE ( $T_A = 25^\circ\text{C}$ ,  $f = 1\text{MHz}$ )**

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A8	$C_{IN1}$	—	5	pF
Input Capacitance, $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$	$C_{IN2}$	—	5	pF
Input/Output Capacitance, DQ1 to DQ4	$C_{DO}$	—	6	pF

## PIN ASSIGNMENTS AND DESCRIPTIONS



2

## RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V <sub>CC</sub>	4.5	5.0	5.5	V	0 °C to +70 °C
		V <sub>SS</sub>	0	0	0		
Input High Voltage, all inputs	1	V <sub>IH</sub>	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	V <sub>IL</sub>	-2.0	—	0.8	V	
Input Low Voltage, DQ(*)	1	V <sub>ILD</sub>	-1.0	—	0.8	V	

\* : Undershoots of up to -2.0 volts with a pulse width not exceeding 20ns are acceptable.

## FUNCTIONAL OPERATION

### ADDRESS INPUTS

Eighteen input bits are required to decode any four of 1,048,576 cell addresses in the memory matrix. Since only nine address bits are available, the column and row inputs are separately strobed by  $\overline{\text{CAS}}$  and  $\overline{\text{RAS}}$  as shown in Figure 1. First, nine row address bits are input on pins A0 through A8 and latched with the row address strobe ( $\overline{\text{RAS}}$ ) then, nine column address bits are input and latched with the column address strobe ( $\overline{\text{CAS}}$ ). Both row and column addresses must be stable on or before the falling edge of  $\overline{\text{CAS}}$  and  $\overline{\text{RAS}}$ , respectively. The address latches are of the flow-through type; thus, address information appearing after  $t_{\text{RAH}}(\text{min}) + t_1$  is automatically treated as the column address.

### WRITE ENABLE

The read or write mode is determined by the logic state of  $\overline{\text{WE}}$ . When  $\overline{\text{WE}}$  is active Low, a write cycle is initiated; when  $\overline{\text{WE}}$  is High, a read cycle is selected. During the read mode, input data is ignored.

### DATA INPUT

Input data is written into memory in either of three basic ways—an early write cycle, an  $\overline{\text{OE}}$  (delayed) write cycle, and a read-modify-write cycle. The falling edge of  $\overline{\text{WE}}$  or  $\overline{\text{CAS}}$ , whichever is later, serves as the input data-latch strobe. In an early write cycle, the input data (DQ1–DQ4) is strobed by  $\overline{\text{CAS}}$  and the setup/hold times are referenced to  $\overline{\text{CAS}}$  because  $\overline{\text{WE}}$  goes Low before  $\overline{\text{CAS}}$ . In a delayed write or a read-modify-write cycle,  $\overline{\text{WE}}$  goes Low after  $\overline{\text{CAS}}$ ; thus, input data is strobed by  $\overline{\text{WE}}$  and all setup/hold times are referenced to the write-enable signal.

### DATA OUTPUT

The three-state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high-impedance state until the column address strobe goes Low. When a read or read-modify-write cycle is executed, valid outputs are obtained under the following conditions:

- t<sub>TRAC</sub> : from the falling edge of  $\overline{\text{RAS}}$  when t<sub>ACD</sub> (max) is satisfied.
- t<sub>TCAC</sub> : from the falling edge of  $\overline{\text{CAS}}$  when t<sub>ACD</sub> is greater than t<sub>ACD</sub>, t<sub>RAD</sub> (max).
- t<sub>TAA</sub> : from column address input when t<sub>AD</sub> is greater than t<sub>RAD</sub> (max).
- t<sub>TOEA</sub> : from the falling edge of  $\overline{\text{OE}}$  when  $\overline{\text{OE}}$  is brought Low after t<sub>TRAC</sub>, t<sub>TCAC</sub>, or t<sub>TAA</sub>.

The data remains valid until either  $\overline{\text{CAS}}$  or  $\overline{\text{OE}}$  returns to a High logic level. When an early write is executed, the output buffers remain in a high-impedance state during the entire cycle.

## DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Notes 3

Parameter	Notes	Symbol	Conditions	Values			Unit
				Min	Typ	Max	
Output high voltage		$V_{OH}$	$I_{OH} = -5 \text{ mA}$	2.4	—	—	V
Output low voltage		$V_{OL}$	$I_{OL} = 4.2 \text{ mA}$	—	—	0.4	
Input leakage current (any input)		$I_{I(L)}$	$0V \leq V_{IN} \leq 5.5V$ ; $4.5V \leq V_{CC} \leq 5.5V$ ; $V_{SS} = 0V$ ; All other pins under test = $0V$	-10	—	10	$\mu\text{A}$
Output leakage current		$I_{OL(O)}$	$0V \leq V_{OUT} \leq 5.5V$ ; Data out disabled	-10	—	10	
Operating current (Average Power supply Current) <span style="border: 1px solid black; padding: 2px;">2</span>	MB81C4256-70	$I_{CC1}$	$\overline{RAS}$ & $\overline{CAS}$ cycling; $t_{rc} = \text{min}$	—	—	75	mA
	MB81C4256-80					70	
	MB81C4256-10					60	
	MB81C4256-12					50	
Standby current (Power supply current)	TTL level	$I_{CC2}$	$\overline{RAS} = \overline{CAS} = V_{IH}$	—	—	2.0	mA
	CMOS level		$\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2V$			1.0	
Refresh current #1 (Average power sup- ply current) <span style="border: 1px solid black; padding: 2px;">2</span>	MB81C4256-70	$I_{CC3}$	$\overline{CAS} = V_{IH}$ , $\overline{RAS}$ cycling; $t_{rc} = \text{min}$	—	—	70	mA
	MB81C4256-80					65	
	MB81C4256-10					55	
	MB81C4256-12					45	
Fast Page Mode current <span style="border: 1px solid black; padding: 2px;">2</span>	MB81C4256-70	$I_{CC4}$	$\overline{RAS} = V_{IL}$ , $\overline{CAS}$ cycling; $t_{rc} = \text{min}$	—	—	47	mA
	MB81C4256-80					45	
	MB81C4256-10					40	
	MB81C4256-12					33	
Refresh current #2 (Average power sup- ply current) <span style="border: 1px solid black; padding: 2px;">2</span>	MB81C4256-70	$I_{CC5}$	$\overline{RAS}$ cycling; $\overline{CAS}$ -before- $\overline{RAS}$ ; $t_{rc} = \text{min}$	—	—	70	mA
	MB81C4256-80					65	
	MB81C4256-10					55	
	MB81C4256-12					45	

2

MB81C4256-70  
 MB81C4256-80  
 MB81C4256-10  
 MB81C4256-12

## AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C4256-70		MB81C4256-80		MB81C4256-10		MB81C4256-12		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		$t_{REF}$	—	8.2	—	8.2	—	8.2	—	8.2	ms
2	Random Read/Write Cycle Time		$t_{RC}$	140	—	155	—	180	—	210	—	ns
3	Read-Modify-Write Cycle Time		$t_{RWC}$	197	—	212	—	240	—	275	—	ns
4	Access Time from RAS	6,9	$t_{RAC}$	—	70	—	80	—	100	—	120	ns
5	Access Time from CAS	7,9	$t_{CAC}$	—	25	—	25	—	25	—	35	ns
6	Column Address Access Time	8,9	$t_{AA}$	—	43	—	45	—	50	—	60	ns
7	Output Hold Time		$t_{OH}$	7	—	7	—	7	—	7	—	ns
8	Output Buffer Turn On Delay Time		$t_{ON}$	5	—	5	—	5	—	5	—	ns
9	Output Buffer Turn off Delay Time	10	$t_{OFF}$	—	25	—	25	—	25	—	25	ns
10	Transition Time		$t_T$	3	50	3	50	3	50	3	50	ns
11	RAS Precharge Time		$t_{RP}$	60	—	65	—	70	—	80	—	ns
12	RAS Pulse Width		$t_{RAS}$	70	100000	80	100000	100	100000	120	100000	ns
13	RAS Hold Time		$t_{RSH}$	25	—	25	—	25	—	35	—	ns
14	CAS to RAS Precharge Time		$t_{CRP}$	0	—	0	—	0	—	0	—	ns
15	RAS to CAS Delay Time	11,12	$t_{RCD}$	20	45	22	55	25	75	25	85	ns
16	CAS Pulse Width		$t_{CAS}$	25	—	25	—	25	—	35	—	ns
17	CAS Hold Time		$t_{CSH}$	70	—	80	—	100	—	120	—	ns
18	CAS Precharge Time (C-B-R cycle)	19	$t_{CPN}$	10	—	10	—	10	—	15	—	ns
19	Row Address Set Up Time		$t_{ASR}$	0	—	0	—	0	—	0	—	ns
20	Row Address Hold Time		$t_{RAH}$	10	—	12	—	15	—	15	—	ns
21	Column Address Set Up Time		$t_{ASC}$	0	—	0	—	0	—	0	—	ns
22	Column Address Hold Time		$t_{CAH}$	15	—	15	—	15	—	20	—	ns
23	RAS to Column Address Delay Time	13	$t_{RAD}$	15	27	17	35	20	50	20	60	ns
24	Column Address to RAS Lead Time		$t_{RAL}$	43	—	45	—	50	—	60	—	ns
25	Read Command Set Up Time		$t_{RCS}$	0	—	0	—	0	—	0	—	ns
26	Read Command Hold Time Referenced to RAS	14	$t_{RRH}$	0	—	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to CAS	14	$t_{RCH}$	0	—	0	—	0	—	0	—	ns
28	Write Command Set Up Time	15	$t_{WCS}$	0	—	0	—	0	—	0	—	ns
29	Write Command Hold Time		$t_{WCH}$	15	—	15	—	15	—	20	—	ns
30	WE Pulse Width		$t_{WP}$	15	—	15	—	15	—	20	—	ns
31	Write Command to RAS Lead Time		$t_{RWL}$	22	—	22	—	25	—	30	—	ns
32	Write Command to CAS Lead Time		$t_{CWL}$	17	—	17	—	20	—	25	—	ns
33	DIN set Up Time		$t_{DS}$	0	—	0	—	0	—	0	—	ns
34	DIN Hold Time		$t_{DH}$	15	—	15	—	15	—	20	—	ns

## AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

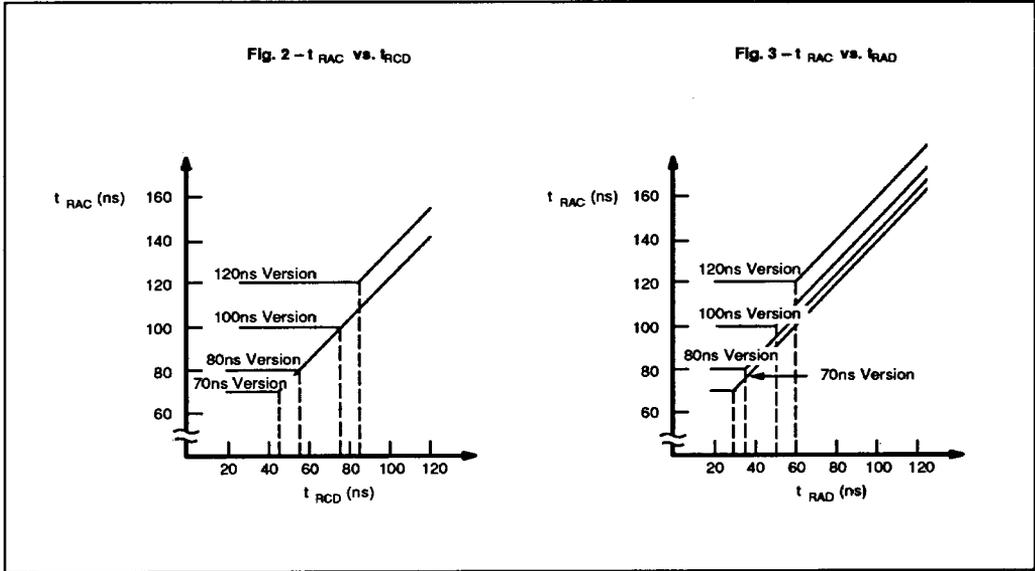
No.	Parameter	Notes	Symbol	MB81C4256-70		MB81C4256-80		MB81C4256-10		MB81C4256-12		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
35	RAS Precharge time to CAS Active Time (Refresh cycles)		t <sub>RPC</sub>	0	—	0	—	0	—	0	—	ns
36	CAS Set Up Time for CAS-before-RAS Refresh		t <sub>CSR</sub>	0	—	0	—	0	—	0	—	ns
37	CAS Hold Time for CAS-before-RAS Refresh		t <sub>CHR</sub>	15	—	15	—	15	—	20	—	ns
38	Access Time from OE	9	t <sub>OEA</sub>	—	22	—	22	—	22	—	30	ns
39	Output Buffer Turn Off Delay from OE	10	t <sub>OEZ</sub>	—	25	—	25	—	25	—	25	ns
40	OE to RAS Lead Time for Valid Data		t <sub>OEL</sub>	10	—	10	—	10	—	10	—	ns
41	OE Hold Time Referenced to WE	16	t <sub>OEH</sub>	0	—	0	—	0	—	0	—	ns
42	OE to Data In Delay Time		t <sub>OED</sub>	25	—	25	—	25	—	25	—	ns
43	DIN to CAS Delay Time	17	t <sub>DZC</sub>	0	—	0	—	0	—	0	—	ns
44	DIN to OE Delay Time	17	t <sub>DZO</sub>	0	—	0	—	0	—	0	—	ns
45	Access Time from CAS (Counter Test Cycle)		t <sub>CAT</sub>	—	43	—	45	—	50	—	60	ns
50	Fast Page Mode Read/Write Cycle Time		t <sub>PC</sub>	53	—	55	—	60	—	70	—	ns
51	Fast Page Mode Read-Modify-Write Cycle Time		t <sub>PRWC</sub>	105	—	107	—	115	—	130	—	ns
52	Access Time from CAS Precharge	9,18	t <sub>CPA</sub>	—	53	—	55	—	60	—	70	ns
53	Fast Page Mode CAS Precharge Time		t <sub>CP</sub>	10	—	10	—	10	—	15	—	ns

### Notes:

- Referenced to VSS
- ICC depends on the output load conditions and cycle rates; The specified values are obtained with the output open.  
ICC depends on the number of address change as RAS = V<sub>IL</sub> and CAS = V<sub>IH</sub>.  
ICC1, ICC3 and ICC5 are specified at three time of address change during RAS = V<sub>IL</sub> and CAS = V<sub>IH</sub>.  
ICC4 is specified at one time of address change during RAS = V<sub>IL</sub> and CAS = V<sub>IH</sub>.
- An Initial pause (RAS = CAS = V<sub>IH</sub>) of 200µs is required after power-up followed by any eight RAS-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight CAS-before-RAS initialization cycles instead of 8 RAS cycles are required.
- AC characteristics assume t<sub>r</sub> = 5ns
- V<sub>IH</sub> (min) and V<sub>IL</sub> (max) are reference levels for measuring timing of input signals. Also transition times are measured between V<sub>IH</sub> (min) and V<sub>IL</sub> (max).
- Assumes that t<sub>RCD</sub> ≤ t<sub>RCD</sub> (max), t<sub>RAD</sub> ≤ t<sub>RAD</sub> (max). If t<sub>RCD</sub> is greater than the maximum recommended value shown in this table, t<sub>RAC</sub> will be increased by the amount that t<sub>RCD</sub> exceeds the value shown. Refer to Fig. 2 and 3.
- Assumes that t<sub>RCD</sub> ≥ t<sub>RCD</sub> (max), t<sub>RAD</sub> ≥ t<sub>RAD</sub> (max). If t<sub>ASC</sub> ≥ t<sub>AA</sub> - t<sub>CAC</sub> - t<sub>T</sub>, access time is t<sub>CAC</sub>.
- If t<sub>RAD</sub> ≥ t<sub>RAD</sub> (max) and t<sub>ASC</sub> ≤ t<sub>AA</sub> - t<sub>CAC</sub> - t<sub>T</sub>, access time is t<sub>AA</sub>.
- Measured with a load equivalent to two TTL loads and 100 pF.
- t<sub>OFF</sub> and t<sub>OEZ</sub> is specified that output buffer change to high impedance state.
- Operation within the t<sub>RCD</sub> (max) limit ensures that t<sub>RAC</sub> (max) can be met. t<sub>RCD</sub> (max) is specified as a reference point only; if t<sub>RCD</sub> is greater than the specified t<sub>RCD</sub> (max) limit, access time is controlled exclusively by t<sub>CAC</sub> or t<sub>AA</sub>.
- t<sub>RCD</sub> (min) = t<sub>RAH</sub> (min) + 2t<sub>T</sub> + t<sub>ASC</sub> (min)
- Operation within the t<sub>RAD</sub> (max) limit ensures that t<sub>RAC</sub> (max) can be met. t<sub>RAD</sub> (max) is specified as a reference point only; if t<sub>RAD</sub> is greater than the specified t<sub>RAD</sub> (max) limit, access time is controlled exclusively by t<sub>CAC</sub> or t<sub>AA</sub>.
- Either t<sub>TRH</sub> or t<sub>TRC</sub> must be satisfied for a read cycle.
- t<sub>WC5</sub> is specified as a reference point only. If t<sub>WC5</sub> ≥ t<sub>WC5</sub> (min) the data output pin will remain High-Z state through entire cycle.
- Assumes that t<sub>WC5</sub> < t<sub>WC5</sub> (min)
- Either t<sub>DZC</sub> or t<sub>DZO</sub> must be satisfied.
- t<sub>CPA</sub> is access time from the selection of a new column address (that is caused by changing CAS from "L" to "H"). Therefore, if t<sub>CP</sub> is shortened, t<sub>CPA</sub> is longer than t<sub>CPA</sub> (max).
- Assumes that CAS-before-RAS refresh, CAS-before-RAS refresh counter test cycle only.

2

2



## FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input				Address		Input Data		Refresh	Note
	RAS	CAS	WE	OE	Row	Column	Input	Output		
Standby	H	H	X	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	L	Valid	Valid	—	Valid	Yes *	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L	L	X	Valid	Valid	Valid	High-Z	Yes *	$t_{WCS} \geq t_{WCS}$ (min)
Read-Modify-Write Cycle	L	L	H→L	L→H	Valid	Valid	Valid	Valid	Yes *	
RAS-only Refresh Cycle	L	H	X	X	Valid	—	—	High-Z	Yes	
CAS-before-RAS Refresh Cycle	L	L	X	X	—	—	—	High-Z	Yes	$t_{CSR} \geq t_{WCSR}$ (min)
Hidden Refresh	H→L	L	X	L	—	—	—	Valid	Yes	Previous data is kept.

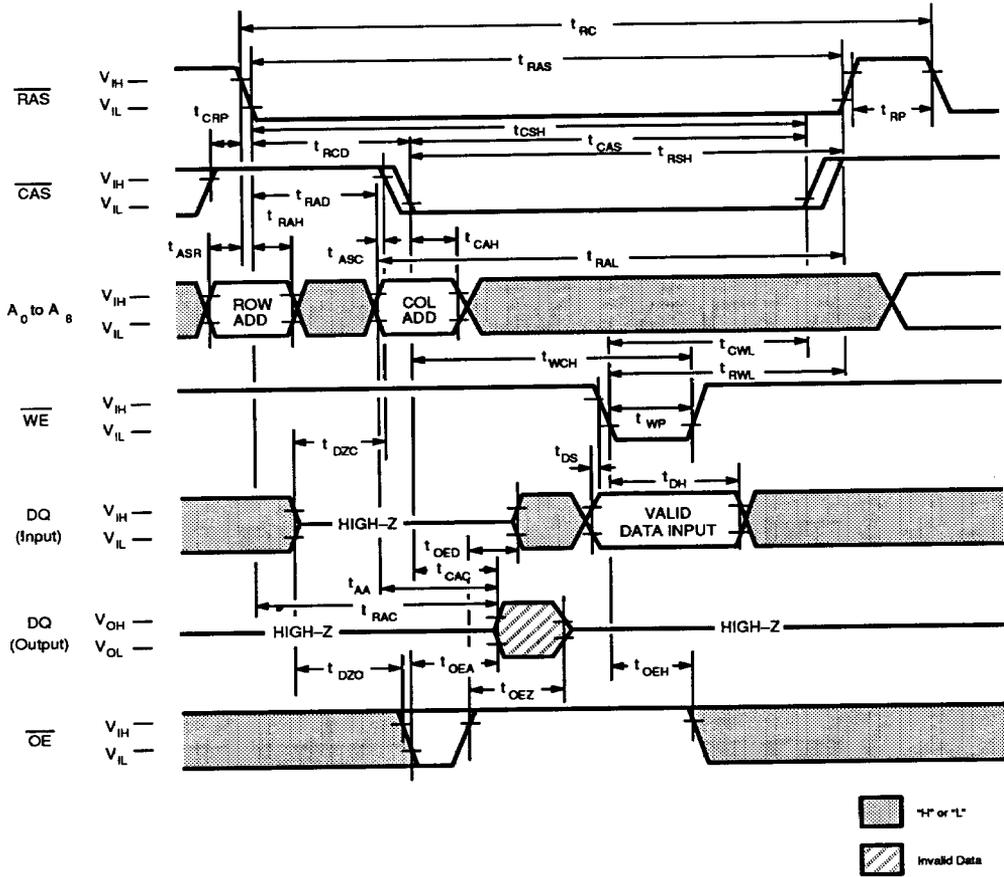
X: "H" or "L"  
 \*: It is impossible in Fast Page Mode





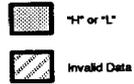
Fig. 6 -  $\overline{OE}$  ( DELAYED WRITE CYCLE )

2



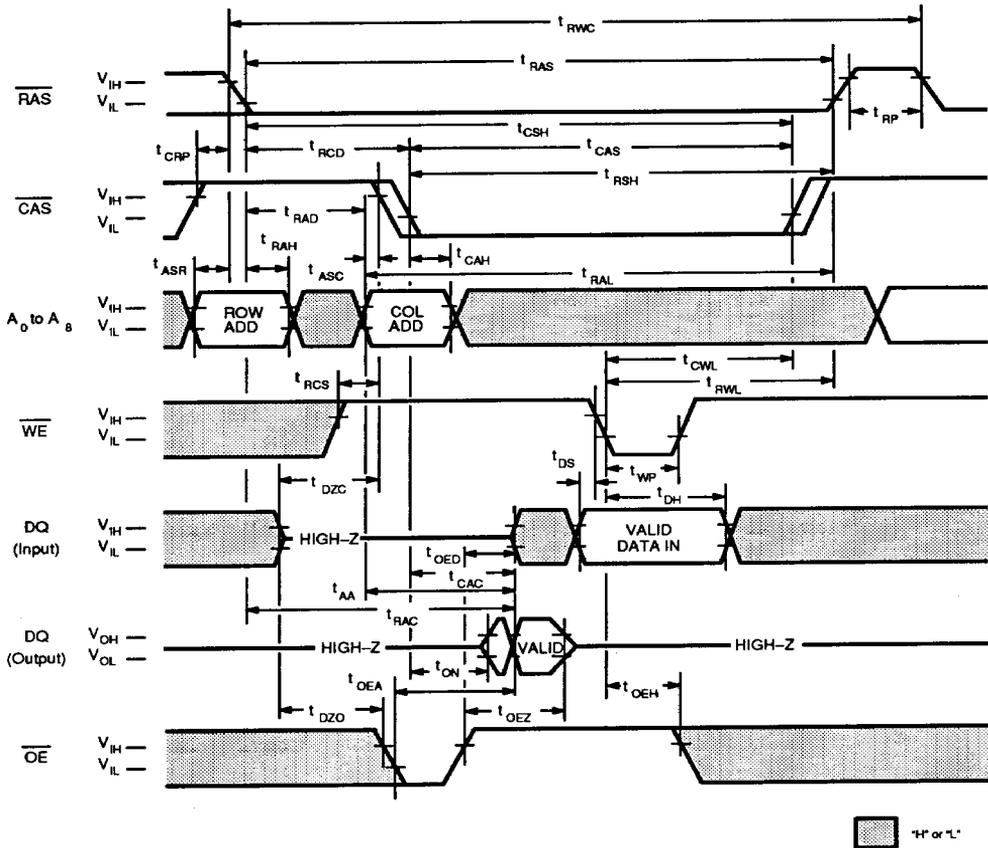
DESCRIPTION

In the  $\overline{OE}$  (delayed write) cycle,  $t_{WCS}$  is not satisfied; thus, the data on the  $DQ$  pins is latched with the falling edge of  $\overline{WE}$  and written into memory. The Output Enable ( $\overline{OE}$ ) signal must be changed from Low to High before  $\overline{WE}$  goes Low ( $t_{OED} + t_{DS}$ ).



2

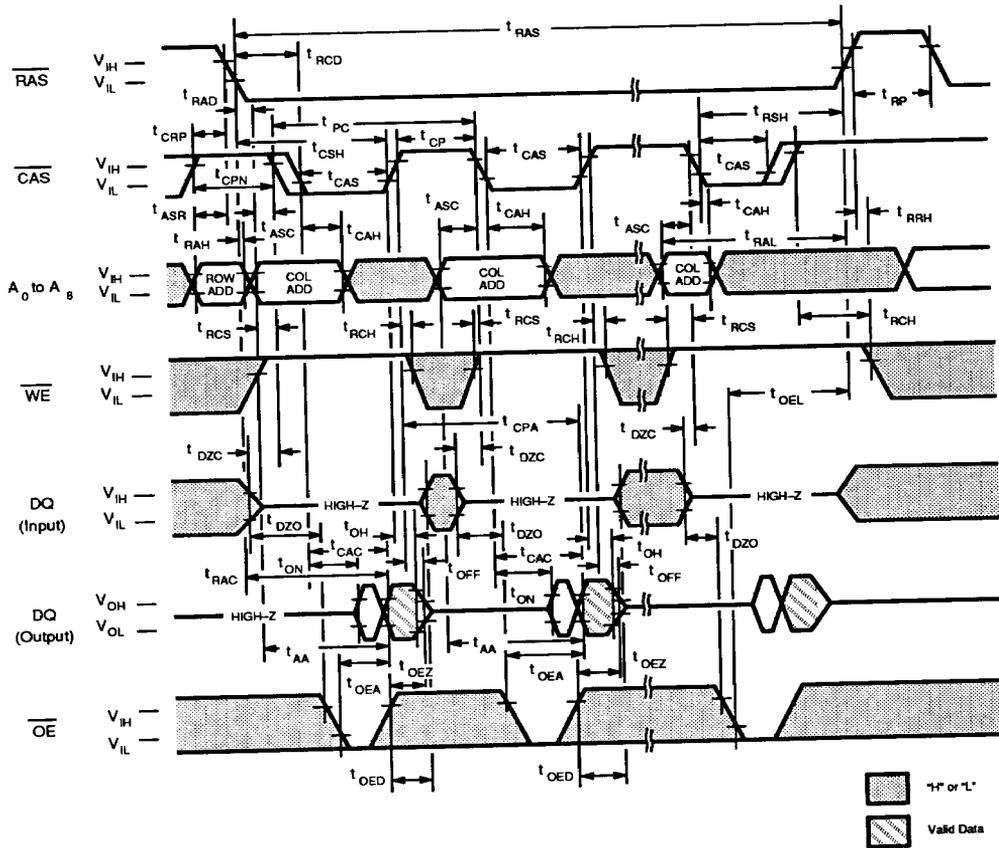
Fig. 7 - READ-MODIFY-WRITE CYCLE



DESCRIPTION

The read-modify-write cycle is executed by changing  $\overline{WE}$  from High to Low after the data appears on the DQ pins. In the read-modify-write cycle, OE must be changed from Low to High after the memory access time.

Fig. 8 - FAST PAGE MODE READ CYCLE

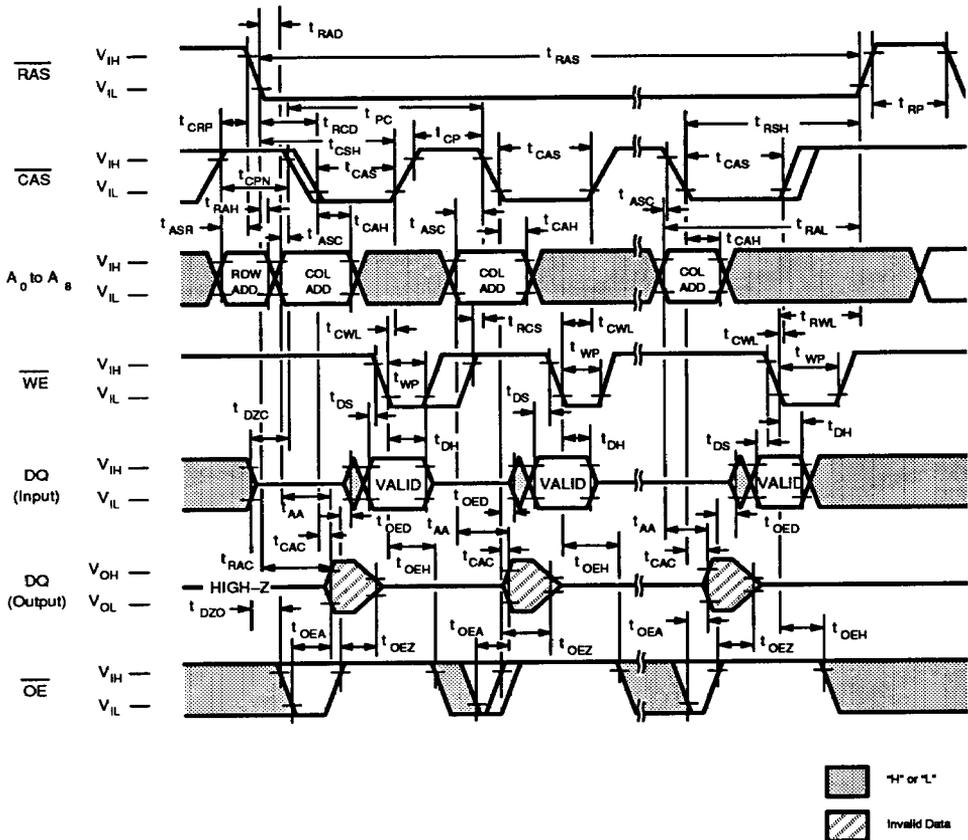


DESCRIPTION

The fast page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining RAS at a Low level and WE at a High level during all successive memory cycles in which the row address is latched. The access time is determined by tCAC, tAA, tCPA, or tOEA, whichever one is the latest in occurring.



Fig. 10 - FAST PAGE MODE  $\overline{OE}$  WRITE CYCLE

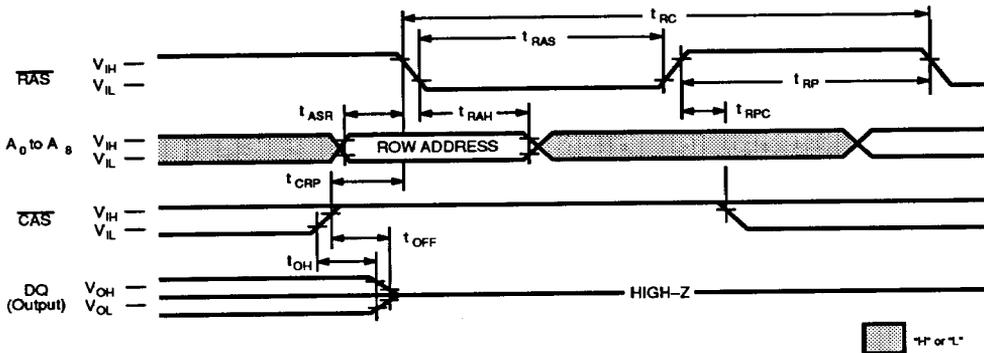


DESCRIPTION

The fast page mode  $\overline{OE}$  (delayed) write cycle is executed in the same manner as the fast page mode write cycle except for the states of WE and OE. Input data on the DQ pins are latched on the falling edge of WE and written into memory. In the fast page mode delayed write cycle, OE must be changed from Low to High before WE goes Low ( $t_{OED} + t_{DS}$ ).



Fig. 12 -  $\overline{\text{RAS}}$ -ONLY REFRESH ( $\overline{\text{WE}} = \overline{\text{OE}} = \text{"H"}$  or  $\text{"L"}$ )



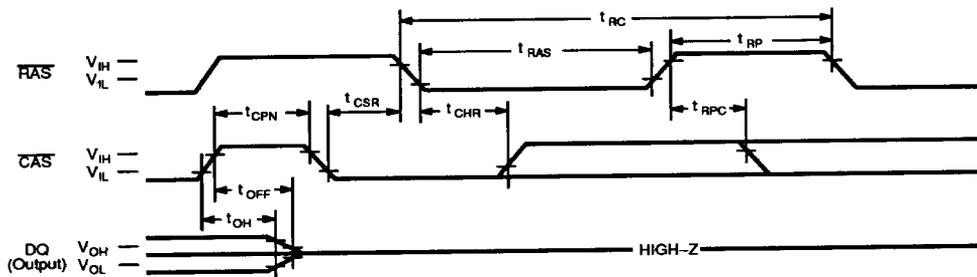
**DESCRIPTION**

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 512 row addresses every 8.2-milliseconds. Three refresh modes are available:  $\overline{\text{RAS}}$ -only refresh,  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh, and hidden refresh.

$\overline{\text{RAS}}$ -only refresh is performed by keeping  $\overline{\text{RAS}}$  Low and  $\overline{\text{CAS}}$  High throughout the cycle; the row address to be refreshed is latched on the falling edge of  $\overline{\text{RAS}}$ . During  $\overline{\text{RAS}}$ -only refresh, Dour pin is kept in a high-impedance state.

2

Fig. 13 -  $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$  REFRESH (ADDRESSES =  $\overline{\text{WE}} = \overline{\text{OE}} = \text{"H"}$  or  $\text{"L"}$ )

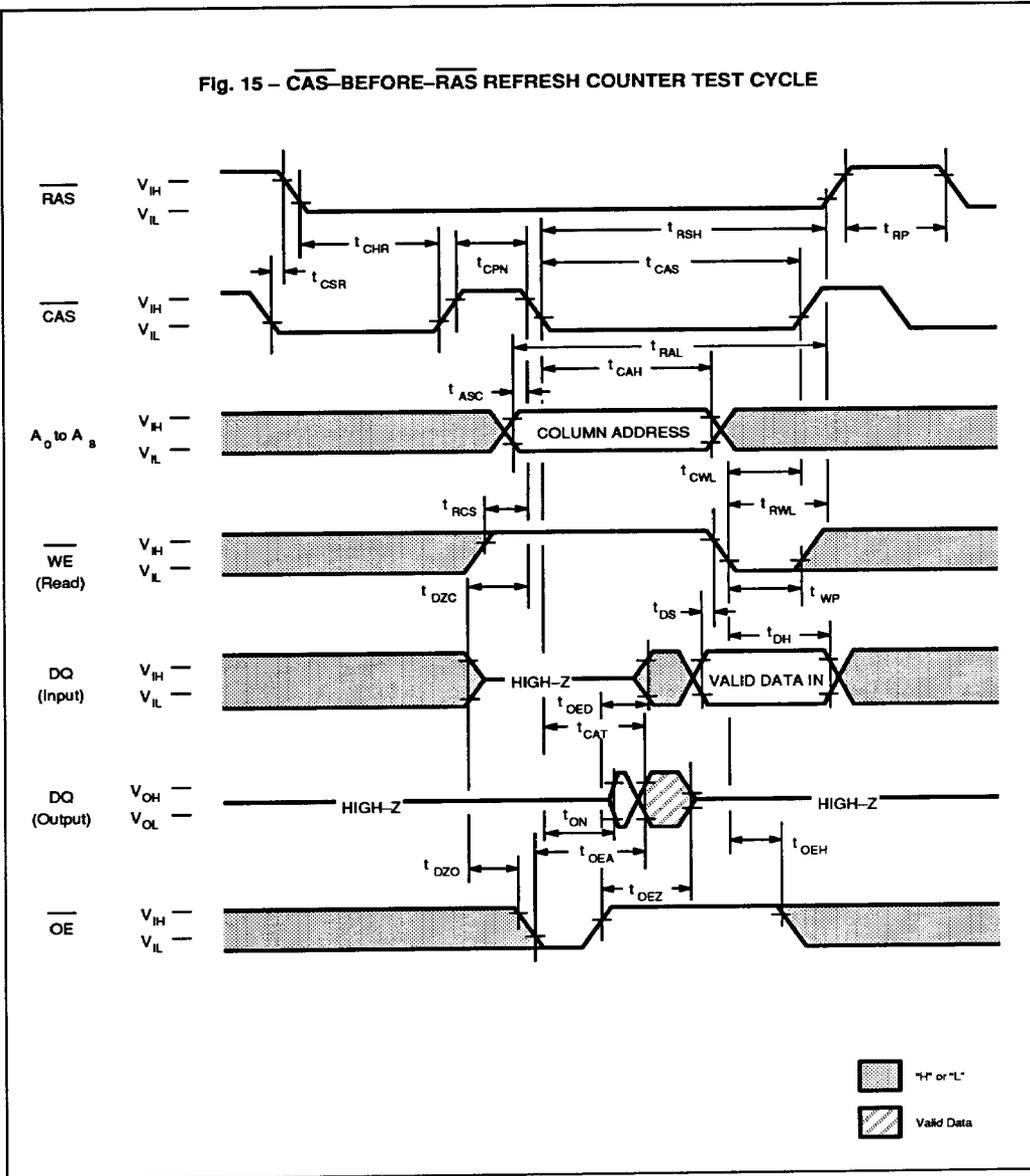


**DESCRIPTION**

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If  $\overline{\text{CAS}}$  is held Low for the specified setup time ( $t_{\text{CSR}}$ ) before  $\overline{\text{RAS}}$  goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh operation.



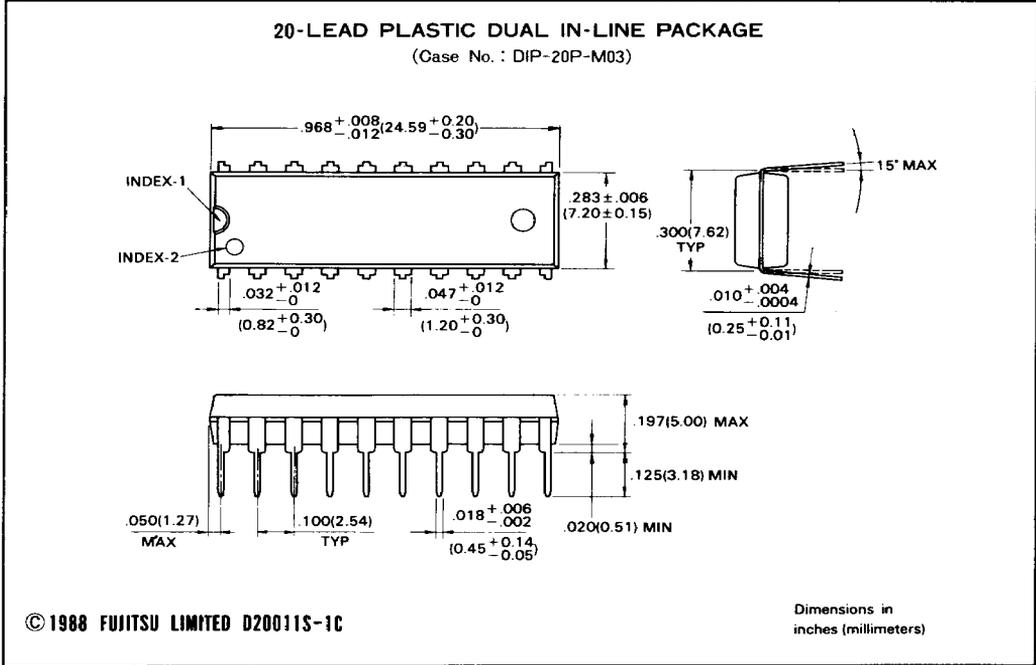
Fig. 15 -  $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$  REFRESH COUNTER TEST CYCLE



**MB81C4256-70**  
**MB81C4256-80**  
**MB81C4256-10**  
**MB81C4256-12**

## PACKAGE DIMENSIONS

(Suffix : -P)



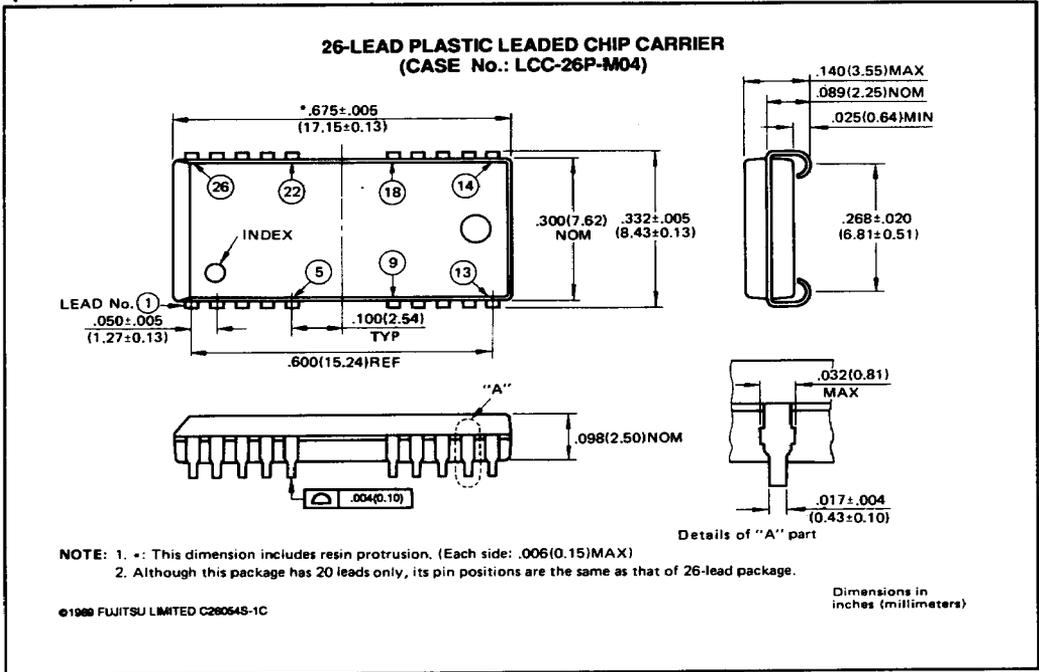
2



MB81C4256-70  
 MB81C4256-80  
 MB81C4256-10  
 MB81C4256-12

## PACKAGE DIMENSIONS (Continued)

(Suffix : -PJ)

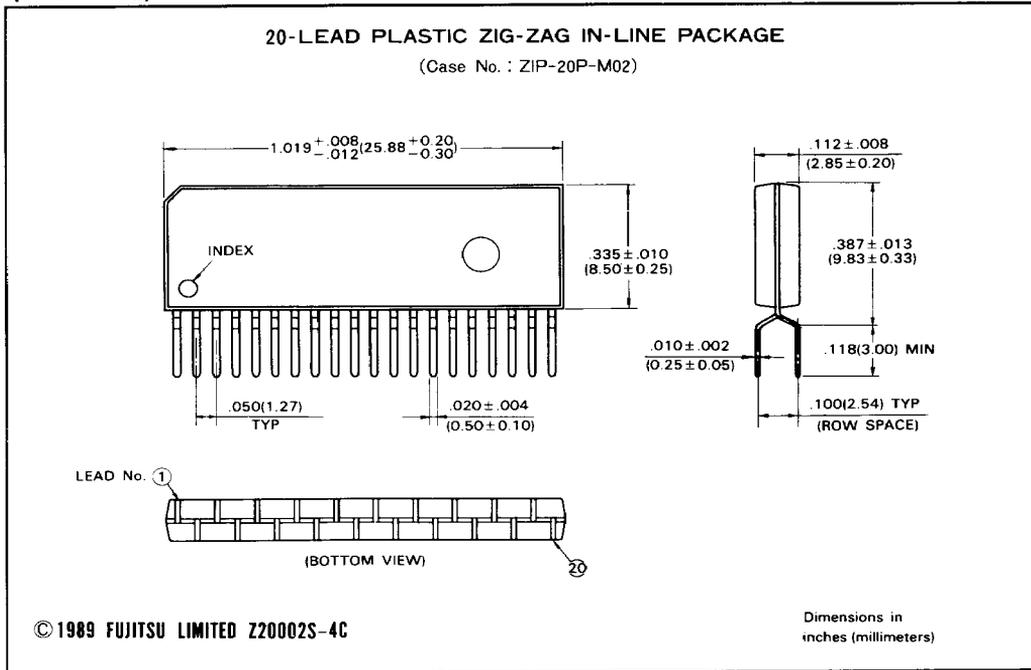


2

MB81C4256-70  
MB81C4256-80  
MB81C4256-10  
MB81C4256-12

## PACKAGE DIMENSIONS (Continued)

(Suffix : -PSZ)



2