

## FEATURES

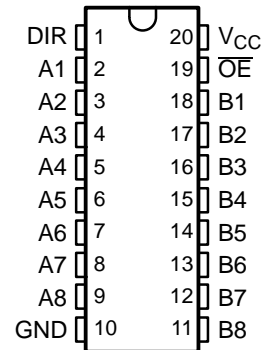
- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 6.3 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) >2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

## DESCRIPTION/ORDERING INFORMATION

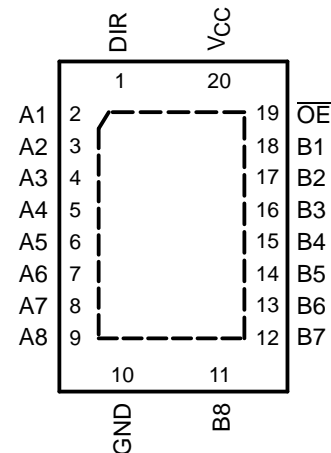
This octal bus transceiver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74LVC245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so the buses effectively are isolated.

DB, DGV, DW, N, NS, OR PW PACKAGE  
(TOP VIEW)



RGY PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube of 20	SN74LVC245AN	SN74LVC245AN
	QFN – RGY	Reel of 1000	SN74LVC245ARGYR	LC245A
	SOIC – DW	Tube of 25	SN74LVC245ADW	LVC245A
		Reel of 2000	SN74LVC245ADWR	
	SOP – NS	Reel of 2000	SN74LVC245ANSR	LVC245A
	SSOP – DB	Reel of 2000	SN74LVC245ADBR	LC245A
	TSSOP – PW	Tube of 70	SN74LVC245APW	LC245A
		Reel of 2000	SN74LVC245APWR	
		Reel of 250	SN74LVC245APWT	
	TVSOP – DGV	Reel of 2000	SN74LVC245ADGVR	LC245A
VFBGA – GQN	Reel of 1000	SN74LVC245AGQNR	LC245A	
VFBGA – ZQN (Pb-Free)		SN74LVC245AZQNR		

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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# SN74LVC245A OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS218T–JANUARY 1993–REVISED FEBRUARY 2005

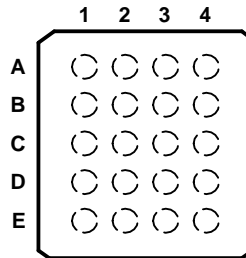
## DESCRIPTION/ORDERING INFORMATION (CONTINUED)

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

GQN OR ZQN PACKAGE  
(TOP VIEW)



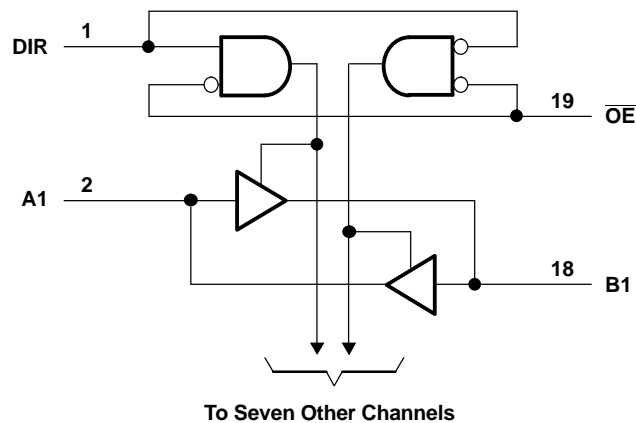
## TERMINAL ASSIGNMENTS

	1	2	3	4
A	A1	DIR	$V_{CC}$	$\overline{OE}$
B	A3	B2	A2	B1
C	A5	A4	B4	B3
D	A7	B6	A6	B5
E	GND	A8	B8	B7

## FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

## LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DB, DGV, DW, N, NS, PW, and RGY packages.

**Absolute Maximum Ratings<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	6.5	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	6.5	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	6.5	V
$V_O$	Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$	-50	mA
$I_{OK}$	Output clamp current	$V_O < 0$	-50	mA
$I_O$	Continuous output current		±50	mA
	Continuous current through $V_{CC}$ or GND		±100	mA
$\theta_{JA}$	Package thermal impedance	DB package <sup>(4)</sup>	70	°C/W
		DGV package <sup>(4)</sup>	92	
		DW package <sup>(4)</sup>	58	
		GQN/ZQN package <sup>(4)</sup>	78	
		N package <sup>(4)</sup>	69	
		NS package <sup>(4)</sup>	60	
		PW package <sup>(4)</sup>	83	
	RGY package <sup>(5)</sup>	37		
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of  $V_{CC}$  is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) The package thermal impedance is calculated in accordance with JESD 51-5.

# SN74LVC245A OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

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## Recommended Operating Conditions<sup>(1)</sup>

		$T_A = 25^\circ\text{C}$		$-40^\circ\text{C TO } 85^\circ\text{C}$		UNIT	
		MIN	MAX	MIN	MAX		
$V_{CC}$	Supply voltage	Operating	1.65	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
$V_{IH}$	High-level input voltage	$V_{CC} = 1.65\text{ V to } 1.95\text{ V}$	$0.65 \times V_{CC}$		$0.65 \times V_{CC}$		V
		$V_{CC} = 2.3\text{ V to } 2.7\text{ V}$	1.7		1.7		
		$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$	2		2		
$V_{IL}$	Low-level input voltage	$V_{CC} = 1.65\text{ V to } 1.95\text{ V}$	$0.35 \times V_{CC}$		$0.35 \times V_{CC}$		V
		$V_{CC} = 2.3\text{ V to } 2.7\text{ V}$	0.7		0.7		
		$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$	0.8		0.8		
$V_I$	Input voltage	0	5.5	0	5.5	V	
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	V	
$I_{OH}$	High-level output current	$V_{CC} = 1.65\text{ V}$	-4		-4		mA
		$V_{CC} = 2.3\text{ V}$	-8		-8		
		$V_{CC} = 2.7\text{ V}$	-12		-12		
		$V_{CC} = 3\text{ V}$	-24		-24		
$I_{OL}$	Low-level output current	$V_{CC} = 1.65\text{ V}$	4		4		mA
		$V_{CC} = 2.3\text{ V}$	8		8		
		$V_{CC} = 2.7\text{ V}$	12		12		
		$V_{CC} = 3\text{ V}$	24		24		
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V	

(1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			–40°C TO 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –100 μA	1.65 V to 3.6 V	V <sub>CC</sub> – 0.2			V <sub>CC</sub> – 0.2		V
	I <sub>OH</sub> = –4 mA	1.65 V	1.29			1.2		
	I <sub>OH</sub> = –8 mA	2.3 V	1.9			1.7		
	I <sub>OH</sub> = –12 mA	2.7 V	2.2			2.2		
		3 V	2.4			2.4		
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V				0.1	0.2	V
	I <sub>OL</sub> = 4 mA	1.65 V				0.24	0.45	
	I <sub>OL</sub> = 8 mA	2.3 V				0.3	0.7	
	I <sub>OL</sub> = 12 mA	2.7 V				0.4	0.4	
	I <sub>OL</sub> = 24 mA	3 V				0.55	0.55	
I <sub>I</sub>	Control inputs	V <sub>I</sub> = 0 to 5.5 V	3.6 V			±1	±5	μA
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0			±1	±10	μA
I <sub>OZ</sub> <sup>(1)</sup>		V <sub>O</sub> = 0 to 5.5 V	3.6 V			±1	±10	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND 3.6 V ≤ V <sub>I</sub> ≤ 5.5 V <sup>(2)</sup>	I <sub>O</sub> = 0	3.6 V			1	10	μA
						1	10	
ΔI <sub>CC</sub>		One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V			500	500	μA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V			4		pF
C <sub>io</sub>	A or B ports	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V			5.5		pF

(1) For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

(2) This applies in the disabled state only.

## Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			–40°C TO 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	B or A	1.8 V ± 0.15 V	1	6	12.2	1	12.7	ns
			2.5 V ± 0.2 V	1	3.9	7.8	1	8.3	
			2.7 V	1	4.2	7.1	1	7.3	
			3.3 V ± 0.3 V	1.5	3.8	6.1	1.5	6.3	
t <sub>en</sub>	OE	A or B	1.8 V ± 0.15 V	1	7	14.8	1	15.3	ns
			2.5 V ± 0.2 V	1	4.5	10	1	10.5	
			2.7 V	1	5.4	9.3	1	9.5	
			3.3 V ± 0.3 V	1.5	4.4	8.3	1.5	8.5	
t <sub>dis</sub>	OE	A or B	1.8 V ± 0.15 V	1	7.8	16.5	1	17	ns
			2.5 V ± 0.2 V	1	4	9	1	9.5	
			2.7 V	1	4.4	8.3	1	8.5	
			3.3 V ± 0.3 V	1.7	4.1	7.3	1.7	7.5	
t <sub>sk(o)</sub>			3.3 V ± 0.3 V				1	ns	

**SN74LVC245A**  
**OCTAL BUS TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

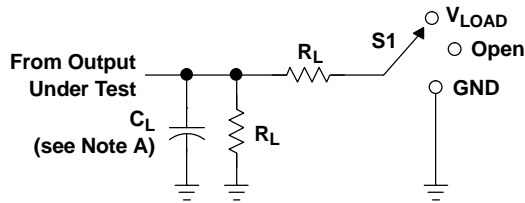
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**Operating Characteristics**

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC}$	TYP	UNIT	
$C_{pd}$	Power dissipation capacitance per transceiver	f = 10 MHz	Outputs enabled	1.8 V	42	pF
				2.5 V	43	
			3.3 V	45		
	Outputs disabled		1.8 V	1		
			2.5 V	1		
			3.3 V	2		

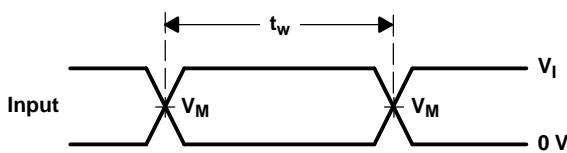
PARAMETER MEASUREMENT INFORMATION



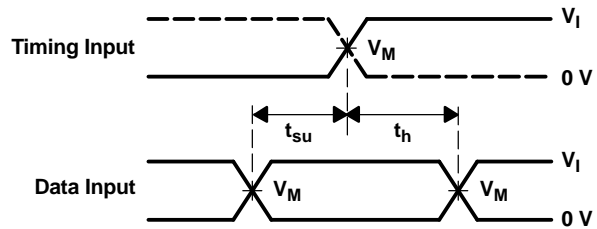
LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

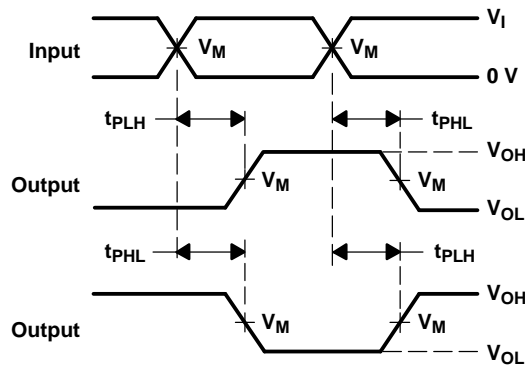
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



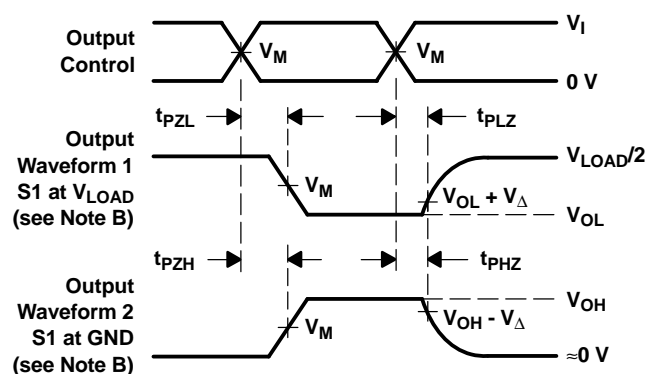
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LVC245ADBLE	OBSOLETE	SSOP	DB	20		None	Call TI	Call TI
SN74LVC245ADBR	ACTIVE	SSOP	DB	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LVC245ADGVR	ACTIVE	TVSOP	DGV	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LVC245ADW	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74LVC245ADWR	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74LVC245AGQNR	ACTIVE	VFBGA	GQN	20	1000	None	SNPB	Level-1-240C-UNLIM
SN74LVC245AN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LVC245ANSR	ACTIVE	SO	NS	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LVC245APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC245APWLE	OBSOLETE	TSSOP	PW	20		None	Call TI	Call TI
SN74LVC245APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC245APWT	ACTIVE	TSSOP	PW	20	250	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LVC245ARGYR	ACTIVE	QFN	RGY	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74LVC245AZQNR	ACTIVE	VFBGA	ZQN	20	1000	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

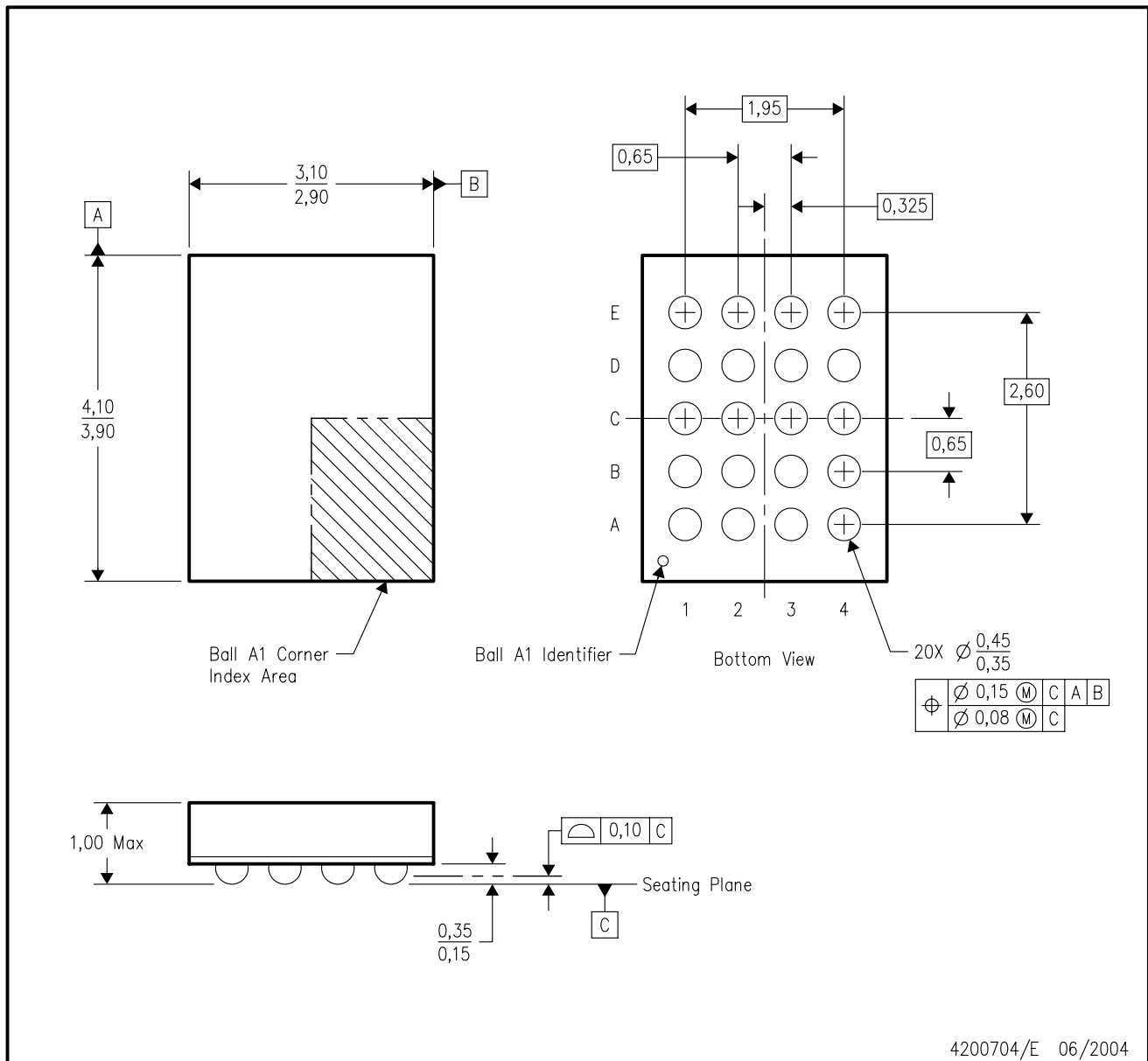
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GQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY

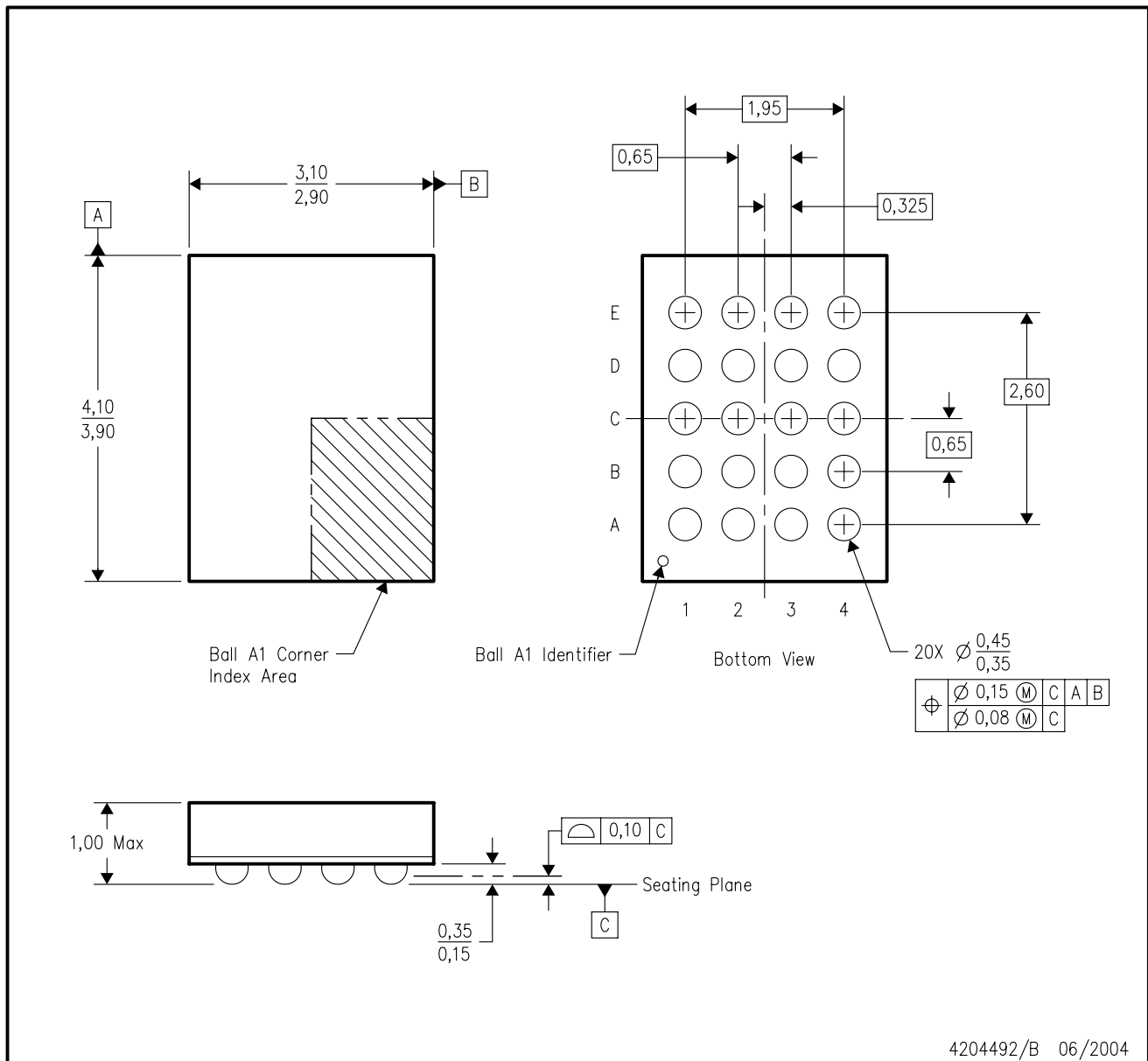


4200704/E 06/2004

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-225 variation BC.
  - D. This package is tin-lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead-free.

ZQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-225 variation BC.
  - D. This package is lead-free. Refer to the 20 GQN package (drawing 4200704) for tin-lead (SnPb).

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G20)

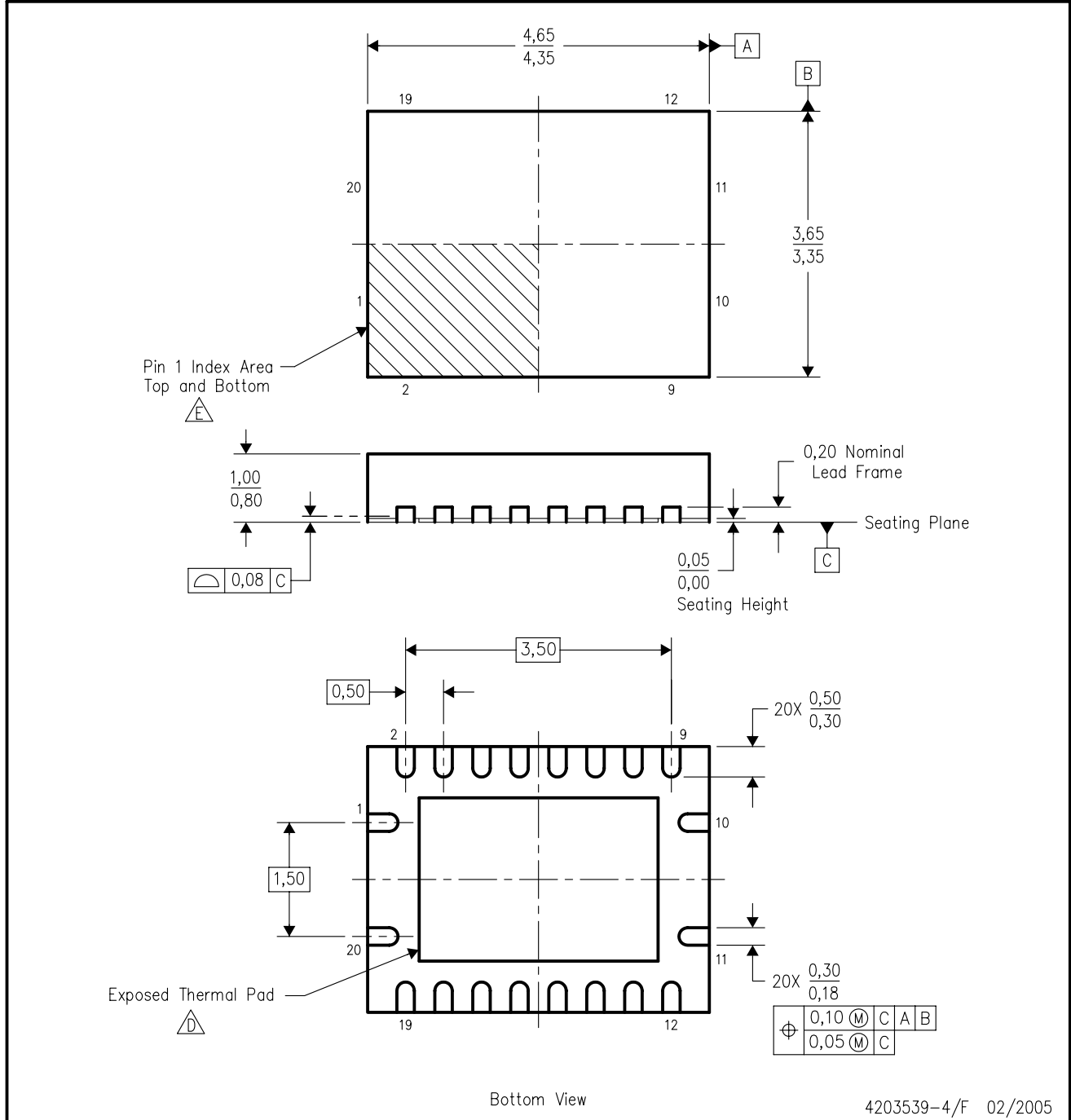
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

RGY (R-PQFP-N20)

PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - F. Package complies to JEDEC MO-241 variation BC.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265