M74LS670P

4-BY-4 REGISTER FILE WITH 3-STATE OUTPUTS

DESCRIPTION

The M74LS670P is a semiconductor integrated circuit containing a 4 word x 4 bit register file circuit with 3-state outputs.

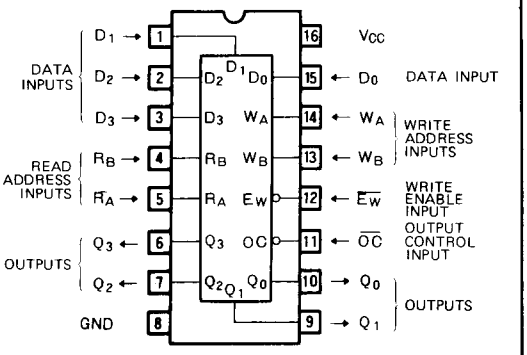
FEATURES

- Since read address and write address are independent, simultaneous writing and reading of data is possible.
- Provided with read enable input and output control inputs
- Storage capacity can be easily expanded with the aid of the enable input.
- AND-tie may be used (With 3-state output)
  Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16 P4

FUNCTIONAL DESCRIPTION

16 flip-flops are used as storage devices, and a discrete enable input, address input, and output controlling input are provided for reading and writing. Accordingly, during writing, the contents of other words can be read, and during reading, other words can be written, thereby enhansing to high-speed operation.

The 3-state output permits 128-output AND-tie even in the worst condition. Expansion of up to 512 words is possible. possible.

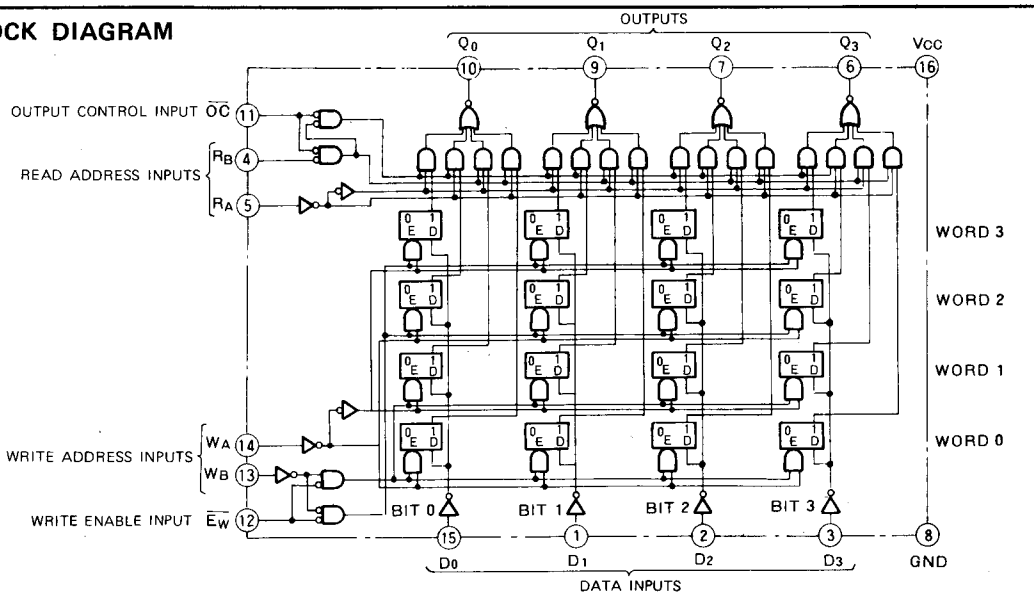
Writing Method

By designating a word using write address inputs W_A and W_B and applying data to the data inputs D_0, D_1, D_2, and D_3, writing into each bit is performed. For writing the write enable input $\overline{E_W}$ is held low (Writing will not be performed if $\overline{E_W}$ is high)

Readout Method

When a word is designated by read address inputs R_A and R_B, the contents of each bit appear in the outputs Q_0, Q_1, Q_2, and Q_3. For reading the output control input $\overline{OC}$ is held low. (when $\overline{OC}$ is high, all the outputs are in the high-impedance state).

BLOCK DIAGRAM



4-BY-4 REGISTER FILE WITH 3-STATE OUTPUTS

FUNCTION TABLE (Note 1)

Writing Method

W_A	W_B	$\overline{E_W}$	Word 0	Word 1	Word 2	Word 3
X	X	H	Q^0	Q^0	Q^0	Q^0
L	L	L	Q=D	Q^0	Q^0	Q^0
H	L	L	Q^0	Q=D	Q^0	Q^0
L	H	L	Q^0	Q^0	Q=D	Q^0
H	H	L	Q^0	Q^0	Q^0	Q=D

Readout Method

R_A	R_B	$\overline{OC}$	Q_0	Q_1	Q_2	Q_3
X	X	H	Z	Z	Z	Z
L	L	L	W_0B_0	W_0B_1	W_0B_2	W_0B_3
H	L	L	W_1B_0	W_1B_1	W_1B_2	W_1B_3
L	H	L	W_2B_0	W_2B_1	W_2B_2	W_2B_3
H	H	L	W_3B_0	W_3B_1	W_3B_2	W_3B_3

Note 1: Q^0 : The level of Q before the indicated steady-state input conditions were established.

Q=D : The four selected internal latch outputs will assume the states applied to the four external data inputs.

W_XB_Y : The Yth bit of word X. X : irrelevant Z : high-impedance

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C,)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	Off-state	−0.5 ~ +5.5	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	V_{OH}≧2.4V	0		−2.6	mA
I_{OL}	Low-level output current	V_{OL}≦0.4V	0		4	mA
		V_{OL}≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS (T_a = −20 ~ +70°C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits Min	Limits Typ*	Limits Max	Unit
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC}=4.75V, V_I=0.8V, V_I=2V, I_{OH}=−2.6mA		2.4	3.1		V
V_{OL}	Low-level output voltage		V_{CC}=4.75V, V_I=0.8V, V_I=2V	I_{OL}=4mA		0.25	0.4	V
				I_{OL}=8mA		0.35	0.5	V
I_{OZH}	Off-state high-level output current		V_{CC}=5.25V, V_I=2V, V_I=2.7V				20	μA
I_{OZL}	Off-state low-level output current		V_{CC}=5.25V, V_I=2V, V_I=0.4V				−20	μA
I_{IH}	High-level input current	$\overline{E_W}$	V_{CC}=5.25V, V_I=2.7V				40	μA
		$\overline{OC}$					60	μA
		Other input					20	μA
		$\overline{E_W}$	V_{CC}=5.25V, V_I=10V				0.2	mA
		$\overline{OC}$					0.3	mA
		Other input					0.1	mA
I_{IL}	Low-level input current	$\overline{E_W}$	V_{CC}=5.25V, V_I=0.4V				−0.8	mA
		$\overline{OC}$					−1.2	mA
		Other input					−0.4	mA
I_{OS}	Short-circuit output current (Note 2)		V_{CC}=5.25V, V_O=0V		−30		−130	mA
I_{CC}	Supply current		V_{CC}=5.25V (Note 3)			30	50	mA

* : All typical values are at V_{CC} = 5V, Ta = 25°C.

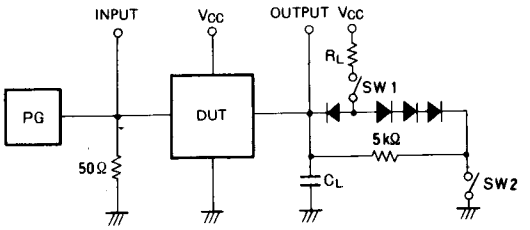
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

3: Icc is measured with W_A, W_B, R_A, R_B inputs grounded and D_0 ~ D_3, $\overline{E_W}$, $\overline{OC}$ inputs at 4.5V.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input R_A, R_B to output Q_0, Q_1, Q_2, Q_3	C_L=15pF (Note 4)		11	40	ns
t_{PHL}				14	45	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{E_W}$ to output Q_0, Q_1, Q_2, Q_3			11	45	ns
t_{PHL}				16	50	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input D_0, D_1, D_2, D_3 to output Q_0, Q_1, Q_2, Q_3			9	45	ns
t_{PHL}				14	40	ns
t_{PZH}	Output enable time to high-level	R_L=2kΩ, C_L=15pF (Note 4)		6	35	ns
t_{PZL}	Output enable time to low-level	R_L=2kΩ, C_L=15pF (Note 4)		10	40	ns
t_{PHZ}	Output disable time from high-level	R_L=2kΩ, C_L= 5pF (Note 4)		16	50	ns
t_{PLZ}	Output disable time from low-level	R_L=2kΩ, C_L= 5pF (Note 4)		7	35	ns

Note 4: Measurement circuit



Symbol	SW 1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

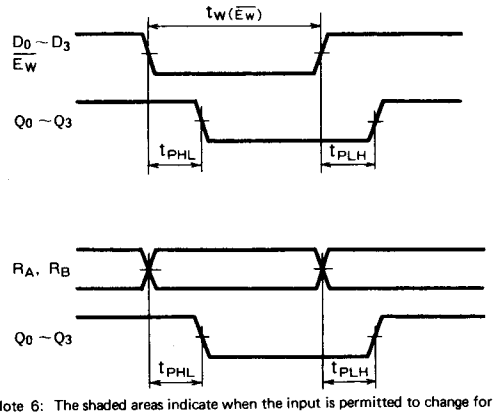
(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns,
V_P = $3V_{P-P}$, Z_O = 50Ω
(2) All diodes are switching diodes ($t_{rr} \leqq$ 4ns)
(3) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

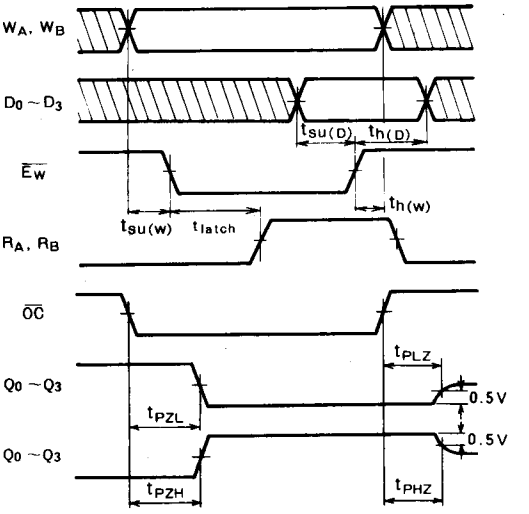
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(\overline{E_W})}$	Write enable input $\overline{E_W}$ pulse width		25	9		ns
$t_{W(\overline{OC})}$	Output control input $\overline{OC}$ pulse width		25	9		ns
$t_{SU(D)}$	Setup time D_0~D_3 to $\overline{E_W}$		10	5		ns
$t_{SU(W)}$	Setup time W_A, W_B to $\overline{E_W}$		15	−2		ns
$t_{h(D)}$	Hold time D_0~D_3 to $\overline{E_W}$		15	1		ns
$t_{h(W)}$	Hold time W_A, W_B to $\overline{E_W}$		5	0		ns
tlatch	Latch time for new date (Note 5)		25	5		ns

Note 5: Latch time is the time allowed for the internal output of the latch to assume the state of new data.

TIMING DIAGRAM (Reference level = 1.3V)

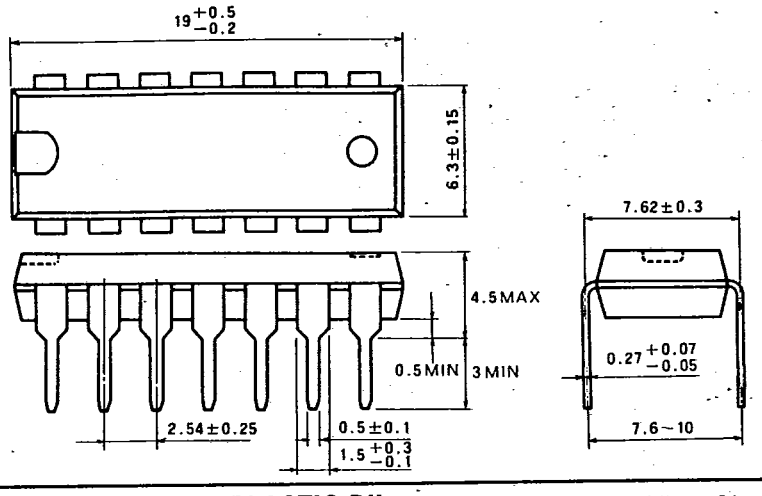


Note 6: The shaded areas indicate when the input is permitted to change for predictable output performance.



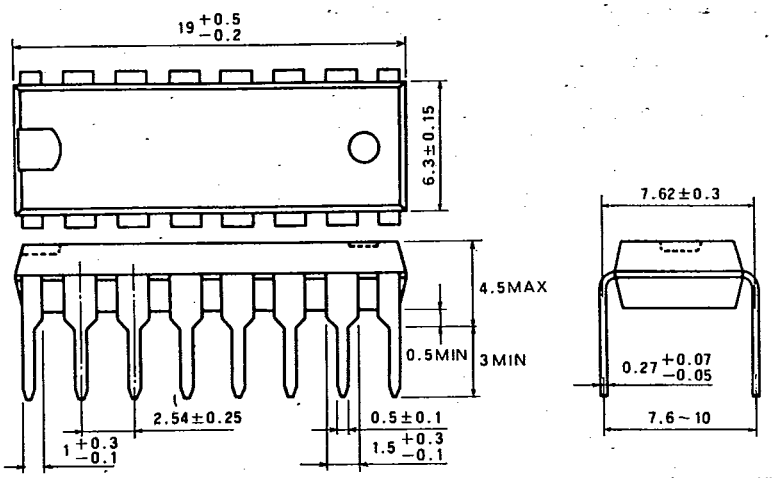
TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimension in mm