HM66204 Series

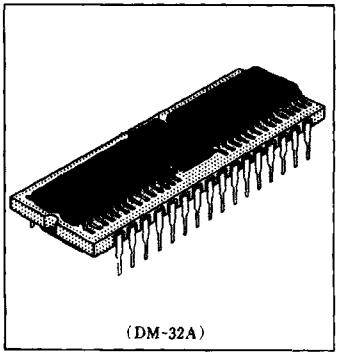
131072-word x 8-bit High Density Static RAM Module

The HM66204 is a high density 1 M-bit static RAM module consisted of 4 pieces of HM62256FP/LFP products (SOP type 256k static RAM) and a HD74HC138FP equivalent product (SOP type CMOS decoder logic).

An outline of the HM66204 is the standard 600 mil width 32 pin dual-in-line package. Its pin arrangement is completely compatible with 1 M-bit monolithic static RAM.

The HM66204 offers the features of low power and high speed by using high speed CMOS devices. And, the HM66204 makes high density mounting possible with no surface mount technology.

These features make the HM66204 ideally suited for high density compacted memory systems.

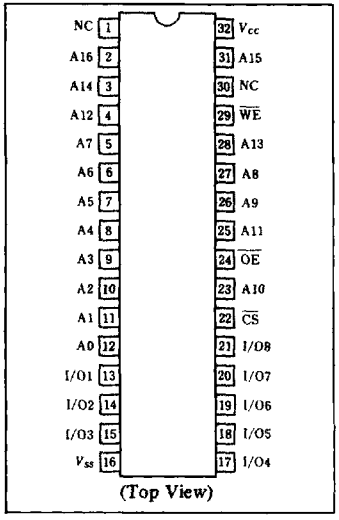


(DM-32A)

Features

- High density 32 pin DIP
  - Mounting 4 pcs. of 256k static RAM (SOP; HM62256FP/LFP) and CMOS decoder logic (SOP; HD74HC138FP equivalent)
- Pin compatible with 1M monolithic static RAM
- High speed
  - Fast access time 120 ns/150 ns (maximum)
- Equal access and cycle time
- Completely static RAM
  - No clock or timing strobe required
- Low power standby and low power operation
  - Standby 40 μW (typical) (L-version)
  - Operation 50 mW (typical) (f = 1 MHz)
- Common data input and output, three state outputs
- Capable of battery backup operation (L-version)

Pin Arrangement



(Top View)

Ordering Information

Part No.	Access Time	Package
HM66204-12	120 ns	600 mil 32-pin DIP
HM66204-15	150 ns	
HM66204L-12	120 ns	
HM66204L-15	150 ns	

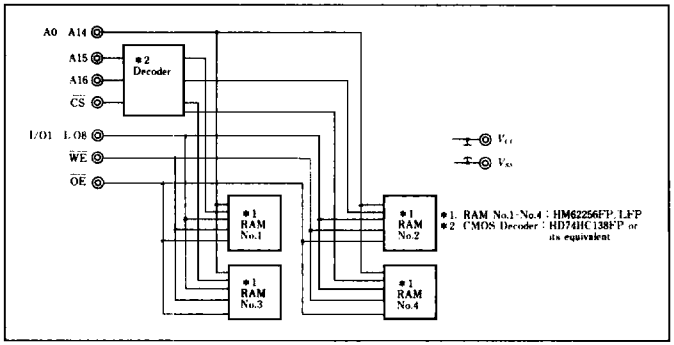
Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5 to +7.0	V
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	−55 to +125	°C
Storage temperature range under bias	Tbias	−10 to +85	°C
Power dissipation	P_T	1.0	W

Pin Description

Pin Name	Function
A0 - A16	Address
I/O1 - I/O8	Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

Block Diagram



Mode Selection

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O	Current	Note
Not selected (Power down)	H	×	×	High-Z	I_{BS}, I_{SB1}	
Read	L	H	L	Dout	I_{CC}	Read cycle (1) – (3)
Write	L	L	H	Din	I_{CC}	Write cycle (1)
	L	L	L	Din	I_{CC}	Write cycle (2)

Note) × = Don't care (H or L)

Electrical Characteristics

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input high (logic 1) Voltage	V_{IH}	3.85	–	6.0	V	A15, A16, $\overline{CS}$
		2.2	–	6.0	V	Others except A15, A16, $\overline{CS}$
Input low (logic 0) Voltage	V_{IL}	–0.5	–	0.8	V	

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test Conditions	Notes
Input leakage current	$\|I_{LI}\|$	–	–	2	μA	V_{IN} = V_{SS} to V_{CC}	
Output leakage current	$\|I_{LO}\|$	–	–	2	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}	
Operating power supply current: DC	I_{CC}	–	10	25	mA	$\overline{CS}$ = V_{IL} $I_{I/O}$ = 0mA	
Average operating power supply current (1)	I_{CC1}	–	37	80	mA	MIN. cycle duty = 100%	–12
		–	35	80		$I_{I/O}$ = 0mA	–15
Average operating power supply current (2)	I_{CC2}	–	10	15	mA	$\overline{CS}$ = V_{IL}, V_{IH} = V_{CC} V_{IL} = 0V, $I_{I/O}$ = 0mA f = 1MHz	
Standby power supply current: DC	I_{SB}	–	2	12	mA	$\overline{CS}$ = V_{IH}	
Standby power supply current (1): DC	I_{SB1}	–	8	400	μA	$\overline{CS}$ ≥ V_{CC}–0.2V A15, A16 ≥ V_{CC}–0.2V	HM66204L Series
		–	0.16	8	mA	or A15, A16 ≤ 0.2V	
Output low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 2.1 mA	
Output high voltage	V_{OH}	2.4	–	–	V	I_{OH} = –1.0 mA	

Note) *1. Typical values are at V_{CC} = 5.0V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	–	–	45	pF	Vin = 0V
Input/output capacitance	$C_{I/O}$	–	–	50	pF	$V_{I/O}$ = 0V

Note) This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

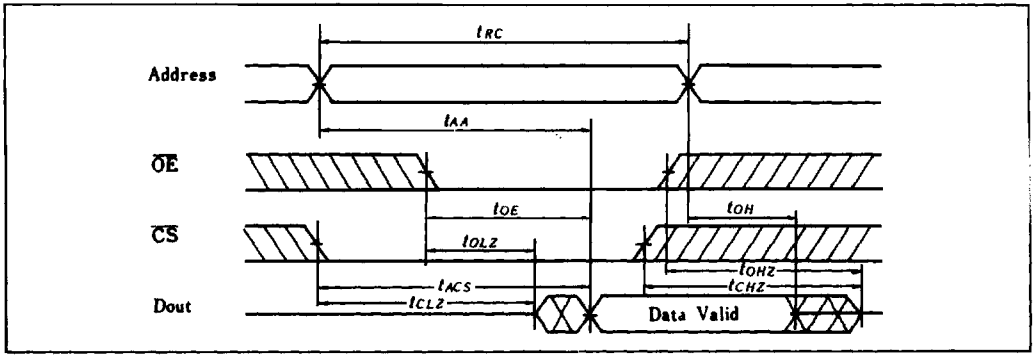
AC Test Conditions

- Input pulse levels:
  0.8V to 4.0V . . . $\overline{CS}$, A15, A16
  0.8V to 2.4V . . . Other pin except $\overline{CS}$, A15, A16
- Input rise and fall times: 5 ns
- Input and output timing reference level: 1.5V
- Output load: 1 TTL Gate and C_L (100pF) (Including scope & jig)

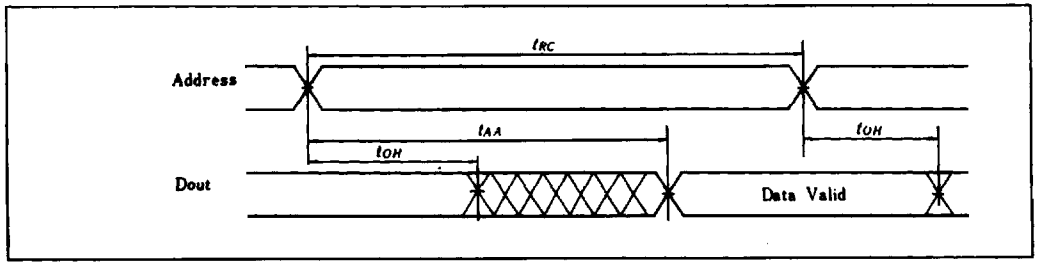
Read Cycle

Parameter	Symbol	HM66204-12		HM66204-15		Unit
		min	max	min	max	
Read cycle time	t_{RC}	120	–	150	–	ns
Address access time	t_{AA}	–	120	–	150	ns
Chip select access time	t_{ACS}	–	120	–	150	ns
Output enable to output valid	t_{OE}	–	60	–	70	ns
Output hold from address change	t_{OH}	10	–	10	–	ns
Chip selection to output in low Z	t_{CLZ}	10	–	10	–	ns
Output enable to output in low Z	t_{OLZ}	5	–	5	–	ns
Chip deselection to output in high Z	t_{CHZ}	0	40	0	50	ns
Output disable to output in high Z	t_{OHZ}	0	40	0	50	ns

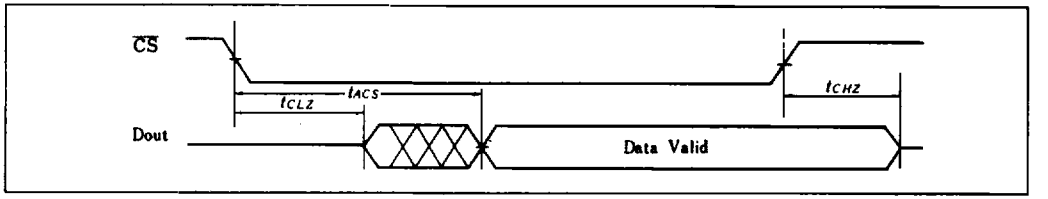
Read Cycle Timing No. 1 *1



Read Cycle Timing No. 2 *1, *2, *4



Read Cycle Timing No. 3 *1, *3, *4

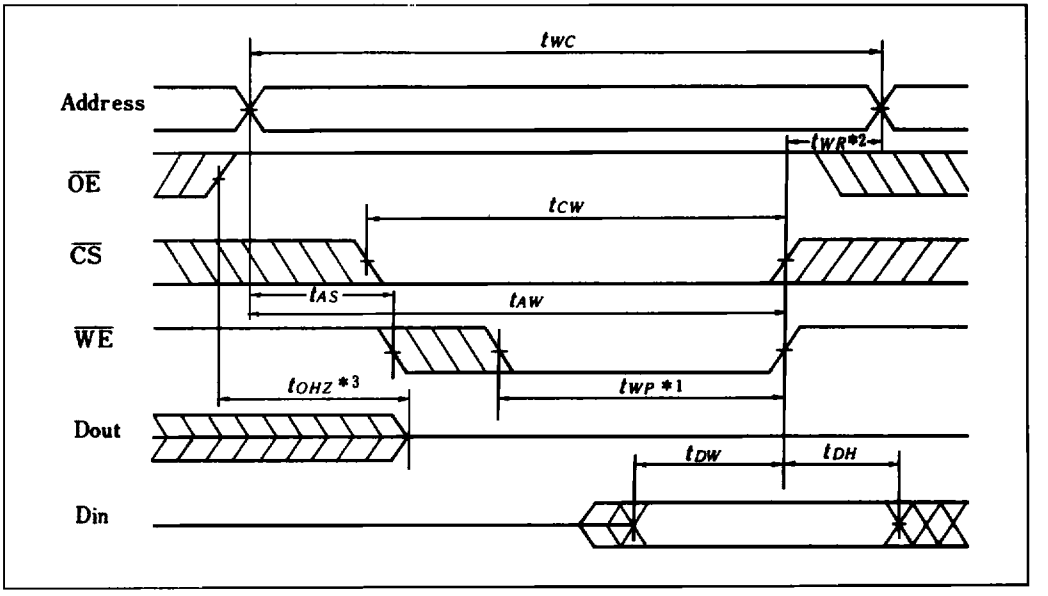


Notes) *1. $\overline{WE}$ is high for read cycle.
*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*3. Address should be valid prior to or coincident with $\overline{CS}$ transition low.
*4. $\overline{OE}$ = V_{IL}.

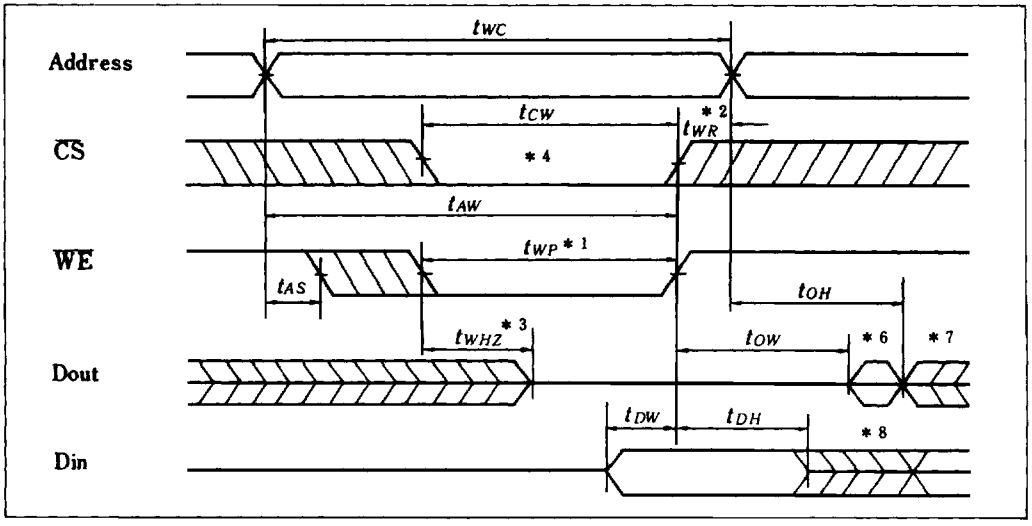
Write Cycle

Parameter	Symbol	HM66204-12		HM66204-15		Unit
		min	max	min	max	
Write cycle time	t_{WC}	120	–	150	–	ns
Chip selection to end of write	t_{CW}	100	–	120	–	ns
Address valid to end of write	t_{AW}	100	–	120	–	ns
Address setup time	t_{AS}	0	–	0	–	ns
Write pulse width	t_{WP}	90	–	110	–	ns
Write recovery time	t_{WR}	5	–	5	–	ns
Write to output in high Z	t_{WHZ}	0	40	0	50	ns
Data to write time overlap	t_{DW}	50	–	60	–	ns
Data hold from write time	t_{DH}	0	–	0	–	ns
Output disable to output in high Z	t_{OHZ}	0	40	0	50	ns
Output active from end of write	t_{OW}	5	–	5	–	ns

Write Cycle Timing No. 1 ($\overline{OE}$ Clock)



Write Cycle Timing No. 2*5 ($\overline{OE}$ Low Fixed)



Notes) *1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*3. During this period, I/O pins are in the output state.
The input signals out of phase must not be applied.
*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, output remain in a high impedance state.
*5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
*6. D_{out} should be held in phase of the written data during this write cycle.
*7. D_{out} is the read data of next address.
*8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. The input signals which are opposite to the output level should not be applied to I/O pins.

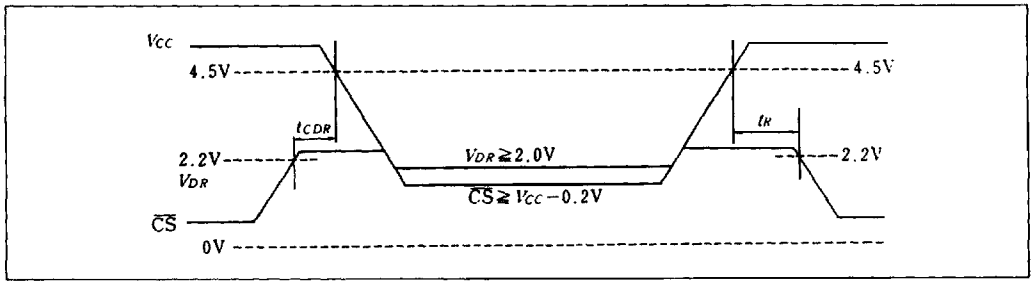
Low V_{CC} Data Retention Characteristics (Ta = 0°C to +70°C)

Data retention characteristics is guaranteed only for L version.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
V_{CC} for data retention	V_{DR}	2.0	–	–	V	$\overline{CS} \geq V_{CC}-0.2V$ A15, A16 $\geq V_{CC}-0.2V$ or A15, A16 $\leq 0.2V$
Data retention current	I_{CCDR}	–	–	200	μA	$V_{CC} = 3.0V$, $\overline{CS} \geq 2.8V$ A15, A16 $\geq 2.8V$ or A15, A16 $\leq 0.2V$
Chip deselect to data retention time	t_{CDR}	0	–	–	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*1	–	–	ns	

Note) *1. t_{RC} = Read Cycle Time.

Low V_{CC} Data Retention Waveform



Package Dimensions; Unit: mm (inch)