TLC32044, Single Channel Codec, 0.15 - 3.6 kHz Bandwidth

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	TLC32044
Resolution (Bits)	14
Sampling Rate (max) (kHz)	19.2
Bandwidth (kHz)	0.15 - 3.6
Number of Channels	1
Supply Voltage(s) (V)	-5
Pd (typ) (mW)	125

FEATURES

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- 14-Bit Dynamic Range ADC and DAC
- 2's Complement Format
- Variable ADC and DAC Sampling Rate Up to 19,200 Samples per Second
- Switched-Capacitor Antialiasing Input Filter and Output-Reconstruction Filter
- Serial Port for Direct Interface to TMS(SMJ)320C17, TMS(SMJ)32020, TMS(SMJ)320C25,and TMS320C30 Digital Signal Processors
- Synchronous or Asynchronous ADC and DAC Conversion Rates With Programmable Incremental ADC and DAC Conversion Timing Adjustments
- Serial Port Interface to SN74(54)299 Serial-to-Parallel Shift Register for Parallel Interface to TMS(SMJ)32010, TMS(SMJ)320C15, or Other Digital Processors
- Internal Reference for Normal Operation and External Purposes, or Can Be Overridden by External Reference
- CMOS Technology

DESCRIPTION

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The TLC32044 and TLC32045 are complete analog-to-digital and digital-to-analog input and output systems on single monolithic CMOS chips. The TLC32044 and TLC32045 integrate a bandpass switched-capacitor antialiasing input filter, a 14-bit-resolution A/D converter, four microprocessor-compatible serial port modes, a 14-bit-resolution D/A converter, and a low-pass switched-capacitor output-reconstruction filter. The devices offer numerous combinations of master clock input frequencies and conversion/sampling rates, which can be changed via digital processor control.

Typical applications for the TLC32044 and TLC32045 include speech encryption for digital transmission, speech recognition/ storage systems, speech synthesis, modems (7.2-, 8-, 9.6-, 14.4-, and 19.2-kHz sampling rate), analog interface for digital signal processors (DSPs), industrial process control, biomedical instrumentation, acoustical signal processing, spectral analysis, data acquisition, and instrumentation recorders. Four serial modes, which allow direct interface to the TMS(SMJ)320C17, TMS(SMJ)32020, TMS(SMJ)320C25, and TMS(SMJ)320C30 digital signal processors, are provided. Also, when the transmit and receive sections of the analog interface circuit (AIC) are operating synchronously, it will interface to two SN74(54)299 serial-to-parallel shift registers. These serial-to-parallel shift registers can then interface in parallel to the TMS(SMJ)32010, TMS(SMJ)320C15, and other digital signal processors, or external FIFO circuitry. Output data pulses are emitted to inform the processor that

data transmission is complete or to allow the DSP to differentiate between two transmitted bytes. A flexible control scheme is provided so that the functions of the TLC32044 or TLC32045 can be selected and adjusted coincidentally with signal processing via software control.

The antialiasing input filter comprises eighth-order and fourth-order CC-type (Chebyshev/elliptic transitional) low-pass and high-pass filters, respectively. The input filter is implemented in switched-capacitor technology and is preceded by a continuous time filter to eliminate any possibility of aliasing caused by sampled data filtering. When only low-pass filtering is desired, the high-pass filter can be switched out of the signal path. A selectable, auxiliary, differential analog input is provided for applications where more than one analog input is required.

The A/D and D/A architectures ensure no missing codes and monotonic operation. An internal voltage reference is provided to ease the design task and to provide complete control over the performance of the TLC32044 or TLC32045. The internal voltage reference is brought out to a terminal and is available to the designer. Separate analog and digital voltage supplies and grounds are provided to minimize noise and ensure a wide dynamic range. Also, the analog circuit path contains only differential circuitry to keep noise to an absolute minimum. The only exception is the DAC sample and hold, which utilizes pseudo-differential circuitry.

The output-reconstruction filter is an eighth-order CC-type (Chebyshev/elliptic transitional low-pass filter) followed by a second-order (sin x)/x correction filter and is implemented in switched-capacitor technology. This filter is followed by a continuous-time filter to eliminate images of the digitally encoded signal. The on-board (sin x)/x correction filter can be switched out of the signal path using digital signal processor control, if desired.

The TLC32044C and TLC32045C are characterized for operation from 0°C to 70°C. The TLC32044E is characterized for operation from -20°C to 85°C. The TLC32044I and TLC32045I are characterized for operation from -40°C to 85° C. The TLC32044M is characterized for operation from -55°C to 125°C.

TECHNICAL RESOURCES

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To view the following documents, Acrobat Reader 4.0 is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

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Full datasheet in Acrobat PDF: tlc32044.pdf (534 KB,Rev.F) (Updated: 05/01/1995)

APPLICATION NOTES

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- Amplifiers and Bits: An Introduction to Selecting Amplifiers for Data Converters (Rev. B) (SLOA035B - Updated: 12/18/2001)
- Understanding Data Converters (SLAA013 - Updated: 07/01/1995)

BLOCK DIAGRAMS

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Generic Web Access Device

PRICING/AVAILABILITY/PKG

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ORDERABLE DEVICE	PACKAGE	PINS	TEMP (°C)	STATUS	BUDGETARY PRICE US$/UNIT QTY=1000+	PACK QTY	DSCC NUMBER	PRICING/AVAILABILITY/PKG
TLC32044CFN	FN	28		NRND	9.42	37		Check stock or order
TLC32044CFNR	FN	28		NRND	9.45	750		Check stock or order
TLC32044CN	N	28		NRND	9.42	13		Check stock or order
TLC32044EFN	FN	28		NRND	9.42	37		Check stock or order
TLC32044IFK	FK	28		ACTIVE	23.24	1		Check stock or order
TLC32044IFK-T	FK	28		ACTIVE	30.43	1		Check stock or order
TLC32044IN	N	28		NRND	9.42	13		Check stock or order

TLC32044MFKB	FK	28	-55 TO 125	ACTIVE	64.06	1		Check stock or order
TLC32044MJ	J	28	-55 TO 125	ACTIVE	54.45	1		Check stock or order
TLC32044MJB	J	28	-55 TO 125	ACTIVE	64.06	1		Check stock or order

Table Data Updated on: 4/14/2002
