FPGA Advantage Tutorial

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Table of Contents

FPGA Advantage Tutorial 5

Invoking FPGA Advantage 6
The Design Manager 8
Set the Default Language 9
Import the Fibonacci Design 10
Browse the Fibonacci Design 12
Use ModelSim to Debug the Design 14
Create a Graphical Test Bench 16
Save the Test Bench 19
Set the Default View 20
Simulate Your Design 22
Add Probes to the Test Bench 24
Add a Breakpoint 25
Add Signals to the Wave Window 26
Run the Simulator 26
Synthesize the Design 27
Running the LeonardoSpectrum Flow 28
View the LeonardoSpectrum RTL Schematic 30
Running the Precision Synthesis Flow 31
View the Precision Synthesis RTL Schematic 32
About Gate Level Simulation 33
Further Information 34

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FPGA Advantage Tutorial

This tutorial uses a simple HDL text design which implements a simple Fibonacci count sequence which repeatedly sums the previous two numbers: 0, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89 to 144.

Invoking FPGA Advantage **6**

Set the Default Language **9**

Import the Fibonacci Design **10**

Browse the Fibonacci Design 12

Use ModelSim to Debug the Design **14**

Create a Graphical Test Bench **16**

Save the Test Bench 19

Simulate Your Design **21**

Add Probes to the Test Bench 23

Add a Breakpoint 24

Add Signals to the Wave Window 25

Run the Simulator 25

Synthesize the Design **26**

Running the LeonardoSpectrum Flow 27

View the LeonardoSpectrum RTL Schematic 29

Running the Precision Synthesis Flow 30

View the Precision Synthesis RTL Schematic 31

About Gate Level Simulation **32**

Further Information **33**

Invoking FPGA Advantage

You can invoke FPGA Advantage on a Windows workstation by double-clicking the shortcut which was created by the install program on your desktop. Alternatively, you can choose the corresponding shortcut from the **FPGA Advantage** cascade of the **Programs** menu.

Configuration	Shortcut
FPGA Advantage with LeonardoSpectrum	FPGAdv with LS
FPGA Advantage with Precision Synthesis	FPGAdv with PS
FPGA Advantage with LeonardoSpectrum and Precision Synthesis	FPGAdv with LS & PS
FPGA Advantage with Precision Physical Synthesis	FPGAdv with PP
FPGA Advantage Personal with LeonardoSpectrum	FPGAdv Personal with LS
FPGA Advantage Personal with Precision Synthesis	FPGAdv Personal with PS
FPGA Advantage Personal with LeonardoSpectrum and Precision Synthesis	FPGAdv Personal with LS & PS
FPGA Advantage Personal Simulation with LeonardoSpectrum and Precision Synthesis	FPGAdv Personal Simulation with LS & PS

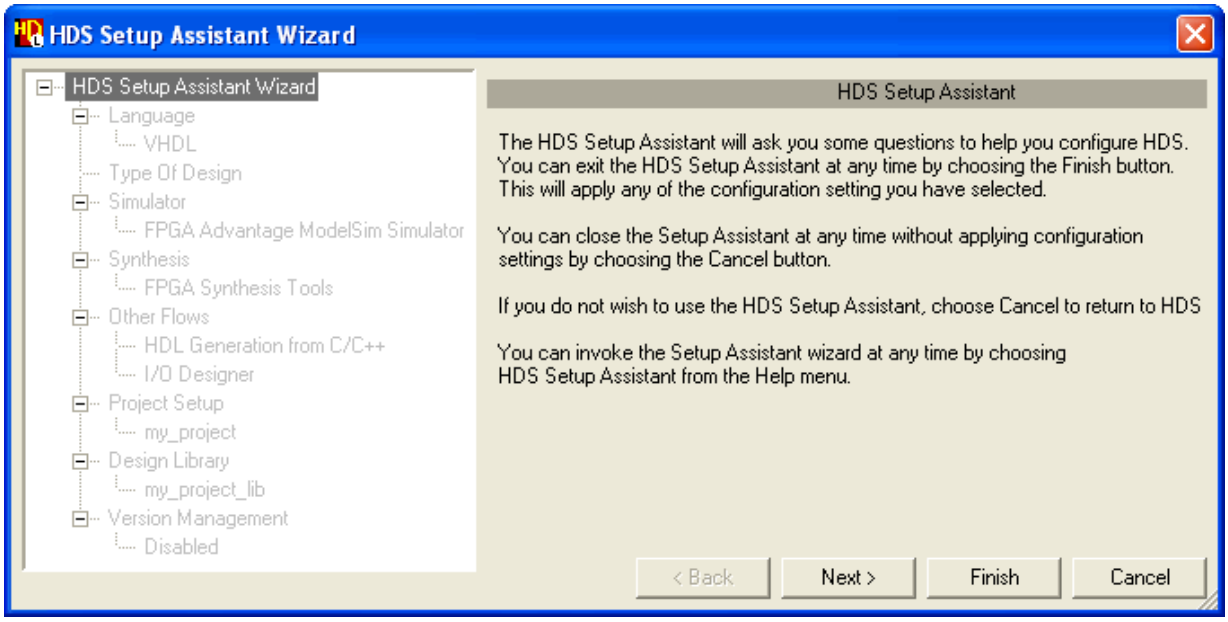
You can invoke FPGA Advantage on a UNIX or Linux workstation by using a script which was created by the install program in the following installation subdirectory:

<install_dir>/Fpgadv/bin

Configuration	Scripts
FPGA Advantage with LeonardoSpectrum	fa_with_ls
FPGA Advantage with Precision Synthesis	fa_with_ps
FPGA Advantage with LeonardoSpectrum and Precision Synthesis	fa_with_ls fa_with_ps
FPGA Advantage with Precision Physical Synthesis	fa_with_pp
FPGA Advantage with ModelSim LE	fa_with_le

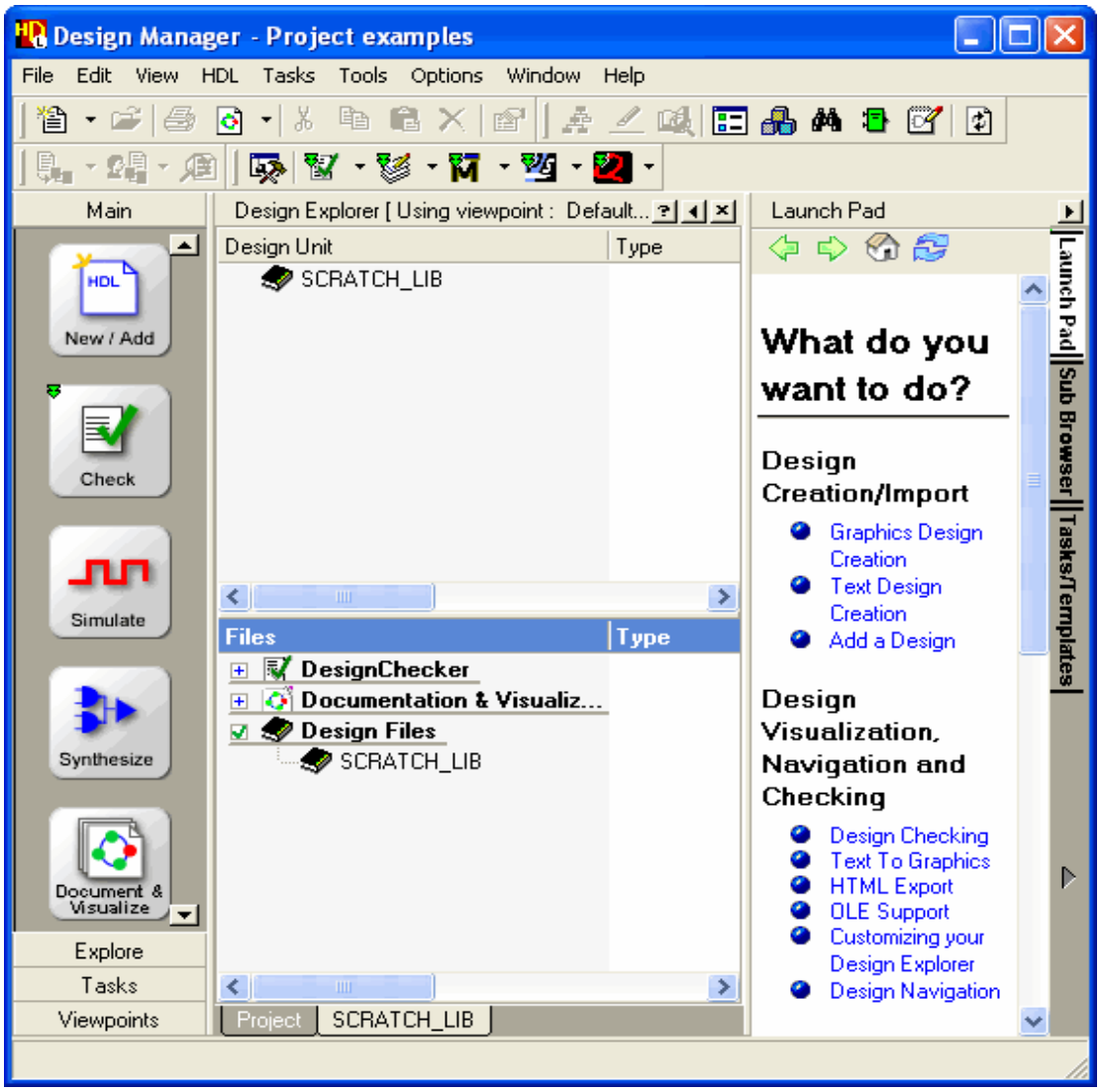
1. Invoke FPGA Advantage using the shortcut (on Windows) or invoke script (on UNIX or Linux) listed in the tables on the previous page. If this is the first time you invoke FPGA Advantage, the HDS Setup Assistant wizard is started.
2. Choose to cancel the wizard. HDS starts with the default examples project, VHDL as the default language and all the available flows and tools.

You can invoke the wizard at any time by choosing **HDS Setup Assistant** from the **Help** menu in the Design Manager window.



The Design Manager

The design manager displays the default *SCRATCH_LIB* library. The *SCRATCH_LIB* library is created in a default location defined in the *examples.hdp* project. On Windows, this is beneath the FPGA Advantage installation tree; on UNIX it is in your home directory.



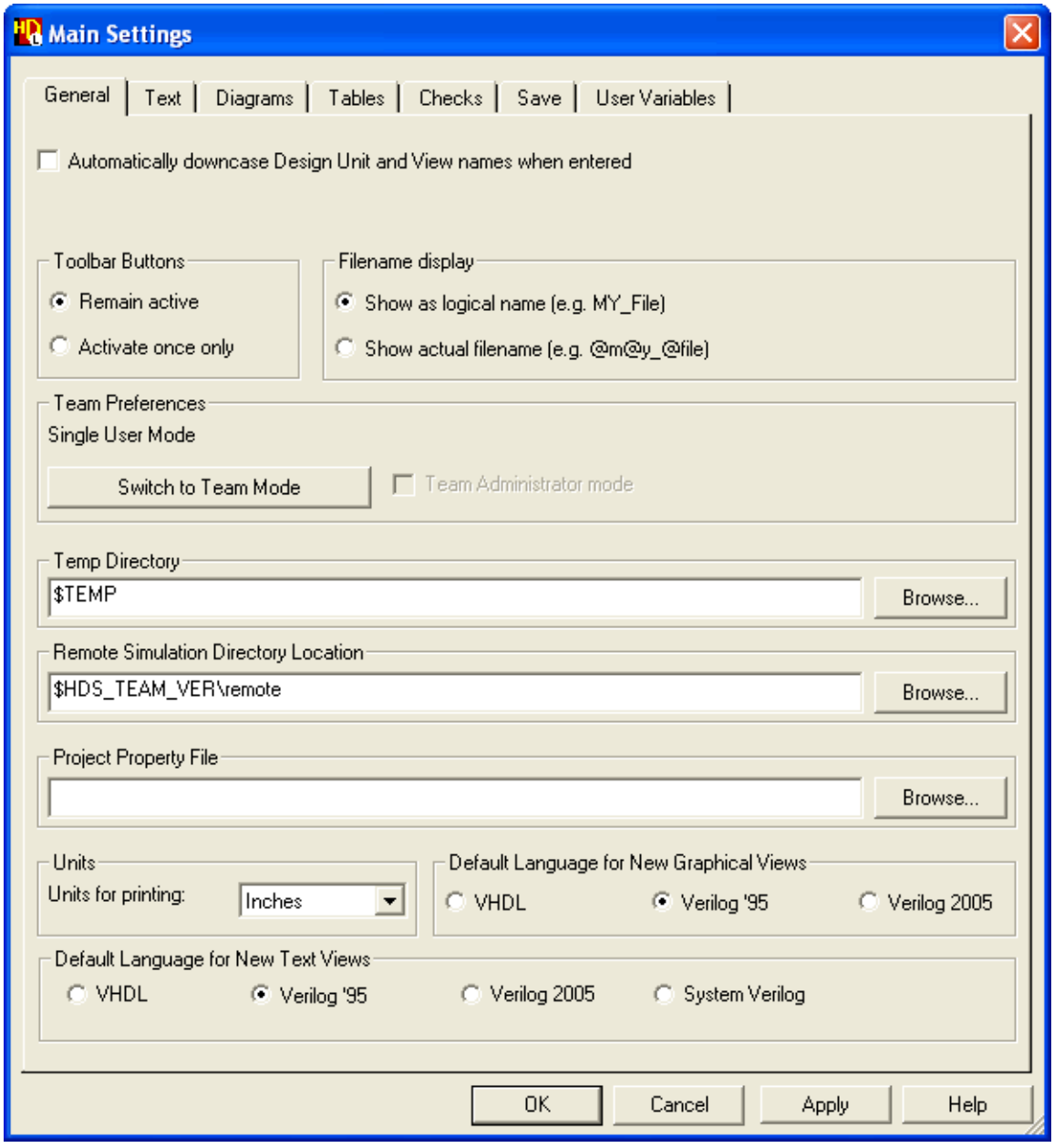
Note

Note that an object tip containing information about the object under the cursor is displayed when you move the cursor over each object in the window.
You can display help about the design manager (including a hyperlink to the section in the *HDL Designer Series User Manual*) by clicking on the icon.

The procedures in this tutorial use the *SCRATCH_LIB* library although you can use any other empty writable library.

Set the Default Language

1. Choose **Main** from the **Options** menu to display the Main Settings dialog box. Select **Verilog 95** as the default language for all new graphical and text views. Click the **Apply** button to confirm your language choice and then click the **OK** button to close the dialog box.



Note

The FPGA Advantage tutorial can be completed using either the Verilog or VHDL languages. Verilog has been used for the examples shown in this manual.

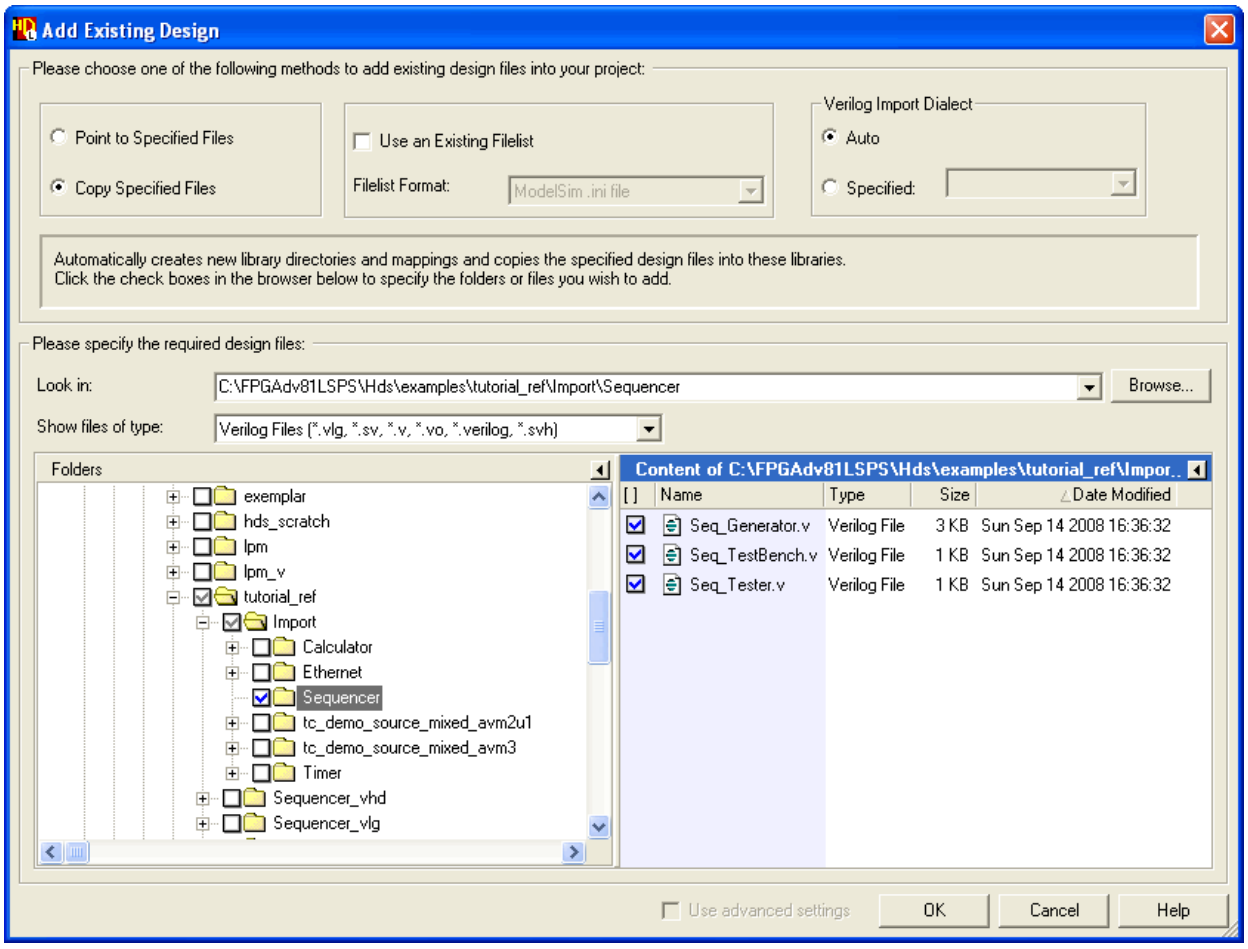
Import the Fibonacci Design

This tutorial uses a Fibonacci sequencer design example which can be imported as either VHDL or Verilog code.

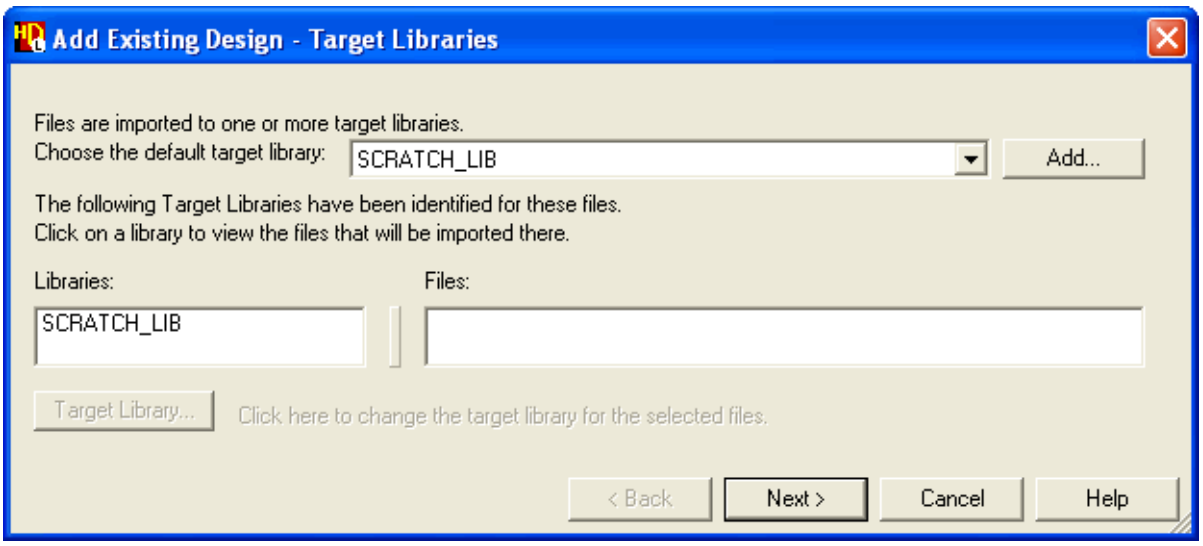
1. Choose **File> Add> Existing Design**.
2. Specify the method to add your design by selecting the *Copy Specified Files* option.
3. In the *Folders* pane, browse to the Fibonacci sequencer source code in the *examples* sub-directory of your FPGA Advantage installation. For example, if FPGA Advantage has been installed in the directory *C:\FPGAdv81LSPS*, the path to locate the tutorial source files would be:

   C:\FPGAdv81LSPS\Hds\examples\tutorial_ref\Import\Sequencer

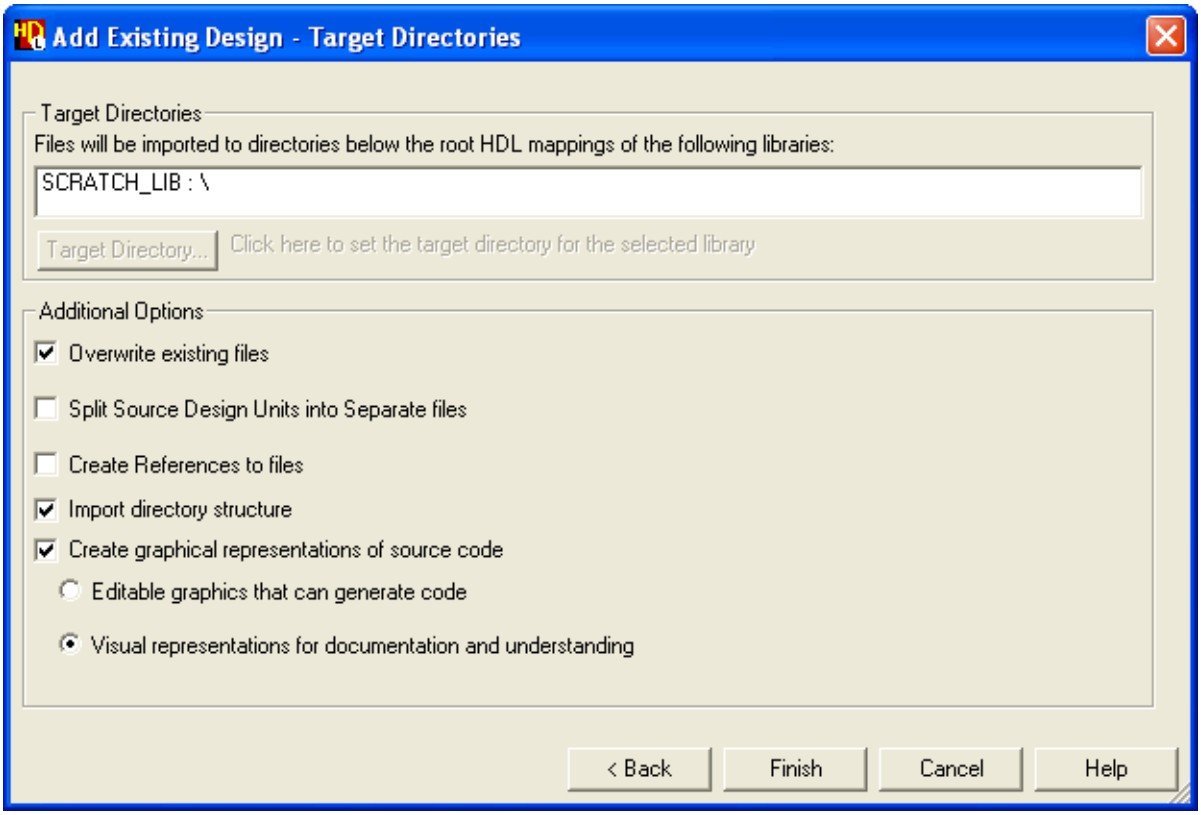
4. From the *Show files of type* list box select *Verilog Files*.



Click the **OK** button to display the **Target Libraries** page of the **Add Existing Design** wizard. The Target Libraries page shows the *SCRATCH_LIB* library as the default target library.



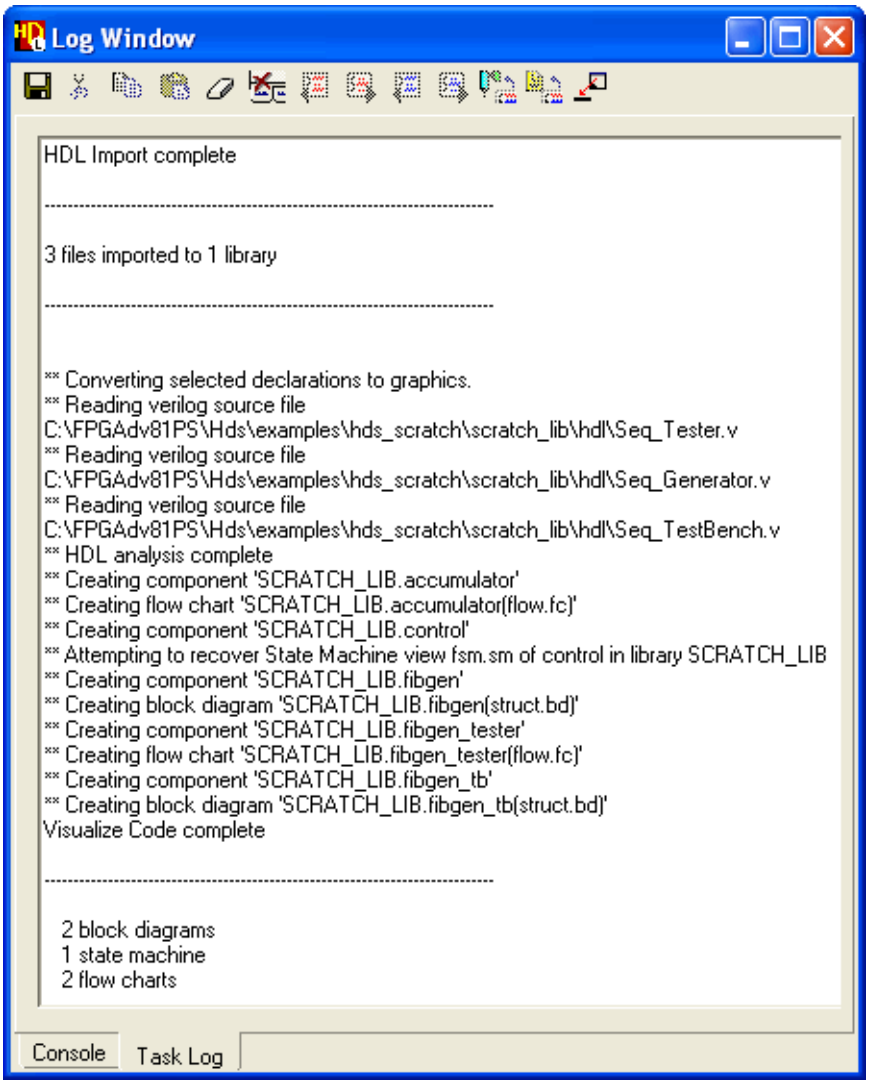
5. Click the **Next** button to display the **Target Directories** page showing where the imported files will appear below the root HDL mapping:



6. Select *Create graphical representations of source code* and click the **Finish** button.

By choosing to create visual representations of your source code you thereby create graphical views that allow only non-logical edits. These views are tightly coupled to their source code and can be used for understanding and documenting your textual designs.

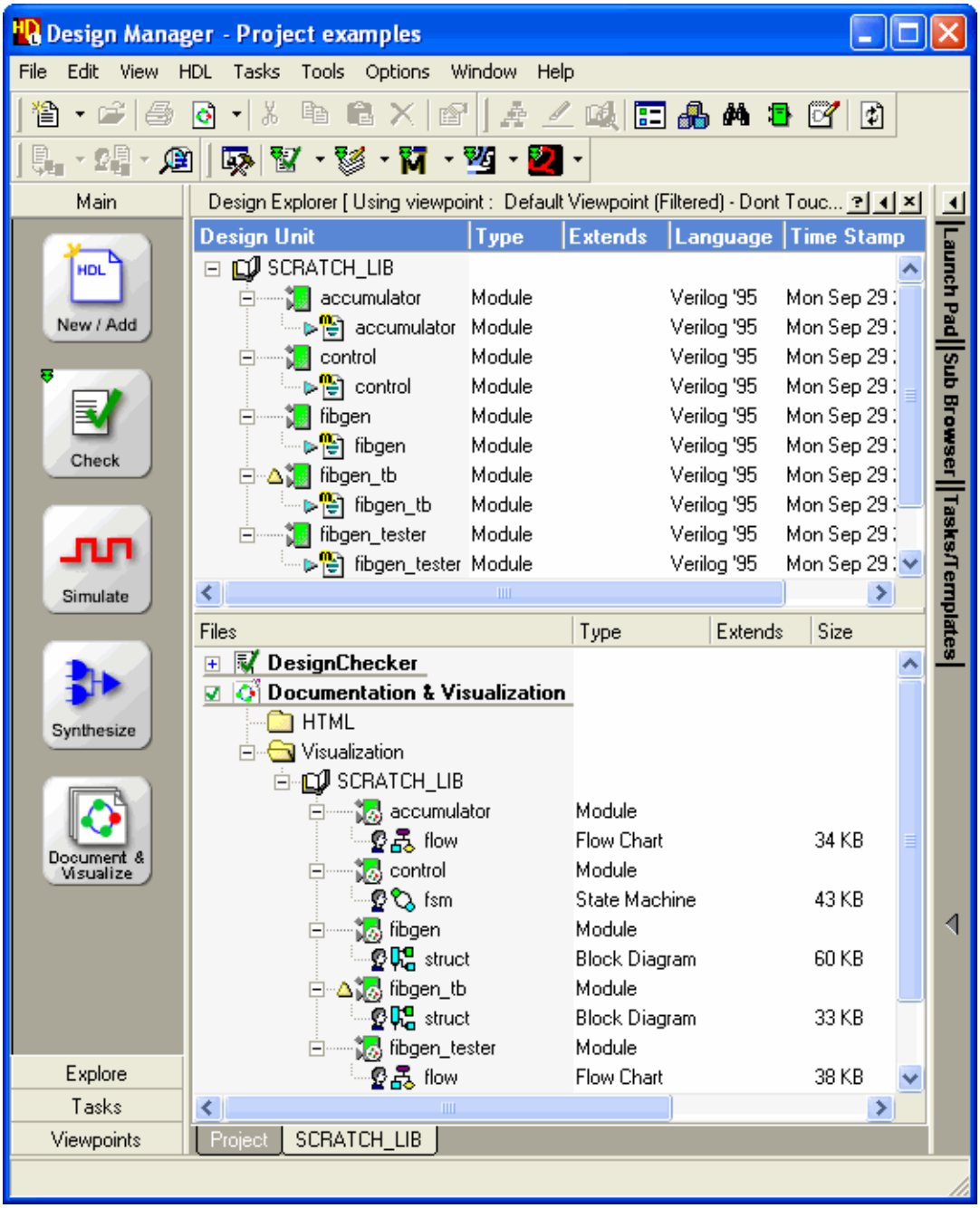
The **HDL Log Window** reports that the HDL import has been completed, three files have been imported to one library and 2 block diagrams, 1 state machine and 2 flow charts have been created.



Browse the Fibonacci Design

1. Select the *SCRATCH_LIB* library in the Design Unit's pane of the Design Manager. Click the right mouse button and choose **Expand All** from the popup menu.

The design units for the Fibonacci design should now be displayed in the Design Unit's pane while the visualization views should be displayed in the Files' pane. The following picture shows the imported verilog design:



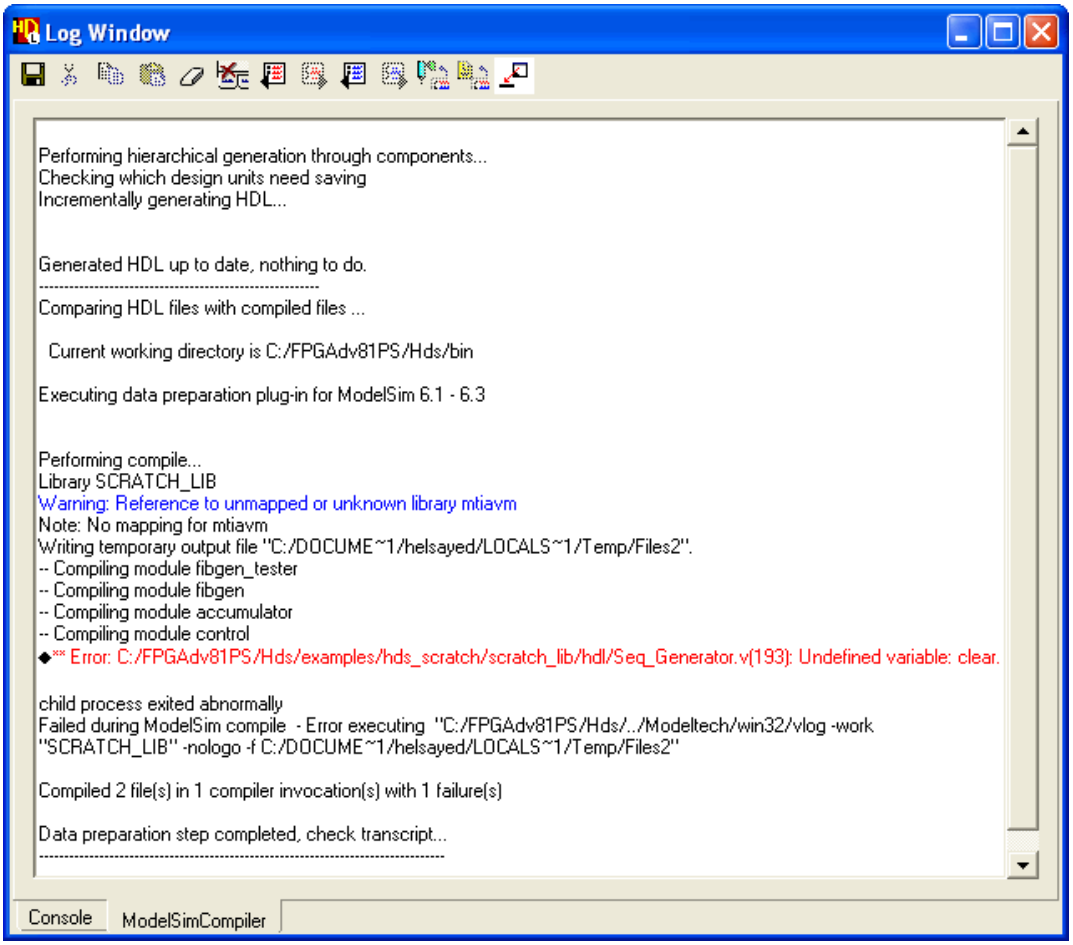
Each Verilog module or VHDL entity in the source HDL code is partitioned into a separate design unit which also includes the corresponding VHDL architectures if you are using VHDL. Notice that a △ icon is displayed adjacent to the *fibgen_tb* design unit in the *Design Units* pane indicating that this test bench component is the top level design unit.

Use ModelSim to Debug the Design

1. Select the component design unit icon for *fibgen_tb* in the design manager.
2. Click the **Model*Sim* Flow** button in the design manager toolbar.

   FPGA Advantage attempts to run the Model*Sim* flow but HDL compilation fails due to deliberate errors in the design example source code.

   The compilation status is displayed in the **Log Window**:



   There is one error message (shown above) if you are using Verilog or five errors if you are using VHDL:

   ** Error: /user/frodo/hds_scratch/scratch_lib/hdl/Seq_Generator.vhd(87): Illegal target for signal assignment.

   ** Error: /user/frodo/hds_scratch/scratch_lib/hdl/Seq_Generator.vhd(87): Unknown identifier 'clear'.

   ** Error: /user/frodo/hds_scratch/scratch_lib/hdl/Seq_Generator.vhd(92): Illegal target for signal assignment.

   ** Error: /user/frodo/hds_scratch/scratch_lib/hdl/Seq_Generator.vhd(92): Unknown identifier 'clear'.

   ** Error: /user/frodo/hds_scratch/scratch_lib/hdl/Seq_Generator.vhd(107): VHDL Compiler exiting

These errors are caused by an inconsistent signal declaration between the body of the HDL text description and its interface. You can cross-reference from the error message in the log window to the incorrect declaration in the source HDL by using the Cross reference to graphics button or by double-clicking on the message.

3. Double-click on the error message in the log window.

   The DesignPad editor is invoked and the first line of HDL code that corresponds to an error message is highlighted.

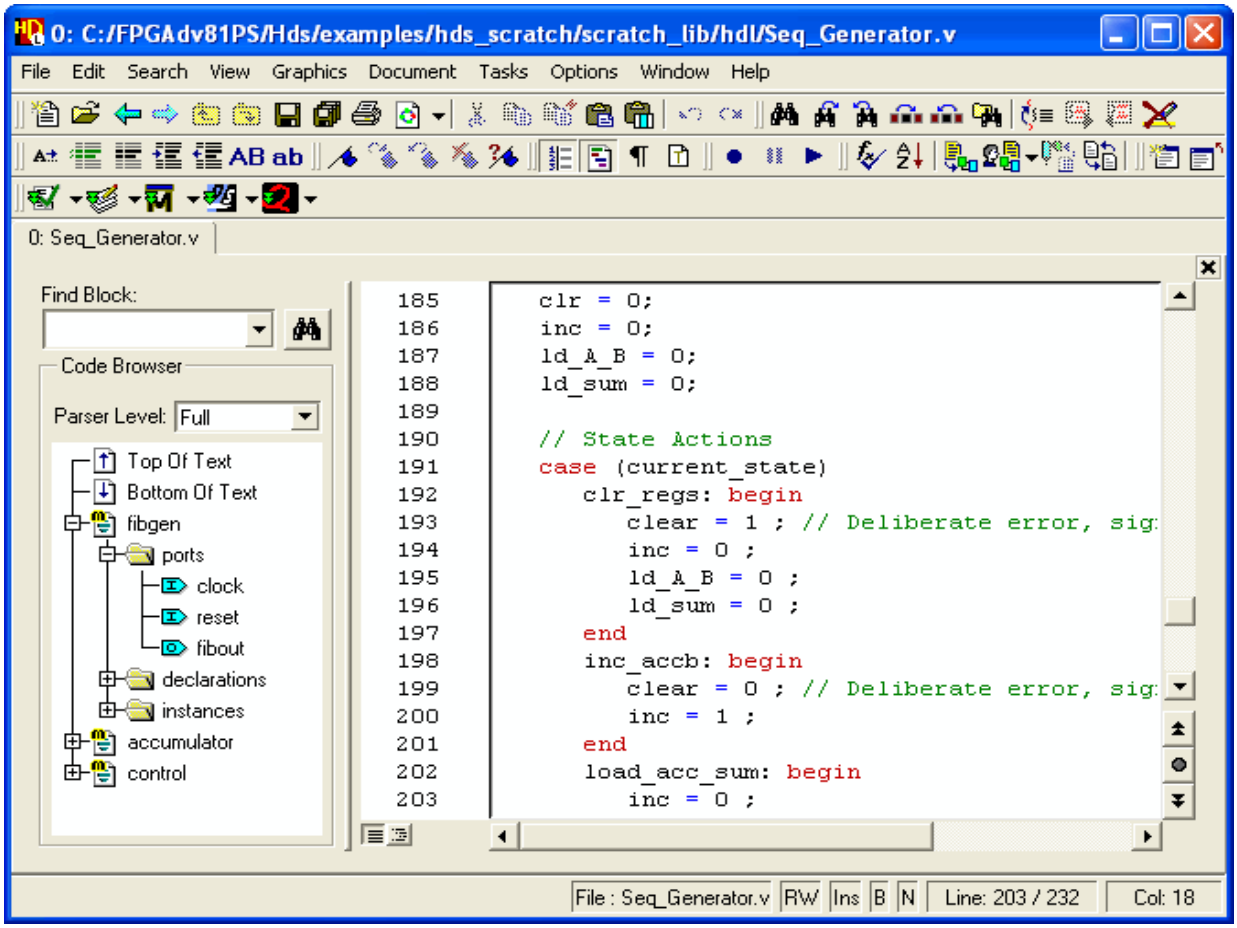
   Notice that the code includes two deliberate errors. If you are using Verilog, these are on lines 193 and 199:

```
193 clear = 1 ; // Deliberate error, signal is declared as clr
199 clear = 0 ; // Deliberate error, signal is declared as clr
```

   If you are using VHDL, the errors are on lines 87 and 92:

```
87 clear <= '1' ; // Deliberate error, signal is declared as clr
92 clear <= '0' ; // Deliberate error, signal is declared as clr
```

   The following picture shows the Verilog code:

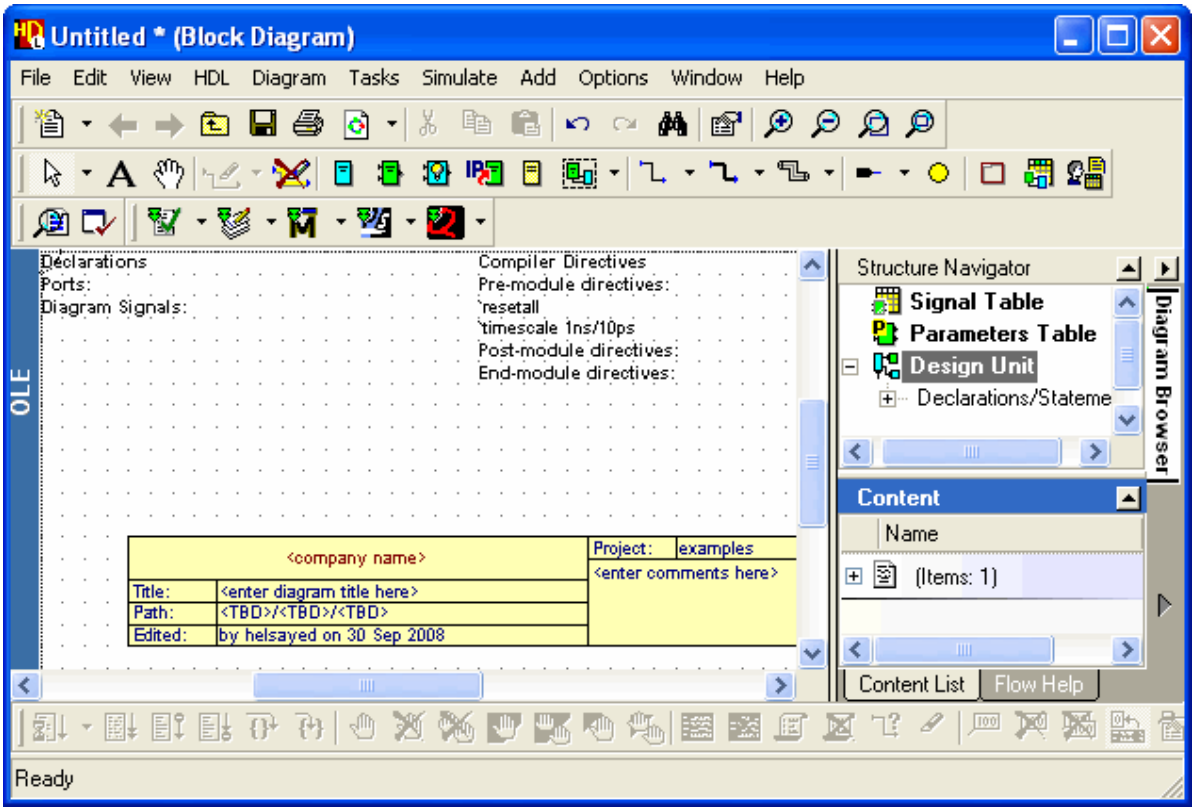


4. Correct the errors by replacing the word *clear* with *clr* and delete all of the comment text after the semi-colon.
5. Click the **Save** button on the DesignPad toolbar to save the edits to the file.
6. Close the text editor by choosing **Close Window** from the DesignPad **Window** menu or by using the keyboard shortcut **Ctrl + F4**.

Create a Graphical Test Bench

Now that you have corrected the errors in the source code, you could use the HDL text view of *fibgen_tb* to simulate your design. However, for this tutorial you will create a graphical test bench which will be used to control and monitor the simulation.

1. Use the **New** button in the design manager window and select **Block Diagram** from the **Graphical View** cascade of the dropdown menu to create a new untitled block diagram.

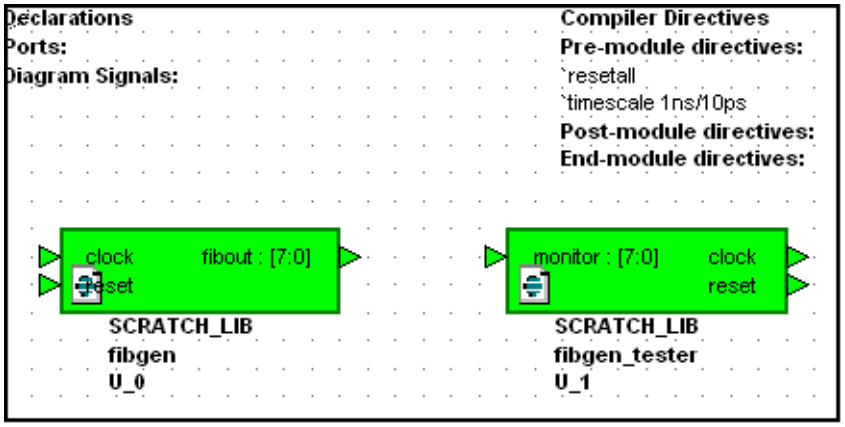


Notice the five toolbars at the top of the diagram. The toolbar buttons provide quick access to many of the most frequently used editing and formatting commands.

2. Click the **Add Component** button on the block diagram toolbar to display the **Component Browser** showing the *SCRATCH_LIB* library:

3. Select the *fibgen* component in the **Component Browser**, hold down the left mouse button and drag the component onto the block diagram.

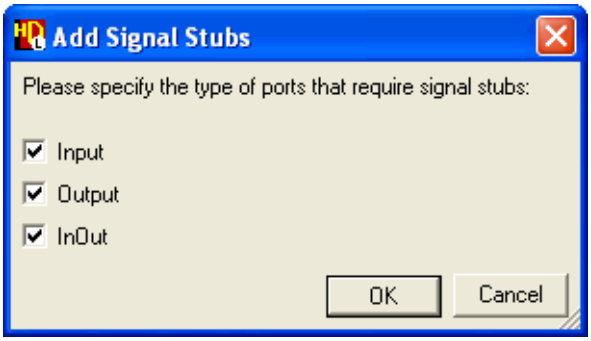
4. Repeat this procedure for the *fibgen_tester* component. The diagram should look similar to the picture shown below:



5. Close the **Component Browser**.

6. Select the *fibgen* component instance and use the right mouse button to choose **Add Signal Stubs** from the popup menu.

The **Add Signal Stubs** dialog box is displayed prompting you to choose the type of ports that require signal stubs:

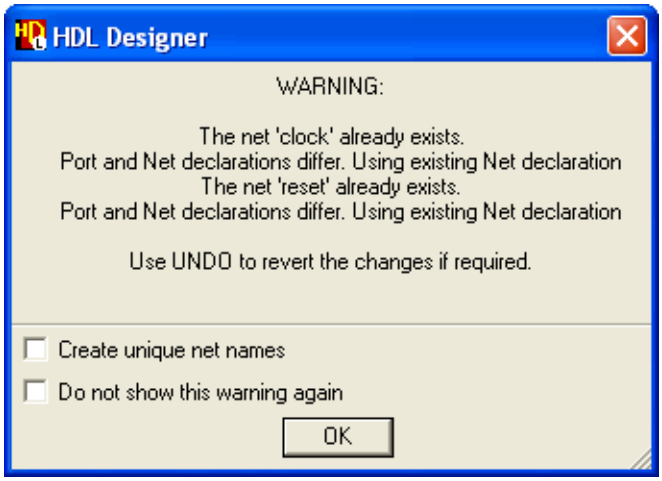


Note

The dialog box includes an additional *Buffer* option if you are using VHDL.

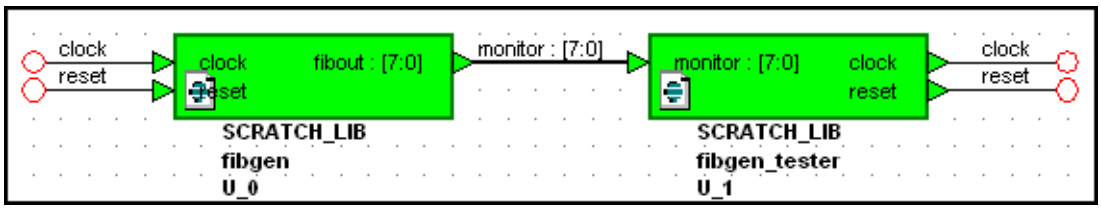
7. Click **OK** to accept the default settings and notice that two signals, *clock* and *reset* plus a bus named *fibout* are added to the ports on the *fibgen* instance.
8. Repeat this procedure for the *fibgen_tester* component.

   You are warned that the nets *clock* and *reset* already exist on the diagram and (if you are using Verilog) that their port and net declarations are different. These warning messages can be ignored.



9. Click **OK** to acknowledge the warning messages.
10. Notice that *clock* and *reset* signals plus a bus named *monitor* are added to the ports on the *fibgen_tester* instance.
11. Select and delete the bus *fibout*.
12. Select the connector on the *monitor* bus and drag it to connect on the *fibout* port of the *fibgen* instance.

The block diagram should look similar to the picture shown below:

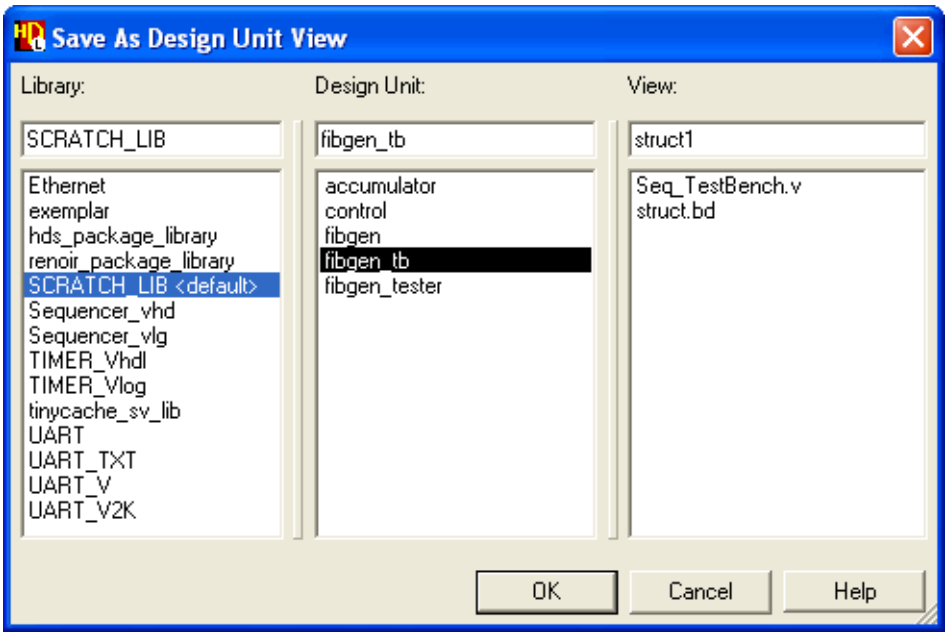


Note

It is not necessary to explicitly connect the *clock* and *reset* signals between each port on the *fibgen* and *fibgen_tester* components because these are implicitly connected by name.

Save the Test Bench

1. Use the **Save** button to save the test bench.
2. The **Save As Design Unit View** dialog box is displayed which allows you to save a design unit into any currently mapped library. The *SCRATCH_LIB* library is selected by default.
3. Select the existing design unit name *fibgen_tb* (which contains the original HDL text view of the test bench) and use the name *struct1*:



4. Click **OK** to save the block diagram as an alternative graphical view of the test bench.

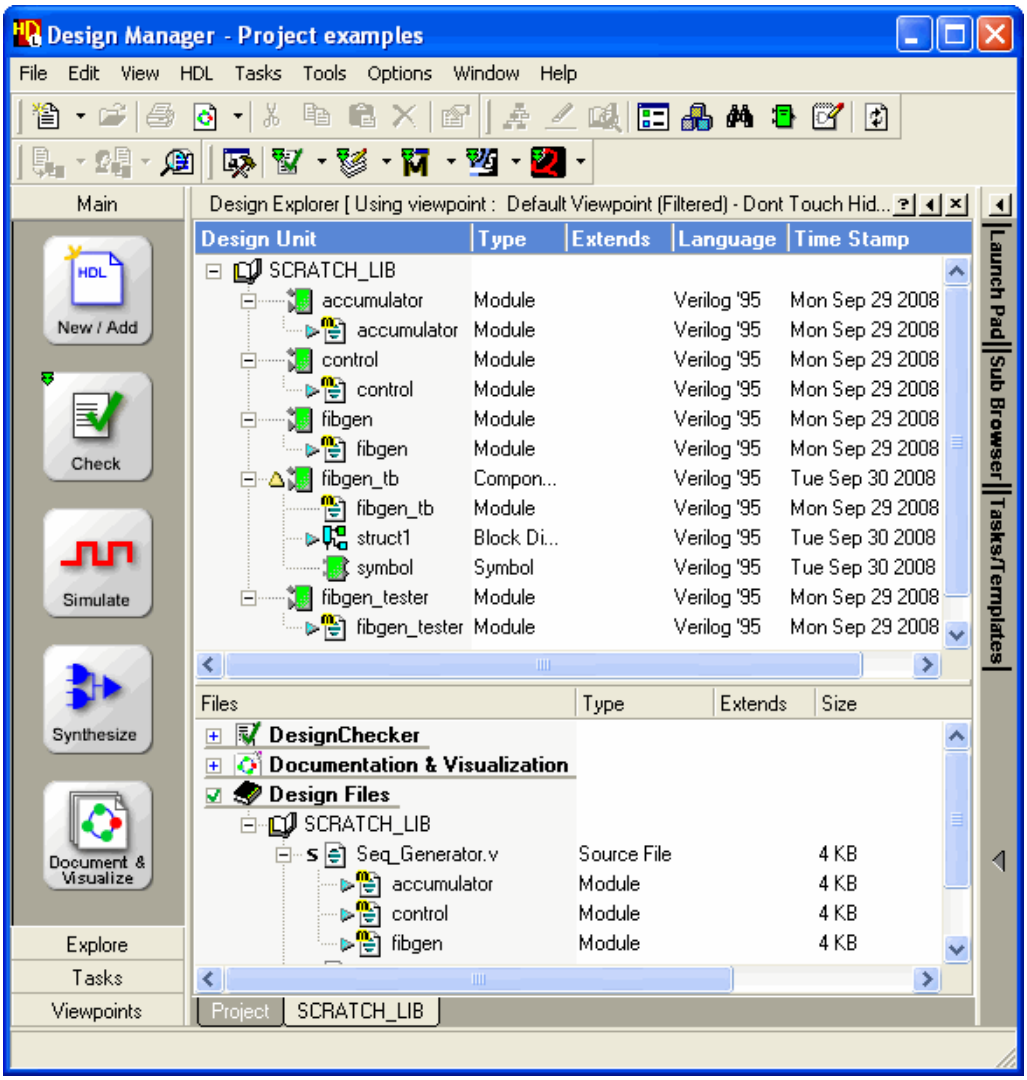
Set the Default View

Notice that the *struct1* block diagram and a graphical *symbol* view are added to the *fibgen_tb* design unit shown in the design explorer.

1. Select the *struct1* view below *fibgen_tb* in the design explorer, right click and choose **Set Default View** from the popup menu.

   This sets the graphical test bench view *struct1* as the default view. An ▶ icon next to *struct1* indicates that it is now the default view.

   For example, the following picture shows the Verilog version of the design after you have set the default view:

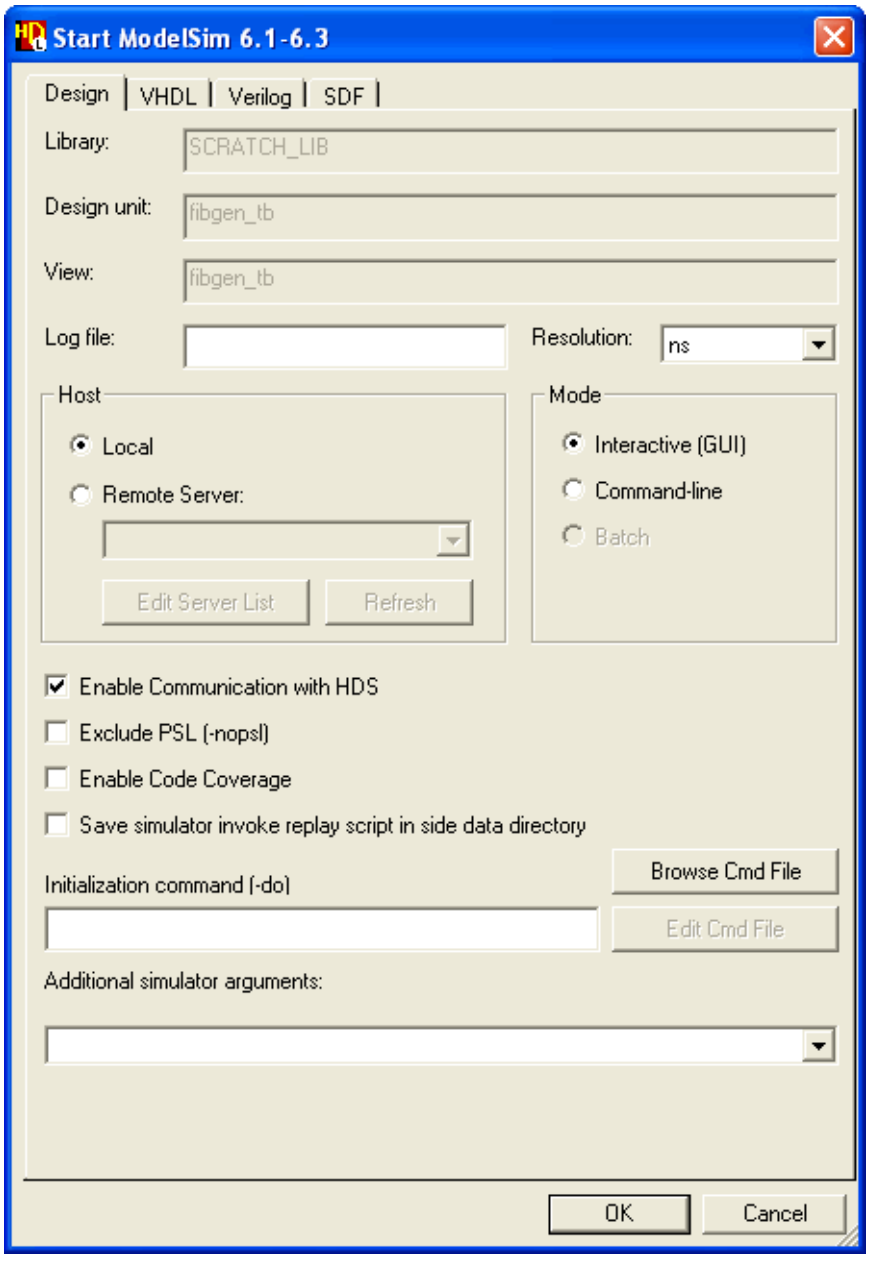


This graphical test bench will be used to control and monitor the simulation as described in the next section.

Simulate Your Design

1. Select the *fibgen_tb* component and use the **ModelSim Flow** button to run the Model*Sim* flow.

   The **Start Model*Sim*** dialog box is displayed:



2. Ensure that the **Enable Communication with HDS** option is set and click the **OK** button to confirm the dialog box.

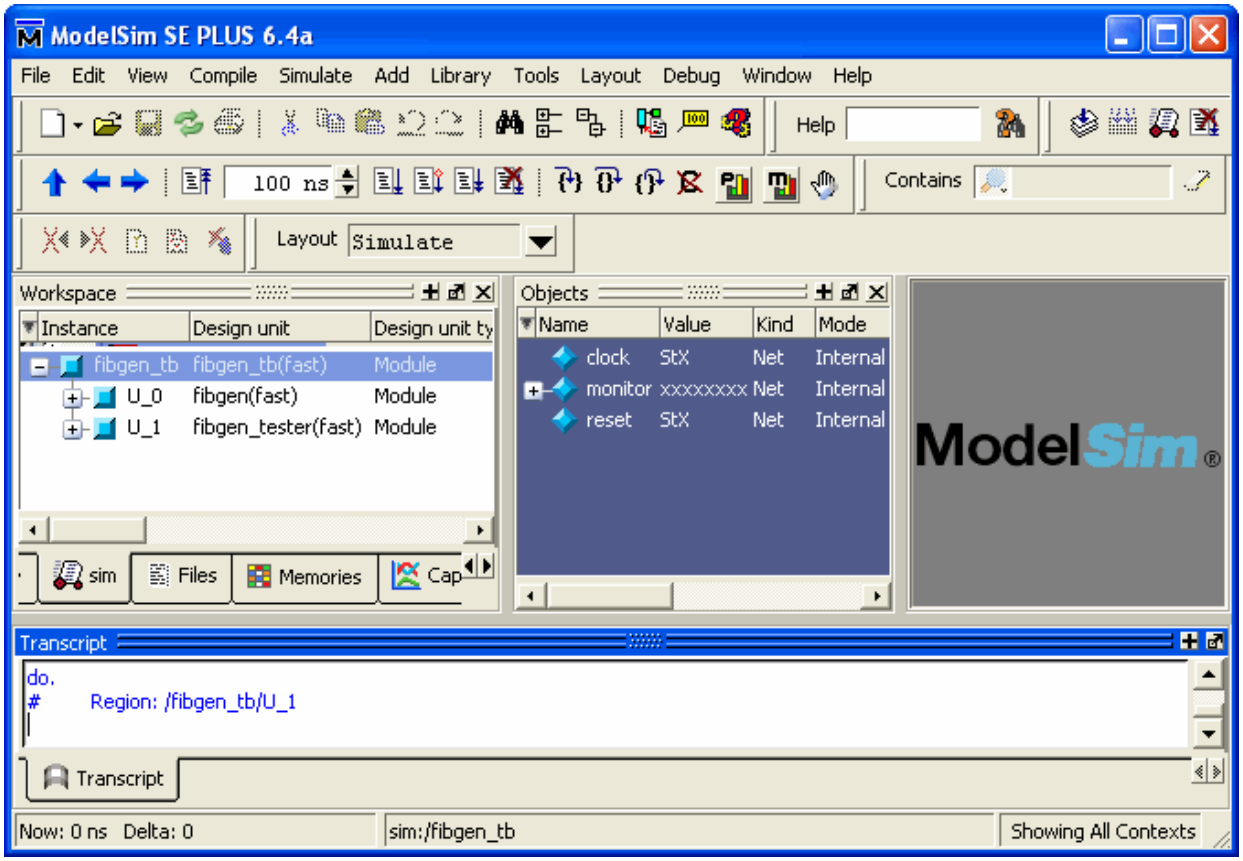
   The flow automatically generates HDL for the graphical test bench and compiles HDL for the hierarchy below the selected design unit.

Note

Messages showing the progress of HDL generation and compilation are displayed in the HDS Log Window. You can cross-reference from the log window to the source graphics or HDL if any generation or compilation errors are detected.

If generation and compilation are completed successfully, the Model*Sim* simulator is invoked and the compiled design is loaded.

The following example shows the ModelSim window when a Verilog version of the tutorial design has been successfully loaded:



Note

A number of warning messages are displayed in the ModelSim window when a Verilog version of the design is loaded. For example:
Module 'fibgen' does not have a `timescale directive in effect, but previous modules do.
These messages are issued because there is a `*timescale* directive in the HDL generated from the graphical test bench but there are no similar directives in the other HDL text views. These messages can be ignored for this tutorial.

Add Probes to the Test Bench

1. Make the *fibgen_tb* block diagram active.

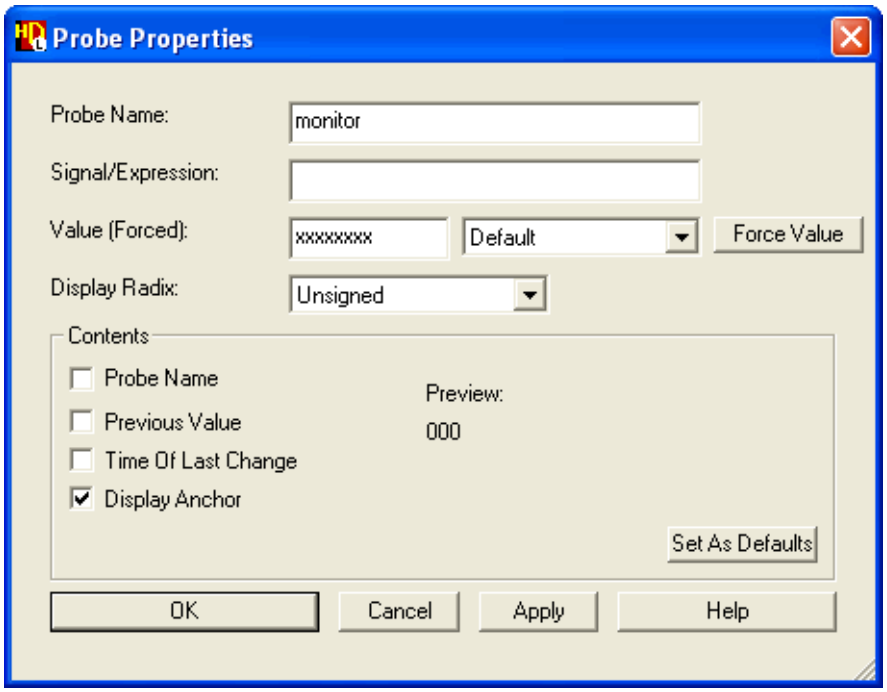
   Notice that an additional simulation toolbar is displayed at the bottom of the block diagram when the simulator is invoked. This toolbar provides commands that can be used to control the simulation of the design from the graphical view.

2. Use **Shift + Left Mouse Button** to select the *clock* and *reset* signals and the *monitor* bus of the fibgen component.

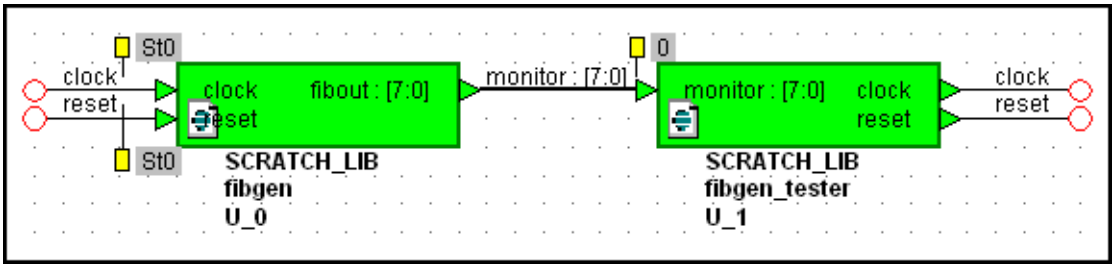
3. Click the **Add Probe** button in the simulation toolbar to add probes on the diagram which show the current value of each signal.

4. Select the probe on the *monitor* signal and use the right mouse button to choose **Probe Properties** from the popup menu. The **Probe Properties** dialog box is displayed.

5. Choose *Unsigned* from the dropdown list for the *Display Radix* and confirm the dialog box.



The block diagram should look similar to the following picture:

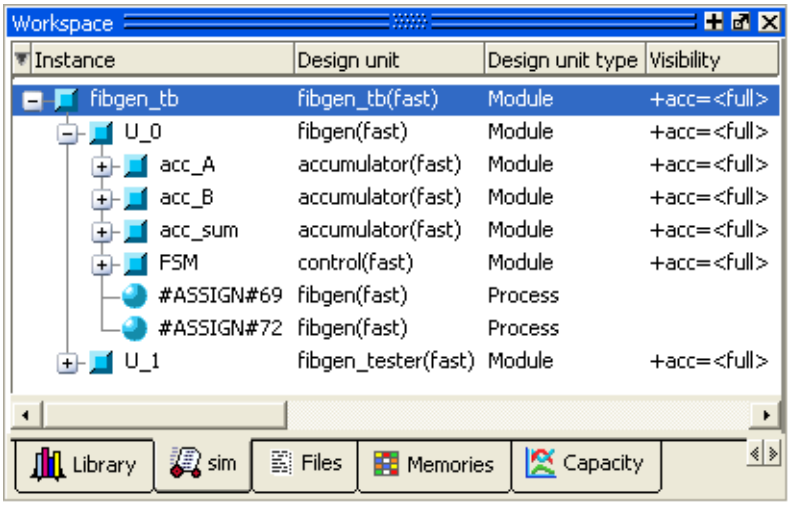


Note

Note that you can drag the probes to improve clarity on the diagram. The corresponding signal or bus is shown by an anchor line (which can be optionally displayed or hidden by setting an option in the Probe Properties dialog box).

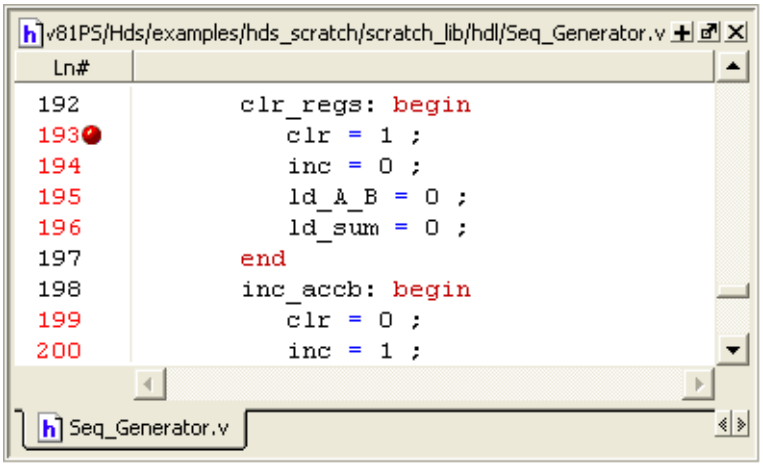
Add a Breakpoint

1. Use the ⊞ icons to expand the hierarchy of the *fibgen_tb* design in the **sim** structure tab of the Model*Sim* workspace window. Select the *FSM* view under the *U_O* instance if you are using Verilog (or the *fsm* view under the *i0* instance if you are using VHDL).



2. Display the Model*Sim* source window (by double clicking on the FSM control design unit in the sim structure tab of the ModelSim workspace or choose **Source** from the **View** cascade of the **Simulate** menu in the *fibgen_tb* test bench block diagram).

3. Navigate to line 193 if you are using Verilog (or line 87 if you are using VHDL) and set a breakpoint for the *clr = 1* (or *clr <= '1'*) assignment by clicking once beside the line number. A red dot is added after the line number indicating that a breakpoint has been set.



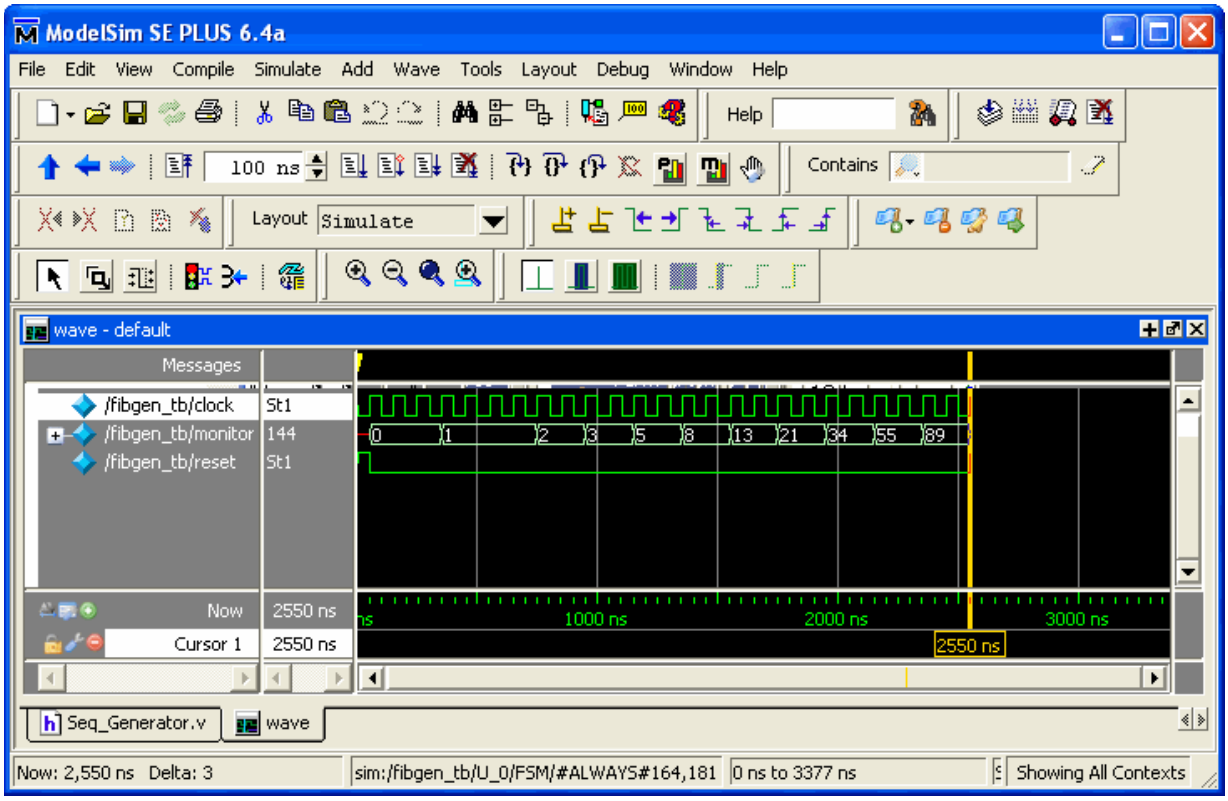
Add Signals to the Wave Window

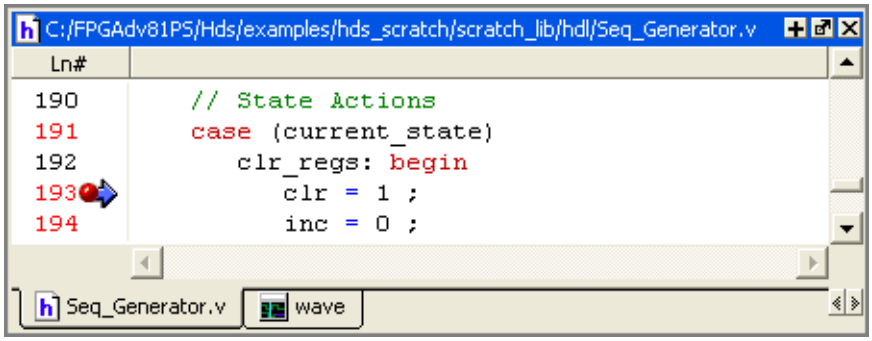
1. Make the *fibgen_tb* block diagram active and ensure that the *monitor* bus and the signals *clock* and *reset* are selected.
2. Click the **Add Wave** button to automatically open the Model*Sim* Wave window with the selected signals displayed.
3. Select the *fibgen_tb/monitor* bus in the Wave window and use the right mouse button to choose **Unsigned** from the **Radix** cascade of the popup menu.

Run the Simulator

1. Arrange the test bench block diagram, source and wave windows so that they are all visible.
2. In the *fibgen_tb* block diagram view, choose **run 200** from the popup menu of the **Run For Time** button to advance the simulation by 200 nanoseconds.

   Notice that the simulation probes on the test bench block diagram change color from yellow to red as their signal values are initialized.
3. Click the **Run Forever** button to run the simulator until the breakpoint is encountered. Notice that the waveform updates through the Fibonacci sequence 0, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89 and 144 as the simulation advances and that a blue arrow appears after the line number in the *Seq_Generator.v* source window.

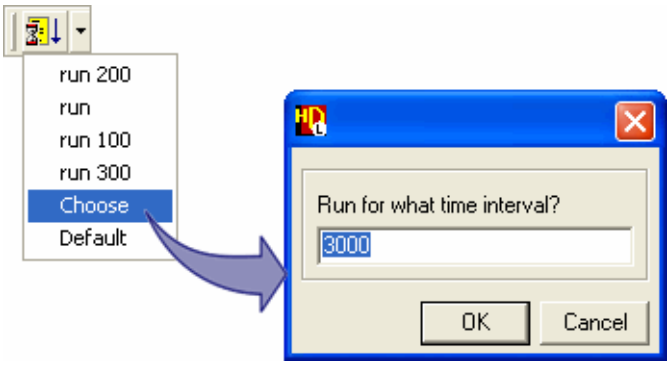




4. Click the **Run Forever** button again and notice that the sequence from 0 to 144 is repeated.

5. Make the source window active and remove the breakpoint by right clicking on the BP column of line 193 and choosing **Remove Breakpoint 193** from the popup menu.

6. In the *fibgen_tb* block diagram click the button adjacent to the **Run For Time** button on the toolbar and select **Choose** from the popup menu. A dialog box is displayed which allows you to enter a simulator run time interval. For example, enter 3000 into the entry box and click **OK** to run the simulator.



Notice that the Fibonacci sequence repeats every 2,650 nano-seconds.

You can display the full waveform in the Model*Sim* Wave window by choosing **Zoom Full** from the **Zoom** cascade of the **Wave** cascade of the **View** menu.

You can restart the simulation by using the **Restart Simulator** button.

7. Simulation is now complete. Choose **Quit** from the Model*Sim* **File** menu to exit from the simulator. Click **Yes** to the exit message. Close the *fibgen_tb* block diagram.

Synthesize the Design

If your FPGA Advantage configuration includes both LeonardoSpectrum and Precision Synthesis, you can perform the synthesis procedures using either of these tools.

Procedures for Running the LeonardoSpectrum Flow are given on page 27.

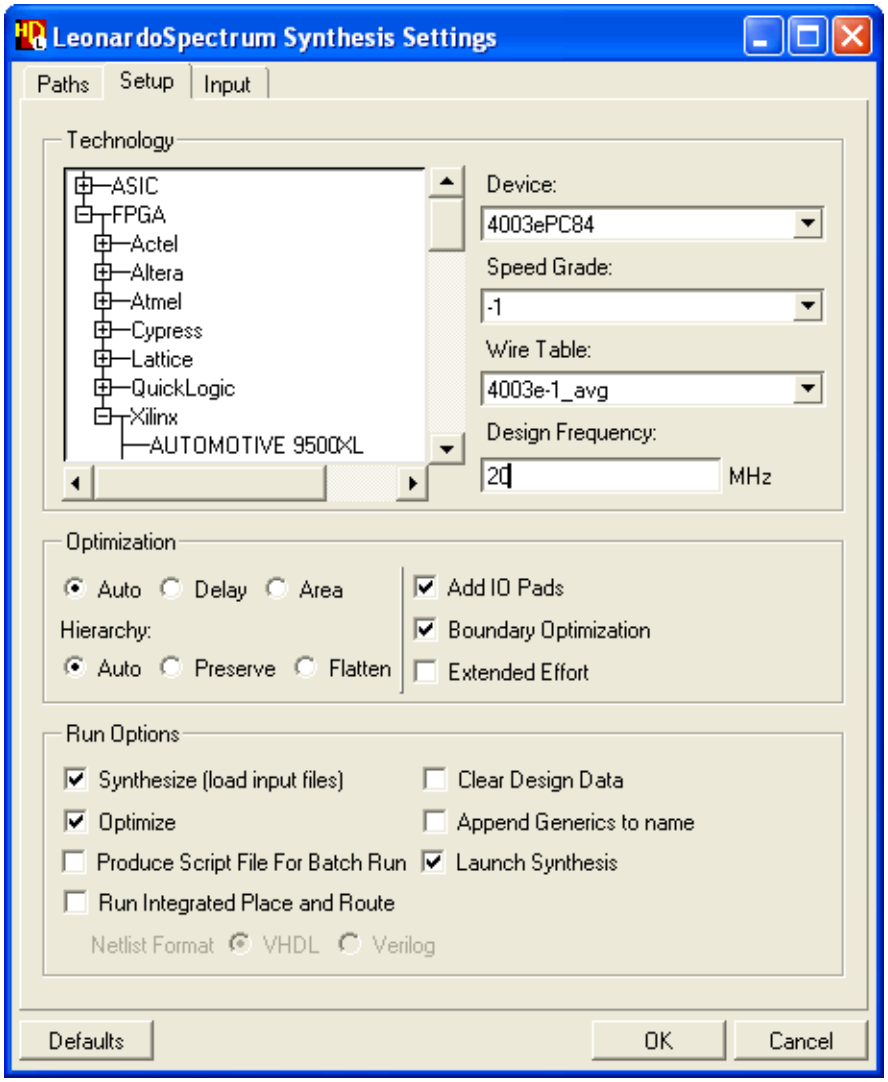
Procedures for Running the Precision Synthesis Flow are given on page 30.

Running the LeonardoSpectrum Flow

1. Select the *fibgen* component in the design manager and click on the  button. To add the button to the toolbar choose **Toolbar** from the **Add to** cascade of Leonardo Spectrum flow popup menu in the Tasks pane.

   The LeonardoSpectrum Synthesis Settings dialog is displayed.

2. Select the technology of your choice in the **Setup** tab. For example, choose ***FPGA*> Xilinx> *XC4000E***.

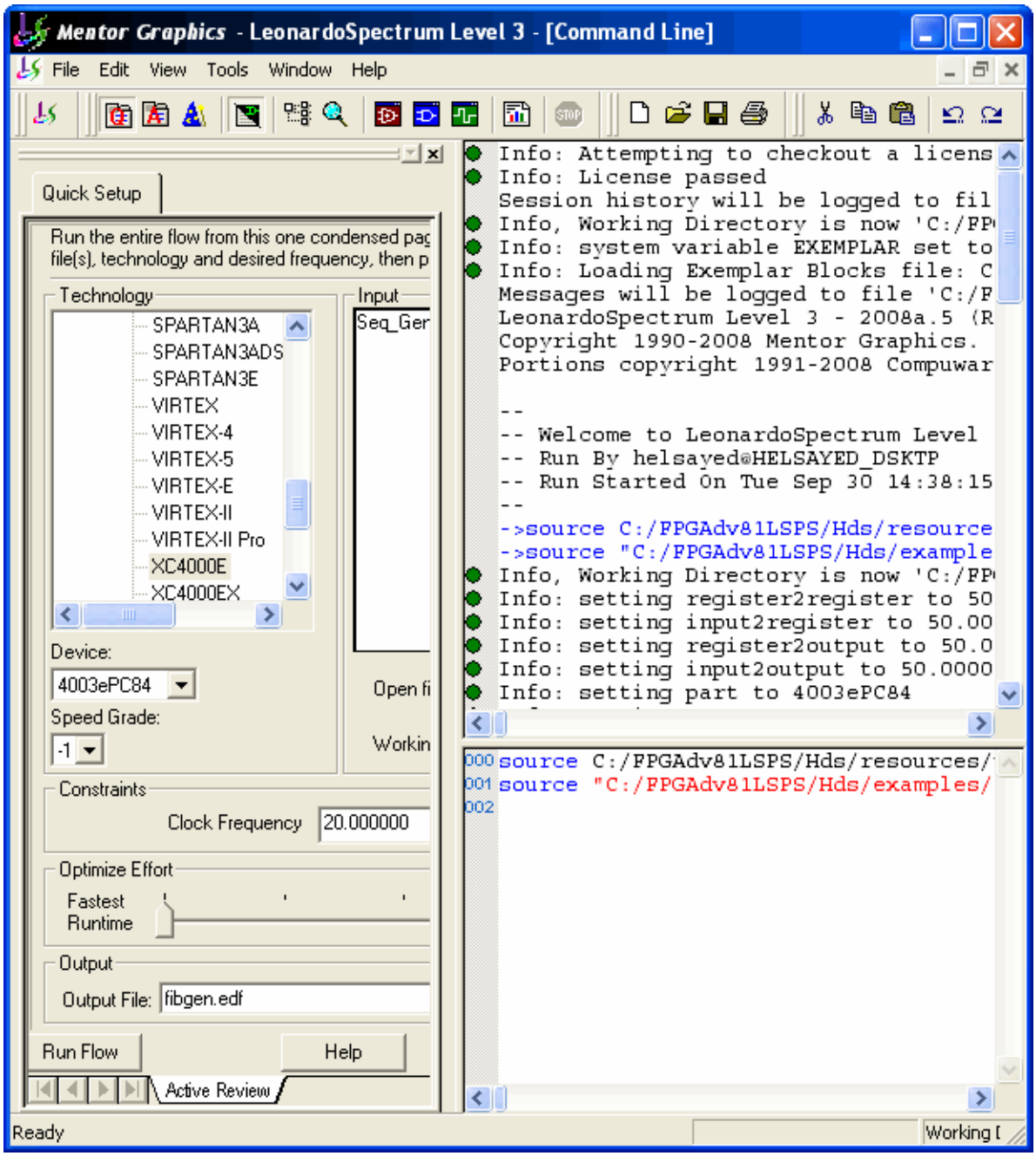


When you select a technology, default values are automatically entered in the Device, Speed Grade and Wire Table fields.

3. Enter the value *20* in the Design Frequency field and synthesize your design using the default options in the remaining fields by clicking the **OK** button.

   When you confirm the dialog box, your design is synthesized and optimized for the selected technology.

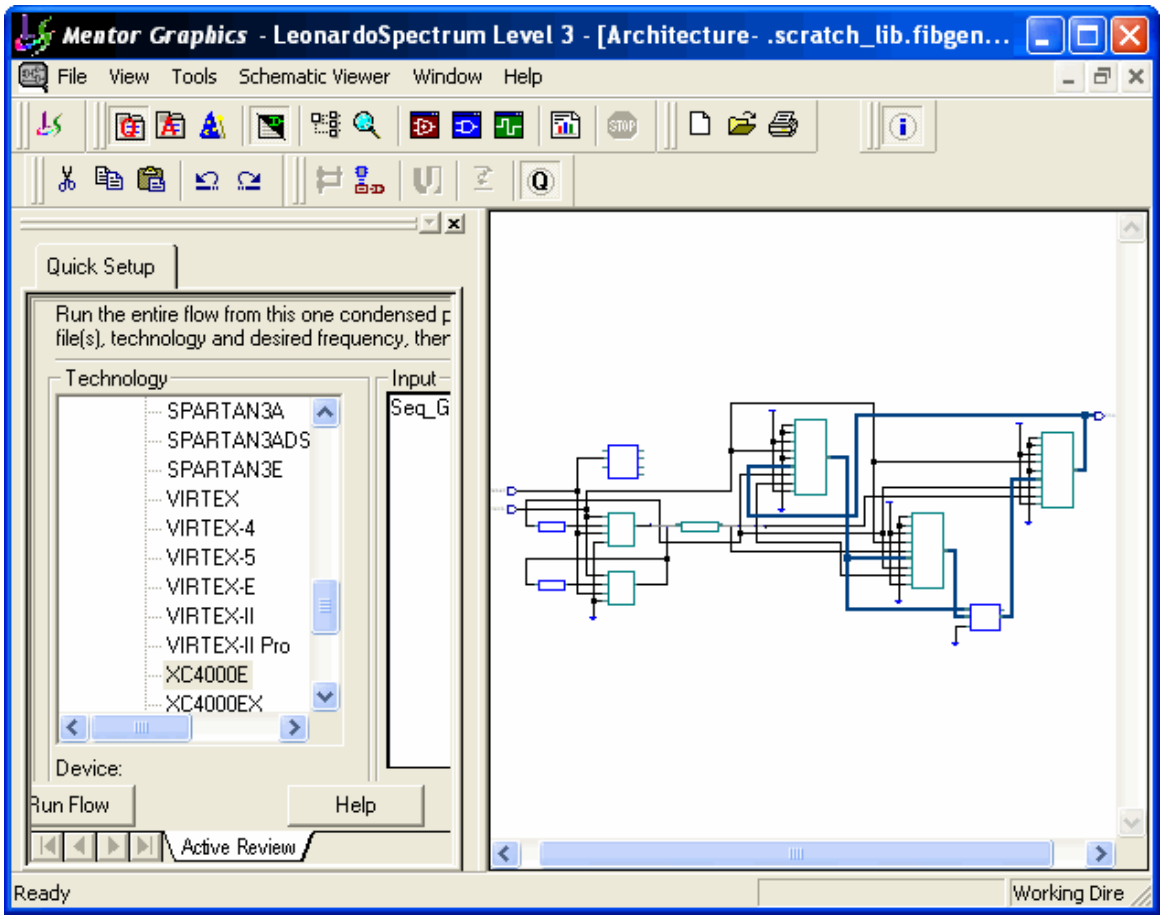
   LeonardoSpectrum optimizes the design. Progress and completion messages are displayed in the information window showing that the synthesis run has finished.



View the LeonardoSpectrum RTL Schematic

1. If you are using the Level 3 license, you can display an RTL Schematic for your design by clicking the **View RTL Schematic** button.

   You can move around the schematic using the scroll bars and the diagram can be enlarged inside the browser by choosing **Zoom In** from the **Zoom** cascade of the **Schematic Viewer** pulldown menu.



   You can cross-probe from the schematic to the corresponding object in a HDS source view by selecting an instance on the schematic and clicking the right mouse button and choosing **Trace to HDL Designer** from the popup menu.

Note

The Schematic Viewer is not available with a LeonardoSpectrum level 2 license unless you have an additional license feature for LeonardoInsight.

2. You have now completed this tutorial. Close any cross-referenced windows. Close the LeonardoSpectrum window by choosing **Exit** from the **File** menu and answering **No** when you are prompted whether to save your project settings. Close the HDS window

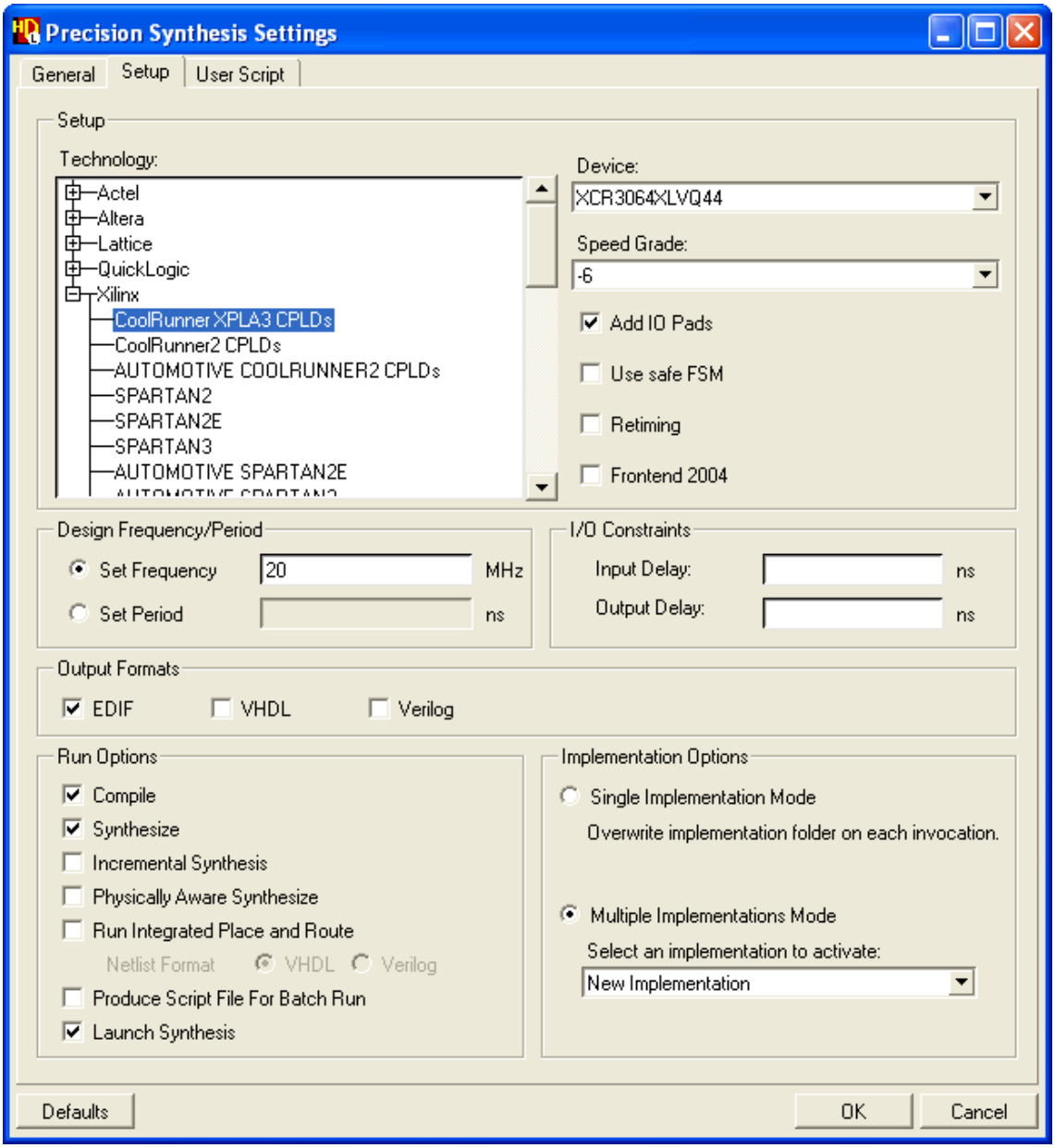
by choosing **Exit** from the **File** menu in the design manager window and answering **Yes** in the confirmation dialog box.

Running the Precision Synthesis Flow

1. Select the *fibgen* component in the HDS Design Manager and click on the **Precision Synthesis Flow** button.

   The Precision Synthesis Settings dialog is displayed.

2. Select the technology of your choice in the **Setup** tab. For example, choose ***Xilinx>CoolRunner XPLA3CPLDS***.

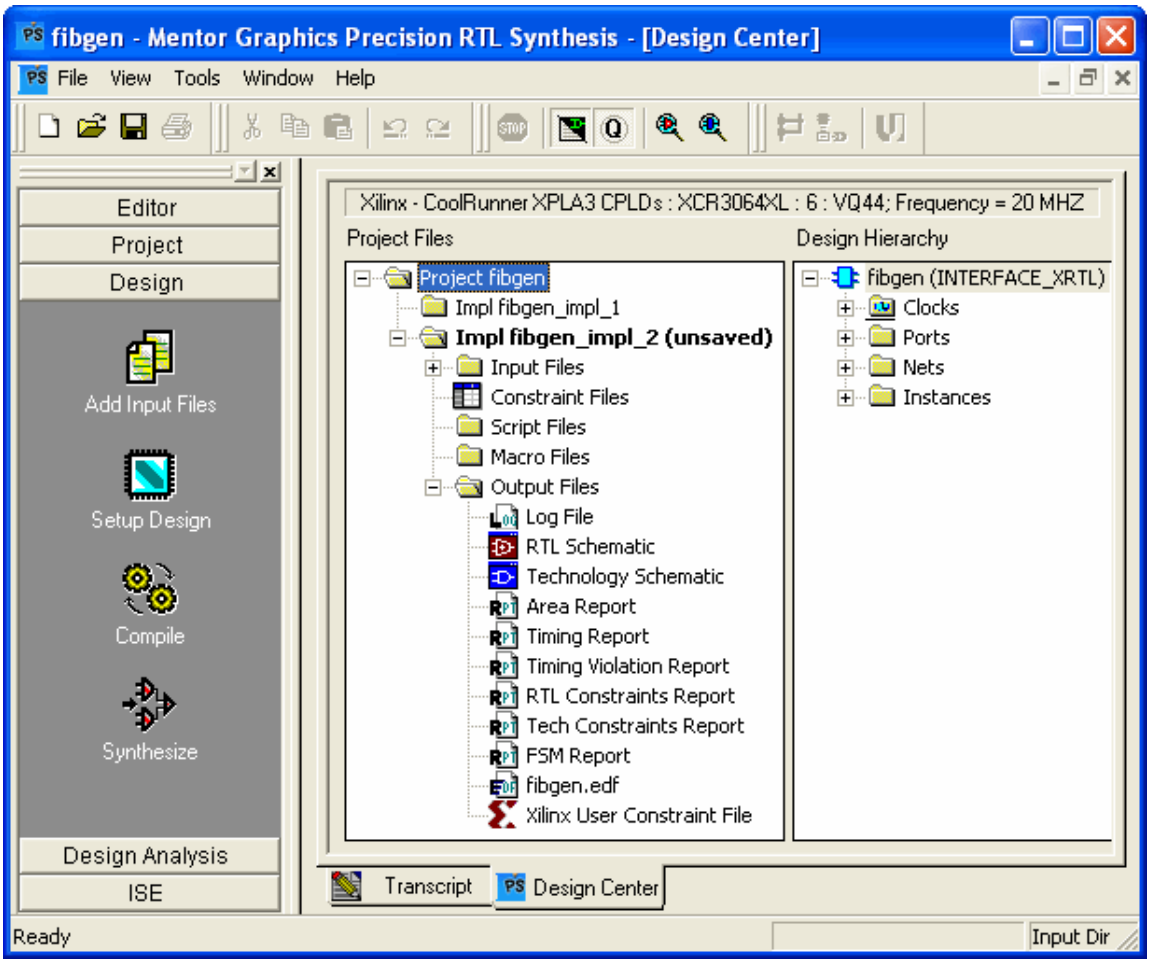


When you select a technology, default values are automatically entered in the *Device* and *Speed Grade* fields.

3. Enter the value *20* in the *Design Frequency/Period* field and synthesize your design using the default options in the remaining fields by clicking the **OK** button.

   The Precision Synthesis design center window is displayed showing all of the project files and design hierarchy for the synthesized design. The contents of the *Log File* in the Output Files folder shows the progress and completion of the synthesis run and indicates that synthesis has been completed successfully.

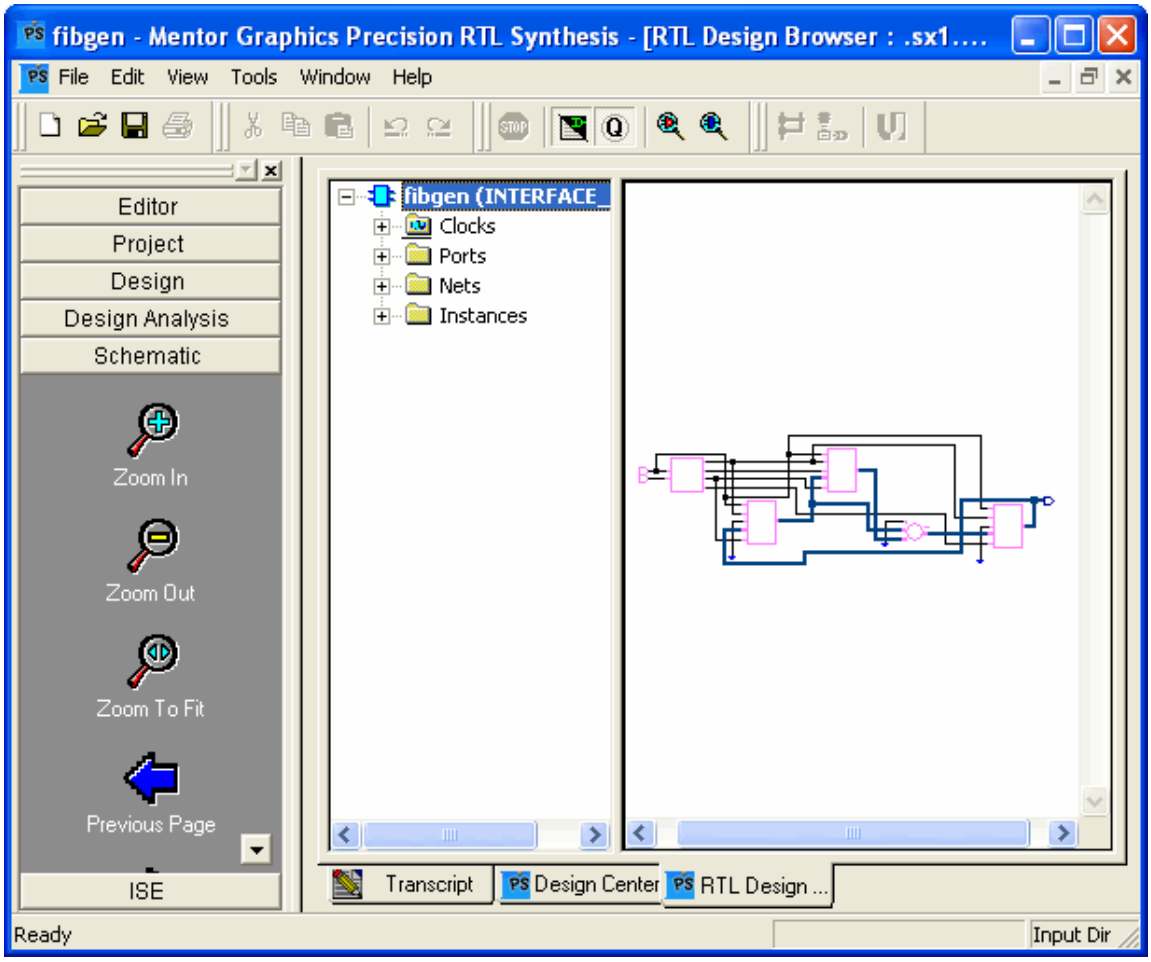
   You can double-click the *Log File* or any other file in the design center to check and monitor the progress of the synthesis tool.



View the Precision Synthesis RTL Schematic

1. Double-click the RTL Schematic icon in the list of output files in the *Project Files* pane to open the schematic diagram in a new **Design Browser** tab.

You can move around the schematic using the scroll bars or the diagram can be enlarged inside the browser by choosing the **Zoom In** shortcut. You can also use the **Zoom Out** or **Zoom To Fit** shortcuts to view and adjust the diagram inside the browser.



You can cross-probe from the schematic to the corresponding object in a HDS source view by selecting an instance on the schematic and clicking the right mouse button and choosing **Trace to HDL Designer** from the popup menu.

2. You have now completed this tutorial. Close any cross-referenced windows. Close the Precision Synthesis window by choosing **Exit** from the **File** menu and answering **No** when you are prompted whether to save your project settings. Close the HDS window by choosing **Exit** from the **File** menu in the design manager window and answering **Yes** in the confirmation dialog box.

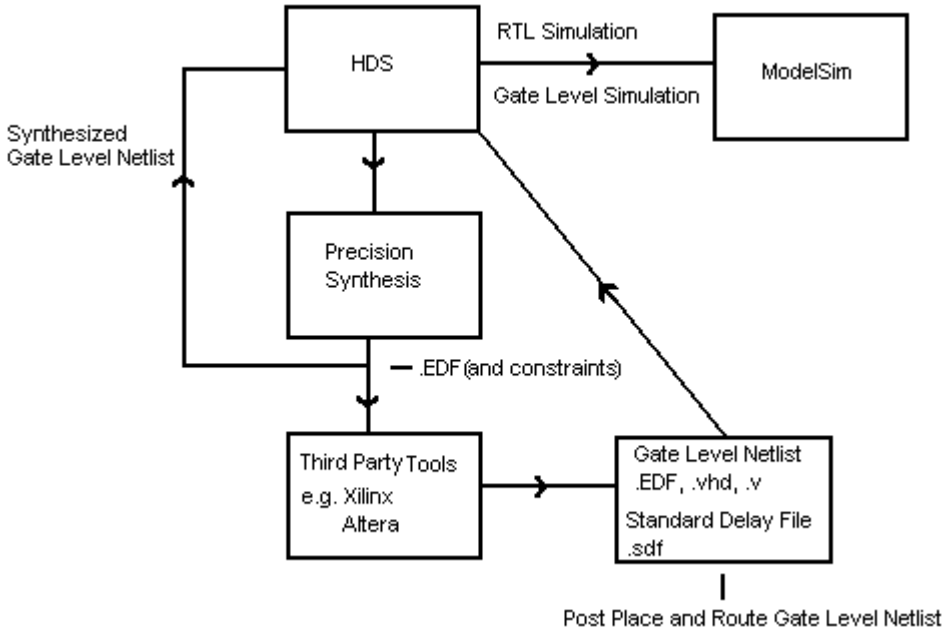
About Gate Level Simulation

The FPGA Advantage Tutorial has shown how to create a simple design flow using a sample text design. The design flow showed the first stage of simulation at RTL level using Model*Sim* as part of the FPGA Advantage design environment.

A second stage of simulation is possible at gate-level after synthesis where the output of an FPGA vendors place and route tool is used to create a gate-level netlist.

The netlist may also include timing information which is defined in a Standard Delay File (.sdf).

This flow is shown in the diagram below where a post place and route gate-level netlist is loaded into the simulation environment along with the.sdf file.



Further Information

Each of the tools integrated within FPGA Advantage support a large range of features which cannot be illustrated in this simple tutorial. For more information, see links which are available from the **Help** menu in each tool.

General information about the documentation including a list of other HDL Designer Series tutorials can be found in the *Start Here Guide for FPGA Advantage*.

Information about supported third party vendors tools can be found at:

http://www.altera.com
http://www.xilinx.com

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