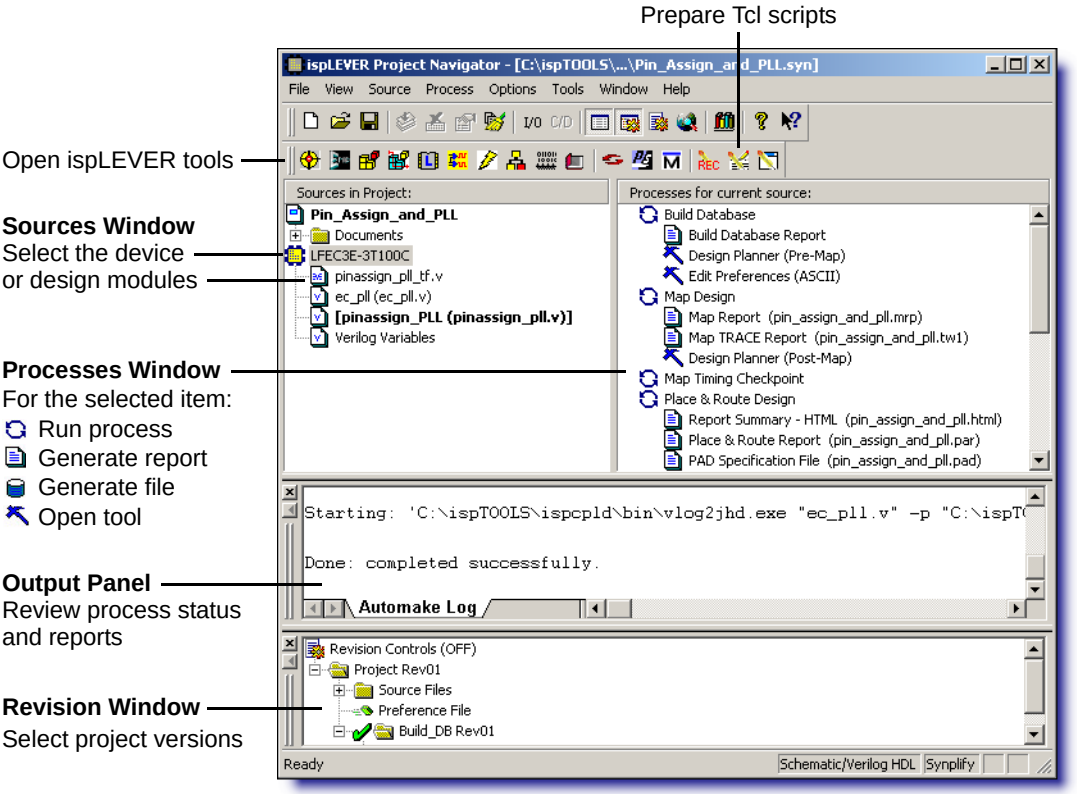
Quick Start Guide for ispLEVER Software

This guide offers a quick overview of using ispLEVER® software to implement a design in a Lattice Semiconductor device. For more information, check the ispLEVER Help in the Help menu.

ispLEVER Project Navigator

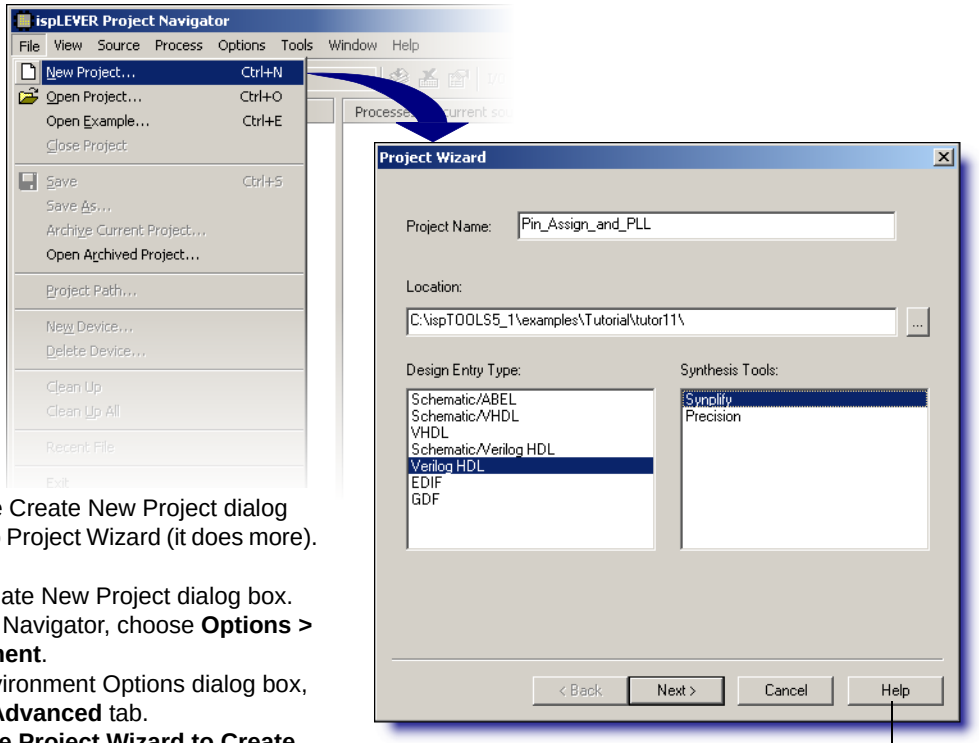
Project Navigator is the primary interface for the ispLEVER software. It organizes the files, gives access to the tools, and delivers messages. To start Project Navigator:

- Windows: choose **Start > Programs > Lattice Semiconductor > ispLEVER Project Navigator**.
- UNIX or Linux: on a command line, enter **ispgui**.



Creating a Project

Choose **File >** **New Project**.



If you see the Create New Project dialog box, switch to Project Wizard (it does more). To switch:

1. Close Create New Project dialog box.
2. In Project Navigator, choose **Options > Environment**.
3. In the Environment Options dialog box, click the **Advanced** tab.
4. Select **Use Project Wizard to Create New Design**.
5. Click **OK**.

With the Project Wizard, set initial values for:

- Project name
- Location of the files
- Design language
- Synthesis tool
- Target device
- Source files

Design Entry Type (language) depends on the target device:

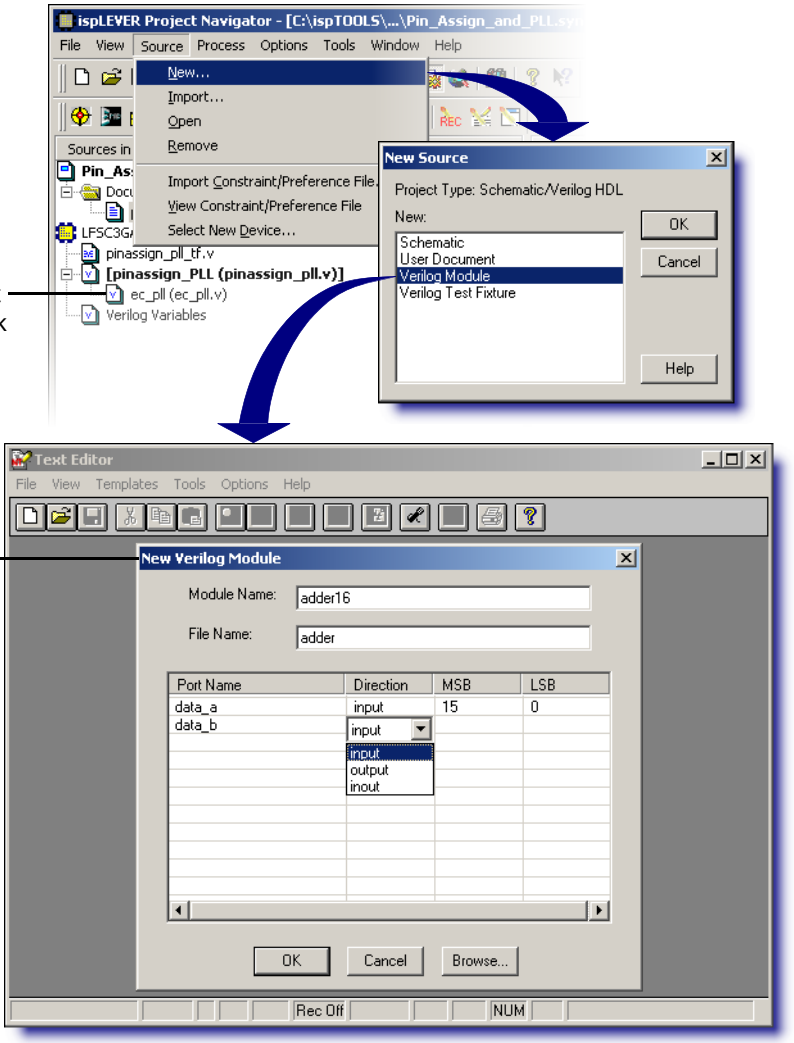
Target Device	Verilog	VHDL	EDIF	Schematic/ Verilog	Schematic/ VHDL	Schematic/ ABEL
FPGA	◆	◆	◆	◆	◆	
ispXPGA®	◆	◆	◆			
CPLD/SPLD	◆	◆	◆	◆	◆	◆
ispXPLD®	◆	◆	◆	◆	◆	
ispGDX2™	◆	◆	◆			

Entering the Design

- To create an HDL or schematic file, choose **Source > New**.
- To import an HDL or schematic file, choose **Source > Import**.
- To add an IP module, choose **Tools >** **IPexpress** (for FPGAs) or **Tools >** **Module/IP Manager** (for all other devices). After generating the IP module, import it and instantiate it in an HDL or schematic module.

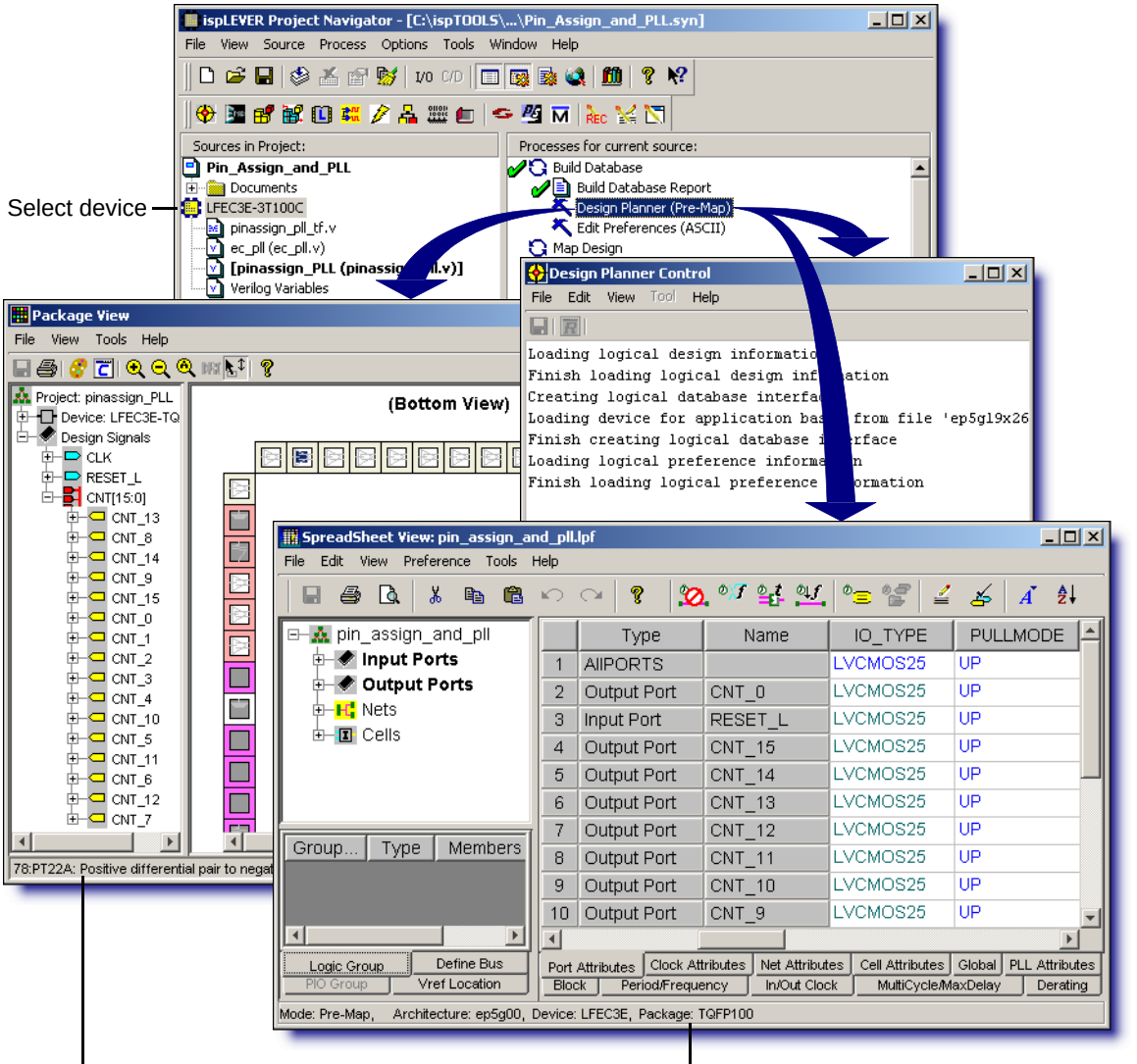
To modify an existing part of the design, double-click the file or module name.

Starts the code for the HDL module and adds the file to the project.



Setting Timing and I/O

Select the device . Then, in the Processes Window, double-click **Design Planner** (for FPGAs) or **Constraint Editor** (for all other devices). The Design Planner starts with three windows, as shown below; the Constraint Editor combines them as three panes in one window.



Package View
Assign pinouts by drag-and-drop.

In Constraint Editor, choose
Device >  **Package View**.

Design Planner's Spreadsheet View
To set preferences, enter them in the sheet or through the **Preference** menu.

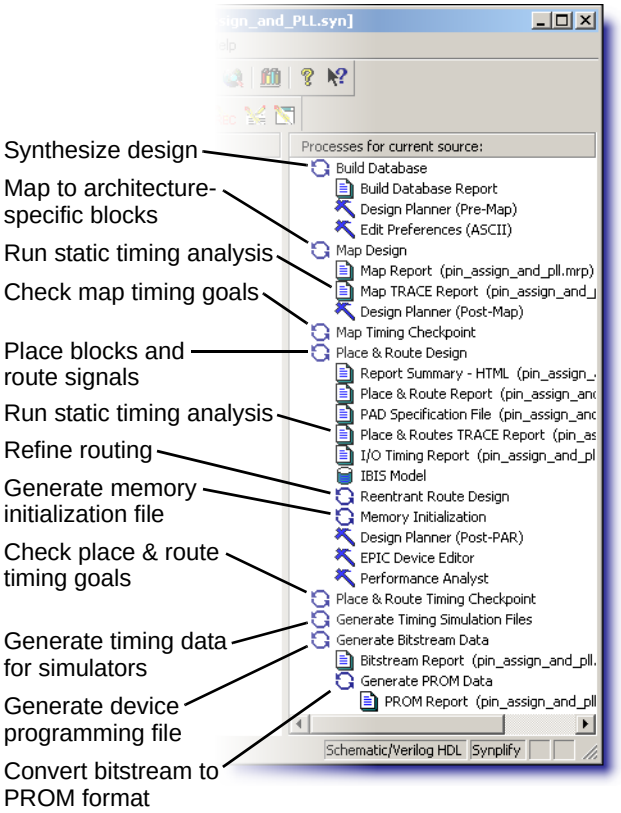
Constraint Editor's Constraint Sheet
To set constraints, enter them in the sheet or through the **Pin Attribute** and **Device** menus.

Implementing the Design

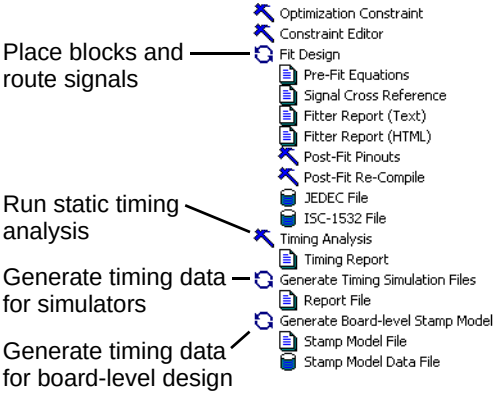
Select the device , then double-click a process . Start at the top and work down. The list of processes varies with the device and other factors. Following are some examples.

For more information about a process, select it and press **F1**.

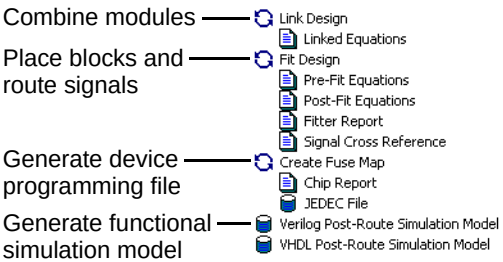
FPGA Processes



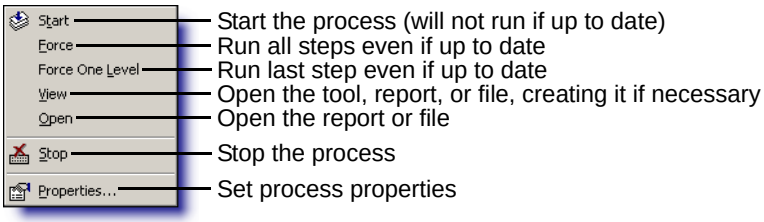
CPLD & ispGDX2 Processes



GAL® & ispGAL® Processes



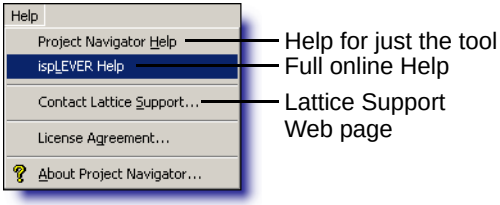
For a menu of options, right-click the process.



Getting More Information

Refer to the Online Help

- Choose **Help > ispLEVER Help**.



- Select an item in a window or dialog box and press **F1**.
- Click **Help** in a dialog box.

From the first topic in the online Help you can also:

- Take tutorials.
- Refer to design guides and reference manuals.
- Refer to synthesis and simulator tool manuals.

Refer to the Web Site

Lattice Semiconductor
www.latticesemi.com

What's New at Lattice
www.latticesemi.com/whatsnew.cfm
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Call between 8 a.m. to 5 p.m. Pacific Time.