

Quick Start Guide for ispLEVER Software

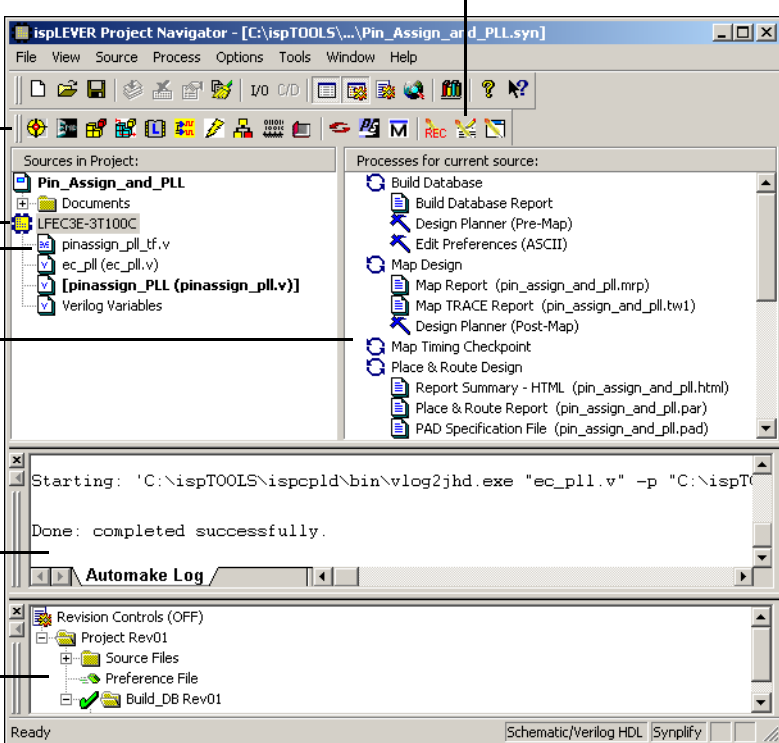
This guide offers a quick overview of using ispLEVER[®] software to implement a design in a Lattice Semiconductor device. For more information, check the ispLEVER Help in the Help menu.

ispLEVER Project Navigator

Project Navigator is the primary interface for the ispLEVER software. It organizes the files, gives access to the tools, and delivers messages. To start Project Navigator:

- ◆ Windows: choose **Start > Programs > Lattice Semiconductor > ispLEVER Project Navigator**.
- ◆ UNIX or Linux: on a command line, enter **ispgui**.

Prepare Tcl scripts



Open ispLEVER tools

Sources Window
Select the device or design modules

Processes Window
For the selected item:

- Run process
- Generate report
- Generate file
- Open tool

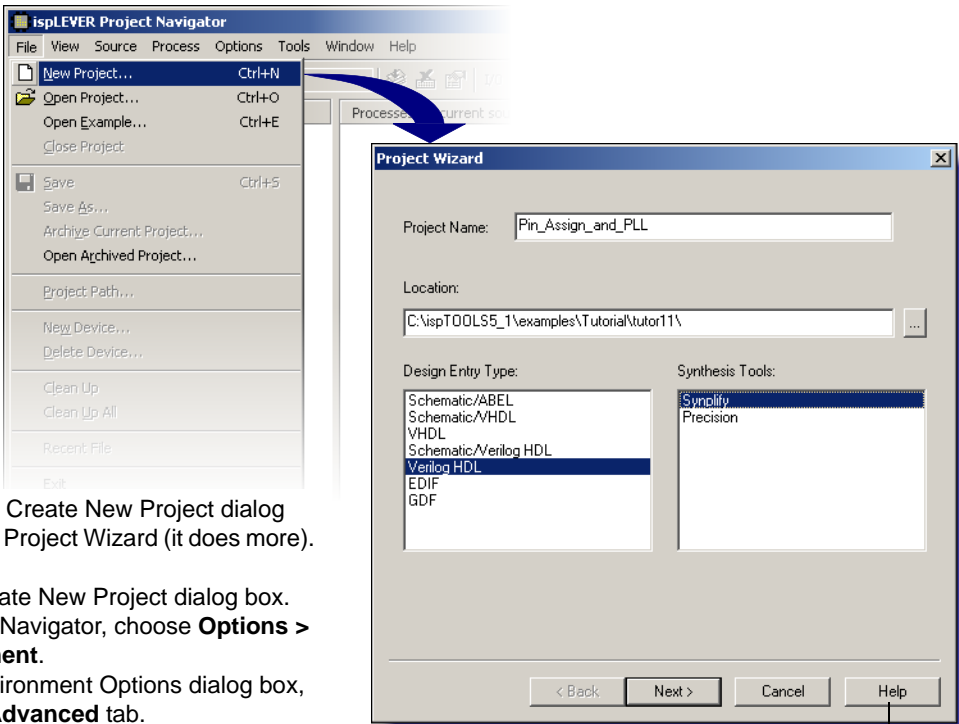
Output Panel
Review process status and reports

Revision Window
Select project versions

Ready

Creating a Project

Choose **File >  New Project.**



If you see the Create New Project dialog box, switch to Project Wizard (it does more). To switch:

1. Close Create New Project dialog box.
2. In Project Navigator, choose **Options > Environment**.
3. In the Environment Options dialog box, click the **Advanced** tab.
4. Select **Use Project Wizard to Create New Design**.
5. Click **OK**.

For more information, click **Help**


With the Project Wizard, set initial values for:

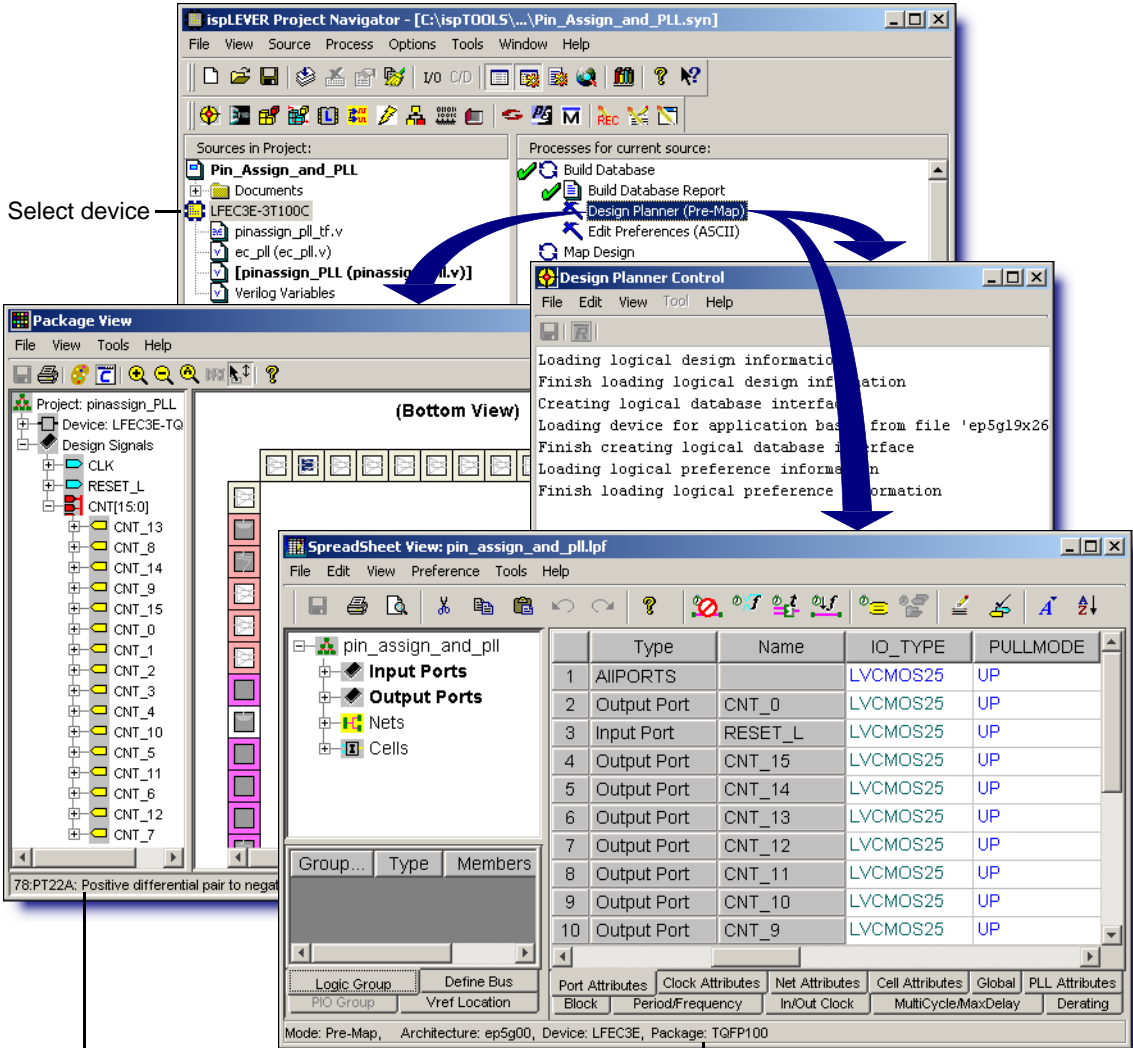
- ◆ Project name
- ◆ Design language
- ◆ Target device
- ◆ Location of the files
- ◆ Synthesis tool
- ◆ Source files

Design Entry Type (language) depends on the target device:

Target Device	Verilog	VHDL	EDIF	Schematic/Verilog	Schematic/VHDL	Schematic/ABEL
FPGA	◆	◆	◆	◆	◆	
ispXPGA [®]	◆	◆	◆			
CPLD/SPLD	◆	◆	◆	◆	◆	◆
ispXPLD [®]	◆	◆	◆	◆	◆	
ispGDX2 [™]	◆	◆	◆			

Setting Timing and I/O

Select the device . Then, in the Processes Window, double-click **Design Planner** (for FPGAs) or **Constraint Editor** (for all other devices). The Design Planner starts with three windows, as shown below; the Constraint Editor combines them as three panes in one window.





Package View
Assign pinouts by drag-and-drop.

In Constraint Editor, choose **Device >**  **Package View.**

Design Planner's Spreadsheet View
To set preferences, enter them in the sheet or through the **Preference** menu.

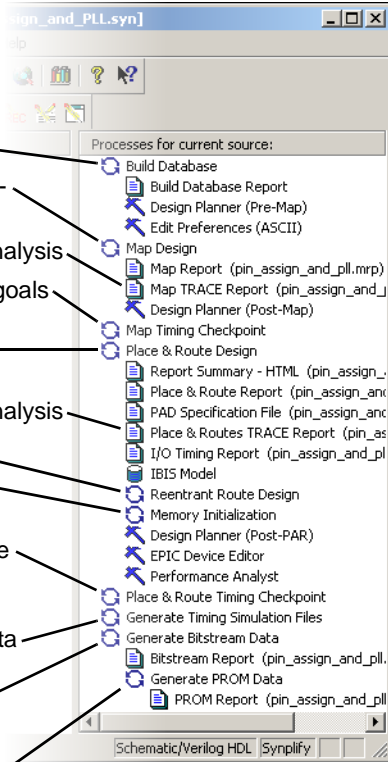
Constraint Editor's Constraint Sheet
To set constraints, enter them in the sheet or through the **Pin Attribute** and **Device** menus.

Implementing the Design

Select the device , then double-click a process . Start at the top and work down. The list of processes varies with the device and other factors. Following are some examples.

For more information about a process, select it and press **F1**.

FPGA Processes



Synthesize design

Map to architecture-specific blocks

Run static timing analysis

Check map timing goals

Place blocks and route signals

Run static timing analysis

Refine routing

Generate memory initialization file

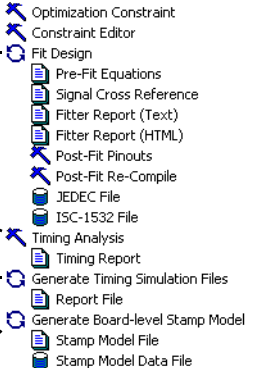
Check place & route timing goals

Generate timing data for simulators

Generate device programming file

Convert bitstream to PROM format

CPLD & ispGDx2 Processes



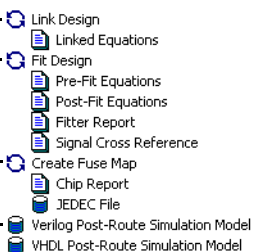
Place blocks and route signals

Run static timing analysis

Generate timing data for simulators

Generate timing data for board-level design

GAL® & ispGAL® Processes



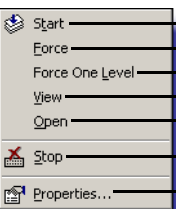
Combine modules

Place blocks and route signals

Generate device programming file

Generate functional simulation model

For a menu of options, right-click the process.



Start — Start the process (will not run if up to date)

Force — Run all steps even if up to date

Force One Level — Run last step even if up to date

View — Open the tool, report, or file, creating it if necessary

Open — Open the report or file

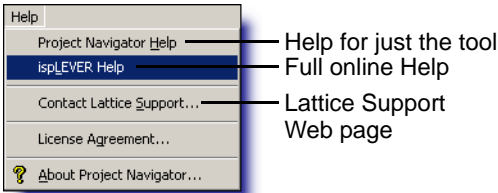
Stop — Stop the process

Properties... — Set process properties

Getting More Information

Refer to the Online Help

- ◆ Choose **Help > ispLEVER Help**.



- ◆ Select an item in a window or dialog box and press **F1**.
- ◆ Click **Help** in a dialog box.

From the first topic in the online Help you can also:

- ◆ Take tutorials.
- ◆ Refer to design guides and reference manuals.
- ◆ Refer to synthesis and simulator tool manuals.


Refer to the Web Site

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www.latticesemi.com

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