



Fremont Micro Devices

FT61FC2

Data Sheet

Key Features

8-bit EEPROM based RISC MCU
Program: 2k x 14; RAM: 128 x 8; Data: 256 x 8
6 / 8 / 10 / 14 / 16 Pins
True 10-bit ADC accuracy ADC
7 Timers, 4 Individual PWMs – 1 with Deadband
2 Comparators, 2 Regulator outputs
Low Standby, WDT and Operation Current
POR, LVR, LVD
High ESD, High EFT
Low V_{DD} Operation

Rev1.03

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8-bit CPU (EEPROM)

- 37 RISC instructions: 2T or 4T
- 16 MHz / 2T ($V_{DD} \geq 2.7$)
- Up to 16 pins

Memory

- PROGRAM: 2k x 14 bit (RW Protect)
- DATA: 256 x 8 bit
- RAM: 128 x 8 bit
- 8-level Hardware Stack

Operation Conditions (5V, 25°C)

- V_{DD} ($V_{POR} \leq 2.0V$) $V_{POR} - 5.5 V$
(Self-regulated by POR, $\leq 1.7V$ for above $0^\circ C$)
- Operation Temperature Grade1 $-40 - +125^\circ C$
- Operation Temperature Grade2 $-40 - +105^\circ C$
- Operation Temperature Grade3 $-40 - +85^\circ C$
- Low Standby 0.8 μA
- WDT 3.2 μA
- Normal Mode (16 MHz) 207 $\mu A/mips$

High Reliability

- 1M cycles, >20 years / $85^\circ C$ storage (typical)
- ESD > 4 kV, EFT > 5.5 kV

ADC (10-bit)

- True 10-bit Accuracy (≤ 1 MHz ADC clk)
- 7 + 1 Channels
- $V_{ADC-REF}$
 - ✓ Internal: 2.0, 3.0, V_{DD}
 - ✓ External: VREF pin
- Special event trigger and Interrupt

2 Comparators

- 16 level programmable voltage reference

2 Regulator outputs

- up to 32 stalls voltage

PWM (Total 5)

- Enhanced capture/Compare/PWM
 - ✓ PWM mode:
 - single PWM, half-bridge, full-bridge
 - ✓ 3 channels (up to 6 I/O):
 - Complementary + Deadband
 - ✓ One-Pulse mode
 - ✓ Same Period, Duty Cycle
 - ✓ Optional output polarity

- PWM (3 channels)
 - ✓ Support RUN in SLEEP
 - ✓ Independent: Period, Duty Cycle, Polarity
 - ✓ Buzzer mode

Timers

- WDT (16-bit): 7-bit postscaler
- Timer0 (8-bit): 8-bit prescaler
- Timer1 (16-bit): 3-bit prescaler with Gate Control
- Timer2 (8-bit): 4-bit pre and post-scaler
- Timer3/4/5(12-bit): 7-bit prescaler and 8-bit postscaler
- Support RUN in SLEEP
- 1 or 2x { Instr. Clock, HIRC}, LP, T0CK, T1CK

I/O PORTS (Up to 14 I/O)

- Resistive Pull-Up / Pull-Down
- All I/O I_{SOURCE} : 22mA (5V, $25^\circ C$)
- All I/O I_{SINK} : 19mA (5V, $25^\circ C$)
- 8 I/O: Interrupt / Wake-Up

Power Management

- SLEEP
- LVR: 2.0, 2.2, 2.5, 2.8, 3.1, 3.6, 4.1 (V)
- LVD: 2.0, 2.4, 2.8, 3.0, 3.6, 4.0 (V)

System Clock (SysClk)

- ✓ HIRC High Speed Internal Oscillator
 - ✓ 16MHz $\leq \pm 1.5\%$ typical (2.5–5.5V, $25^\circ C$)
 - ✓ 1, 2, 4, 8, 16, 32, 64 divider
- LIRC Low Power Internal Oscillator
 - ✓ 32 kHz or 256 kHz
- External Clock (I/O input)
- Crystal Input (LP / XT)
 - ✓ HIRC or LIRC during startup
 - ✓ Fail Detect

Integrated Development Environment (IDE)

- On-Chip Debug (OCD), ISP
- 3 hardware breakpoints
- System-Reset, Stop, Single Step, Run

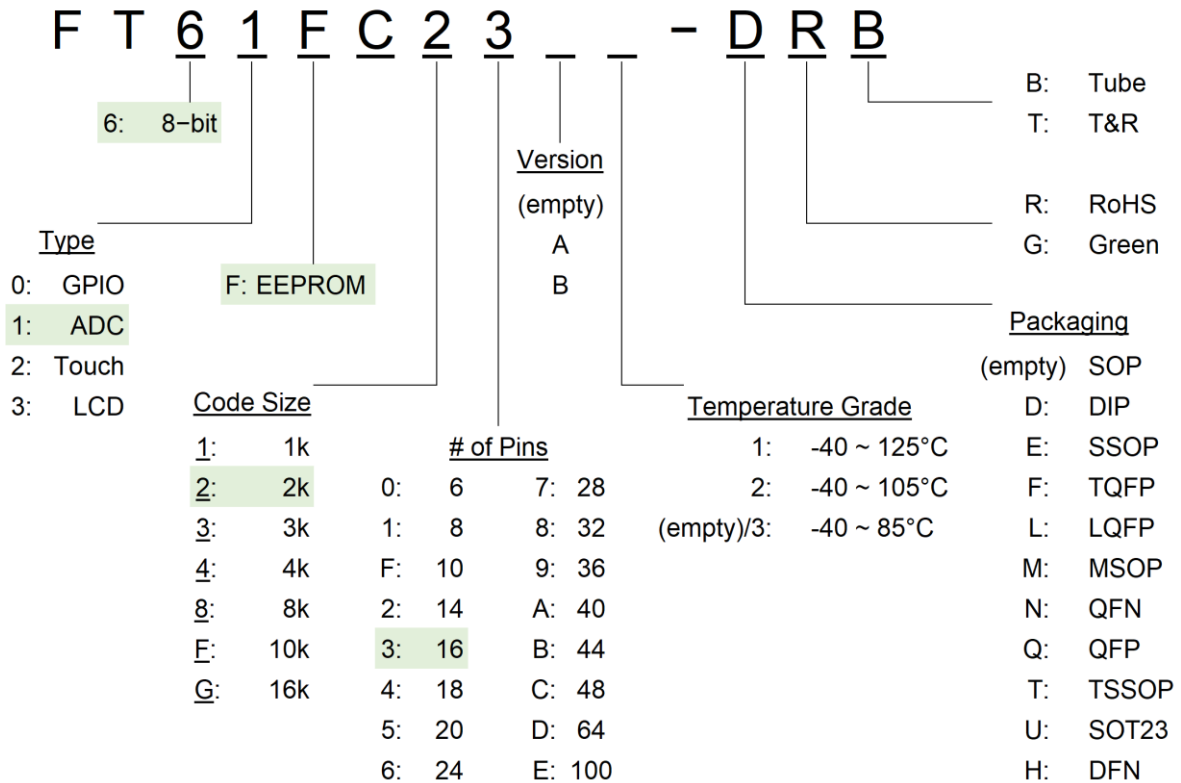
Packages

- SOT23-6 SOP8 DIP8 MSOP10
- SOP14 DIP14 SOP16 DIP16

PARTS INFORMATION AND SELECTIONS

| Part # | # of I/O | Package |
|--------------------------|----------|---------|
| FT61FC20-U _{ab} | 4 | SOT23-6 |
| FT61FC21A- <u>ab</u> | 6 | SOP8 |
| FT61FC21A-D <u>ab</u> | | DIP8 |
| FT61FC21B- <u>ab</u> | | SOP8 |
| FT61FC21B-D <u>ab</u> | | DIP8 |
| FT61FC2F-M <u>ab</u> | 8 | MSOP-10 |
| FT61FC22A- <u>ab</u> | 12 | SOP14 |
| FT61FC22A-D <u>ab</u> | | DIP14 |
| FT61FC23- <u>ab</u> | 14 | SOP16 |
| FT61FC23-D <u>ab</u> | | DIP16 |

Where a = R; RoHS
 = G; Green b = B; Tube
 = T; T&R



MCU Part # Selections

Revision History

| Date | Revision | Description |
|------------|----------|---|
| 2022-01-17 | 1.00 | Preliminary version |
| 2022-03-01 | 1.01 | Updated Section 18 Electrical Specifications |
| 2022-06-10 | 1.02 | Updated Section 18 Electrical Specifications |
| 2022-08-24 | 1.03 | Updated Section 6 Oscillator and Sysclk description |

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1. BLOCK DIAGRAM AND PINOUTS

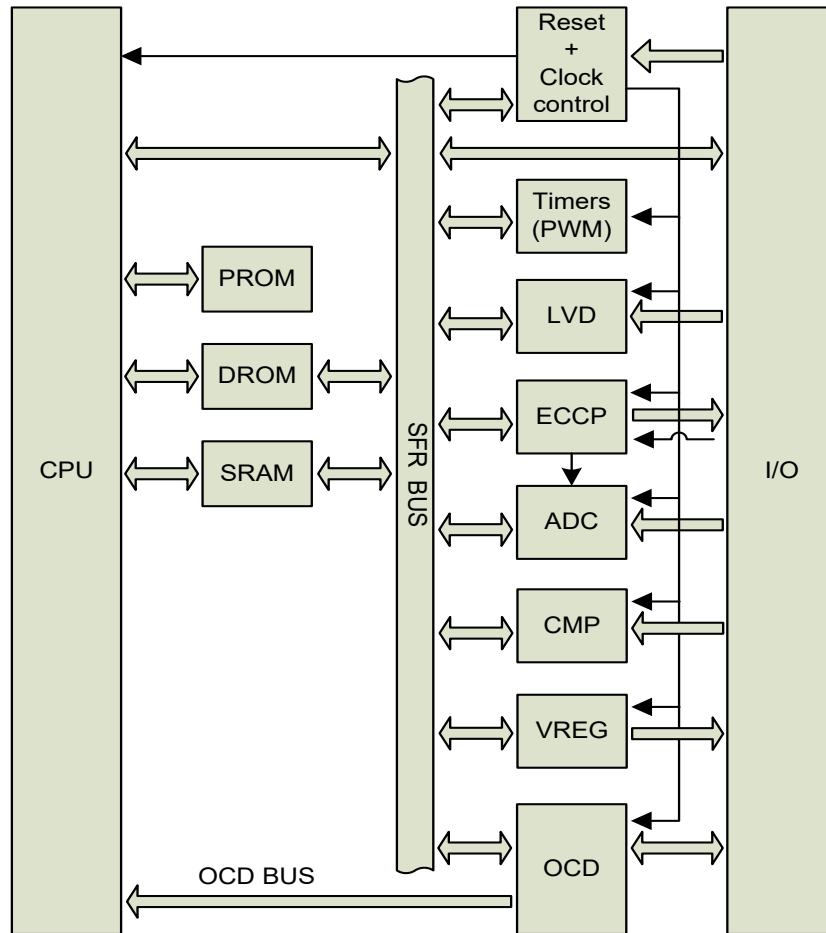


Figure 1-1 System block diagram

The list of standard abbreviation is as follows:

| Abbreviation | Description |
|--------------|---|
| CPU | Central Processing Unit |
| SFR | Special Function Registers |
| SRAM | Static Random Access Memory |
| DROM | Data EEPROM |
| PROM | Program EEPROM |
| Timers | WDT, Timer0, Timer1, Timer2, Timer3, Timer4, Timer5 |
| PWM | Pulse Width Modulator |
| ECCP | Enhanced Capture Compare and PWM |
| ADC | Analog to Digital Converter |
| CMP | Comparator |
| VREG | Voltage Regulator |
| LVD | Low Voltage Detect |
| OCD | On Chip Debug |
| I/O | Input / Output |

1.1 Pinouts

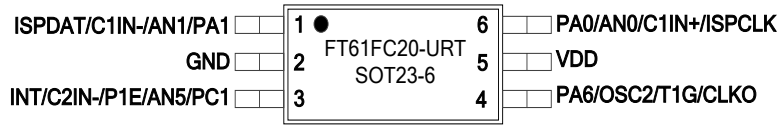


Figure 1-2 SOT23-6

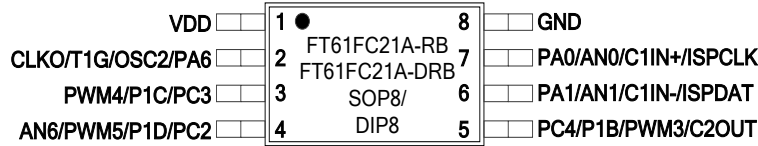


Figure 1-3 SOP8 / DIP8 (A)

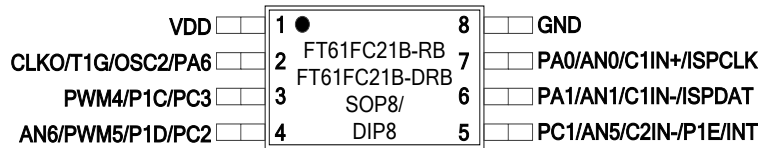


Figure 1-4 SOP8 / DIP8 (B)

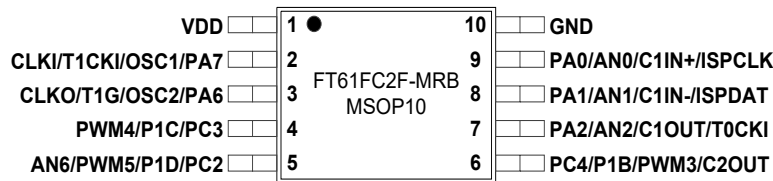


Figure 1-5 MSOP10

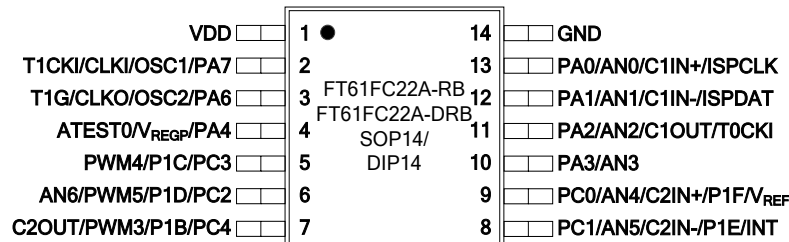


Figure 1-6 SOP14 / DIP14

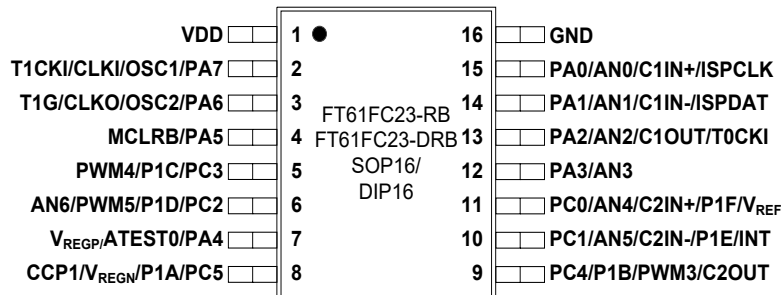


Figure 1-7 SOP16 / DIP16

1.2 Pin Description by Functions

| Function | Description | Pin Name | GPIO equiv. | 6 pins | 8(A) pins | 8(B) pins | 10 pins | 14 pins | 16 pins | |
|-------------------------------|--|----------|-------------|--------|-----------|-----------|---------|---------|---------|----|
| Power | | VDD | | 5 | 1 | 1 | 1 | 1 | 1 | |
| | | GND | | 2 | 8 | 8 | 10 | 14 | 16 | |
| GPIO | Pull-Up / Pull-Down, Digital Input, Digital Output | PC5 | | | | | | | 8 | |
| | | PC4 | | | 5 | | 6 | 7 | 9 | |
| | | PC3 | | | | 3 | 3 | 4 | 5 | 5 |
| | | PC2 | | | | 4 | 4 | 5 | 6 | 6 |
| | | PC1 | | | 3 | | 5 | | 8 | 10 |
| | | PC0 | | | | | | | 9 | 11 |
| | | PA7 | | | | | | 2 | 2 | 2 |
| | | PA6 | | | 4 | 2 | 2 | 3 | 3 | 3 |
| | | PA5 | | | | | | | | 4 |
| | | PA4 | | | | | | | 4 | 7 |
| | | PA3 | | | | | | | 10 | 12 |
| | | PA2 | | | | | | 7 | 11 | 13 |
| | | PA1 | | | 1 | 6 | 6 | 8 | 12 | 14 |
| | | PA0 | | | 6 | 7 | 7 | 9 | 13 | 15 |
| Clock | Output | CLKO | PA6 | 4 | 2 | 2 | 3 | 3 | 3 | |
| | Timer0 Clock | T0CKI | PA2 | | | | 7 | 11 | 13 | |
| | Timer1 Clock | T1CKI | PA7 | | | | 2 | 2 | 2 | |
| | OSC + | OSC1 | PA7 | | | | 2 | 2 | 2 | |
| | OSC - | OSC2 | PA6 | 4 | 2 | 2 | 3 | 3 | 3 | |
| Timer1 Gate input | | T1G | PA6 | 4 | 2 | 2 | 3 | 3 | 3 | |
| ISP Debugger | ISP-Data | ISPDAT | PA1 | 1 | 6 | 6 | 8 | 12 | 14 | |
| | ISP-CLK | ISPCLK | PA0 | 6 | 7 | 7 | 9 | 13 | 15 | |
| Reset | Pull-up | /MCLR | PA5 | | | | | | 4 | |
| PC1-INT Edge | | INT | PC1 | 3 | | 5 | | 8 | 10 | |
| PORTA Logic-Changes Interrupt | Input | PA7 | | | | | 2 | 2 | 2 | |
| | | PA6 | | 4 | 2 | 2 | 3 | 3 | 3 | |
| | | PA5 | | | | | | | 4 | |
| | | PA4 | | | | | | 4 | 7 | |
| | | PA3 | | | | | | 10 | 12 | |
| | | PA2 | | | | | 7 | 11 | 13 | |
| | | PA1 | | 1 | 6 | 6 | 8 | 12 | 14 | |
| PA0 | | | 7 | 7 | 9 | 13 | 15 | | | |

| Function | Description | Pin Name | GPIO equiv. | 6 pins | 8(A) pins | 8(B) pins | 10 pins | 14 pins | 16 pins | |
|-------------------------------------|---------------------|-------------------|-------------|--------|-----------|-----------|---------|---------|---------|---|
| Voltage Regulator | High voltage output | V _{REGP} | PA4 | | | | | 4 | 7 | |
| | Low voltage output | V _{REGN} | PC5 | | | | | | 8 | |
| ADC | Input | AN6 | PC2 | | 4 | 4 | 5 | 6 | 6 | |
| | | AN5 | PC1 | 3 | | 5 | | 8 | 10 | |
| | | AN4 | PC0 | | | | | 9 | 11 | |
| | | AN3 | PA3 | | | | | 10 | 12 | |
| | | AN2 | PA2 | | | | 7 | 11 | 13 | |
| | | AN1 | PA1 | 1 | 6 | 6 | 8 | 12 | 14 | |
| | AN0 | PA0 | 6 | 7 | 7 | 9 | 13 | 15 | | |
| | V _{REF+} | VREF | PC0 | | | | | 9 | 11 | |
| Comparator1 | Positive Input | C1IN+ | PA0 | 6 | 7 | 7 | 9 | 13 | 15 | |
| | Inverting Input | C1IN- | PA1 | 1 | 6 | 6 | 8 | 12 | 14 | |
| | Output | C1OUT | PA2 | | | | 7 | 11 | 13 | |
| Comparator2 | Positive Input | C2IN+ | PC0 | | | | | 9 | 11 | |
| | Inverting Input | C2IN- | PC1 | 3 | | 5 | | 8 | 10 | |
| | Output | C2OUT | PC4 | | 5 | | 6 | 7 | 9 | |
| Enhanced Capture/Compare/PWM (ECCP) | Capture/Compare | CCP1 | PC5 | | | | | | 8 | |
| | PWM | P1A | PC5 | | | | | | | 8 |
| | | P1B | PC4 | | 5 | | 6 | 7 | 9 | |
| | | P1C | PC3 | | 3 | 3 | 4 | 5 | 5 | |
| | | P1D | PC2 | | 4 | 4 | 5 | 6 | 6 | |
| | | P1E | PC1 | 3 | | 5 | | 8 | 10 | |
| | | P1F | PC0 | | | | | 9 | 11 | |
| PWM3 | | PWM3 | PC4 | | 5 | | 6 | 7 | 9 | |
| PWM4 | | PWM4 | PC3 | | 3 | 3 | 4 | 5 | 5 | |
| PWM5 | | PWM5 | PC2 | | 4 | 4 | 5 | 6 | 6 | |

Table 1-1 Pin description by functions

2. I/O PORTS

Up to 14 I/O pins are available depending on the types of package. I/O ports are divided into 2 groups: PORTA (8) and PORTC (6) [Table 2-5](#) lists the functions of all I/O pins.

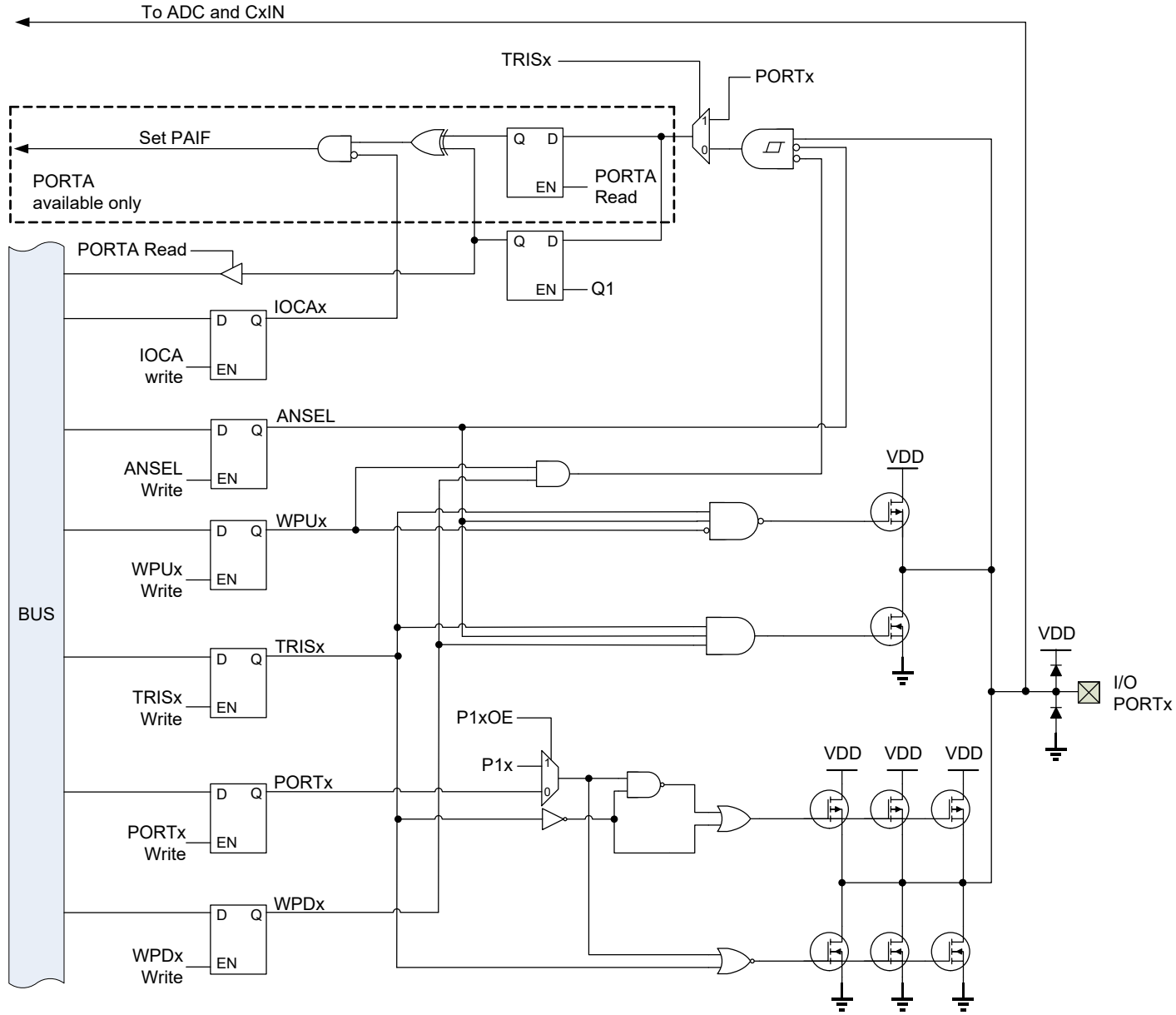


Figure 2-1 PORT block diagram

All I/O pins have the following functions ([Table 2-3](#), [Table 2-4](#)):

- Digital Output
- Digital Input
- Weak Pull-Up
- Weak Pull-Down (PA4, PC1, PC2, PC3)

In addition some I/O's have special functions assigned.

- a. Debugger pins (ISP-Data, ISP-CLK) are hardwired and require no set-up.
- b. Some special functions are configured at the IDE and loaded during BOOT ([Table 2-2](#)):
 - External Clock (OSC1, OSC2)
 - Internal Clock OUT
 - System-Reset (/MCLR)B
- c. All other functions are Instruction Level assigned to the various I/O's. They are divided into 3 categories:
 - a. Digital Output
 - PWM3/4/5
 - Enhanced PWM
 - ECCP output
 - Comparator output CxOUT
 - b. Digital Input
 - Timer0 Clock Input
 - Timer1 Clock Input
 - Timer1 Clock Input
 - ECCP capture input
 - External Edge Interrupt (INT)
 - GPIO Interrupt-on-Change
 - c. Analog Input
 - LVD / BOR
 - ADC
 - V_{REF}
 - Comparator input CxIN+ / CxIN-
 - d. Analog Output
 - Voltage Regulator output (V_{REG})

| Name | ISP Debugger | CLK | ADC | Voltage Regulator or | Comparator or | Interrupt | ECCP / PWM | Digital I/O Pull-Up/Down Open Drain | Source Current (mA) | Sink Current (mA) |
|-------|--------------|--------------|-----------------------|----------------------|---------------|--------------|------------|-------------------------------------|--|-------------------|
| PA0 | CLK | | AN0 | | C1IN+ | √ | | √ / -- | 22 | 19 |
| PA1 | DATA | | AN1 | | C1IN- | √ | | √ / -- | 22 | 19 |
| PA2 | | T0CKI | AN2 | | C1OUT | √ | | √ / -- | 22 | 19 |
| PA3 | | | AN3 | | | √ | | √ / -- | 22 | 19 |
| PA4 | | | | V _{REGP} | | √ | | √ / √ | 22 | 19 |
| PA5 | | | | | | √ + /MCLR | | √ / -- | 22 | 19 |
| PA6 | | output /OSC- | | | | √ | | √ / -- | 22 | 19 |
| PA7 | | T1CKI /OSC+ | | | | √ | | √ / -- | 22 | 19 |
| PC0 | | | AN4 | | C2IN+ | | P1F | √ / -- | 22 | 19 |
| PC1 | | | AN5 | | C2IN- | INT | P1E | √ / √ | 22 | 19 |
| PC2 | | | AN6 | | | | PWM5 / P1D | √ / √ | 22 | 19 |
| PC3 | | | | | | | PWM4 / P1C | √ / √ | 22 | 19 |
| PC4 | | | | | C2OUT | | PWM3 / P1B | √ / -- | 22 | 19 |
| PC5 | | | | V _{REGN} | | | CCP1 / P1A | √ / -- | 22 | 19 |
| Notes | | T1G=PA6 | V _{REF} =PC0 | | | | | | V _{DD} =5, V _{DS} =0.5 | |

Table 2-1 I/O PORT Functions

2.1 Summary of I/O PORT Related Registers

| Name | Function | Default |
|--------|---|----------|
| RDCTRL | <u>READ register when TRISx = 0 (Output enabled)</u> <ul style="list-style-type: none"> Input latch Output latch | Output |
| MCLRE | Reset by External I/O | disabled |
| FOSC | <ul style="list-style-type: none"> LP external oscillator across PA7 (+) and PA6 (-) XT external oscillator across PA7 (+) and PA6 (-) EC external oscillator at PA7 (+), PA6 as I/O INTOSC mode: PA6 output "Instruction Clock", PA7 as I/O INTOSCIO mode: PA7 and PA6 as I/O | INTOSCIO |

Table 2-2 BOOT Level I/O related configurations

| Name | Address | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Reset Value |
|--------|---------|--------------------------------------|--------|-----------------------|-------|-------|-------|-------|-------|-------------|
| ANSEL | 0x91 | ANSEL [7:0] | | | | | | | | 1111 1111 |
| TRISA | 0x85 | TRISA[7:0], PORTA Direction | | | | | | | | 1111 1111 |
| TRISC | 0x87 | - | - | PORTC Direction | | | | | | --11 1111 |
| PORTA | 0x05 | PORTA Output Register | | | | | | | | xxxx xxxx |
| PORTC | 0x07 | - | - | PORTC Output Register | | | | | | --xx xxxx |
| WPUA | 0x95 | PORTA Weak Pull-Up | | | | | | | | 1111 1111 |
| WPUC | 0x88 | - | - | PORTC Weak Pull-Up | | | | | | --00 0000 |
| WPD | 0x89 | - | - | - | WPDA4 | WPDC1 | WPDC2 | WPDC3 | - | ---0 000- |
| IOCA | 0x96 | IOCA[7:0]: PORTA Interrupt-on-Change | | | | | | | | 0000 0000 |
| OPTION | 0x81 | /PAPU | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 |

Table 2-3 Addresses and Reset Values of I/O related registers

| Name | Status | Register | Addr. | Reset | |
|-------|---|---|------------|-------|--------------|
| TRISA | PORTA | <u>PORT Digital Output (Direction)</u> | TRISA[7:0] | 0x85 | RW-1111 1111 |
| TRISC | PORTC | 1 = <u>Disables</u> 0 = Enables (Disables Pull-Up/Down) | TRISC[5:0] | 0x87 | RW-11 1111 |
| ANSEL | 1 = Disables Pull-Up / Pull-Down, Digital Input (8 ADC ports only) 0 = (no action) | | ANSEL[7:0] | 0x91 | RW-1111 1111 |
| /PAPU | 1 = <u>Disables all PORTA Pull-Up</u> 0 = WPUA settings apply | | OPTION[7] | 0x81 | RW-1 |
| WPUA | PORTA | <u>Weak Pull-Up</u> | WPUA[7:0] | 0x95 | RW-1111 1111 |
| WPUC | PORTC | 1 = Enables (PORTA defaults) 0 = Disables (PORTC defaults) | WPUC[5:0] | 0x88 | RW-00 0000 |
| WPDA4 | PORTA | <u>Weak Pull-Down</u> | WPD[4] | 0x89 | RW-0 |
| WPDC | PORTC | 1 = Enables 0 = <u>Disables</u> | WPD[3:1] | | RW-000 |
| PORTA | PORTA | Data Out Register | PORTA[7:0] | 0x05 | RW-xxxx xxxx |
| PORTC | PORTC | | PORTC[5:0] | 0x07 | RW-xx xxxx |

Table 2-4 Instruction Level I/O related registers

2.2 Configuring the I/O

For each PORT, configures the following four modules according to their functions ([Table 2-5](#))

- Weak Pull-Up
- Weak Pull-Down (PA4, PC1, PC2, PC3)
- Digital Input
- Digital Output

| Functions | Digital Input | Pull-Up / Pull-Down | Digital Output | Settings |
|----------------------|---------------|---------------------|----------------|-----------------------------------|
| ISP-DATA | On | Off | On | (hardwired, instructions ignored) |
| ISP-CLK | On | Off | Off | (hardwired, instructions ignored) |
| /MCLR | On | Pull-Up | Off | (BOOT set, instructions ignored) |
| CLOCK OUT | (don't care) | Off | On | (BOOT set, instructions ignored) |
| OSC+ (EC) | On | (optional) | Off | (BOOT set, instructions ignored) |
| OSC+ / OSC- (LP, XT) | Off | Off | Off | (BOOT set, instructions ignored) |
| ADC | Off | Off | Off | TRISx = 1; ANSELx = 1 |
| V _{REF} | Off | Off | Off | TRISx = 1; ANSELx = 1 |
| Comparator input | Off | Off | Off | TRISx = 1; ANSELx = 1 |
| Comparator output | On | Off | On | TRISx = 0 |
| Timer0 Clock | On | (optional) | Off | TRISx = 1 |
| Timer1 Clock | On | (optional) | Off | TRISx = 1 |
| Timer1 Gate | On | (optional) | Off | TRISx = 1 |
| Timer3/4/5 Clock | On | (optional) | Off | TRISx = 1 |
| Interrupt-on-Change | On | (optional) | Off | TRISx = 1 |
| PC1-INT | On | (optional) | Off | TRISx = 1 |
| Digital input | On | (optional) | Off | TRISx = 1 |
| PWM | On | Off | On | TRISx = 0 |
| ECCP capture | On | (optional) | Off | TRISx = 1 |
| ECCP compare/PWM | On | Off | On | TRISx = 0 |
| Voltage regulator | (don't care) | Off | Off | VREG_OE = 1 |
| Digital Output | On | Off | On | TRISx = 0 |

Table 2-5 Instruction Level I/O Configuration Flags and Registers

Notes:

1. TRISx = 0: "Digital Output" enabled, "Pull-Up / Pull-Down" disabled (WPDx, WPUx ignored).
2. TRISx = 1: "Digital Output" disabled.
3. ANSELx = 1: "Pull-Up", "Pull-Down", "Digital Input" disabled (WPDx and WPUx ignored).
4. Only way to turn off "Digital Input" by instructions is "ANSELx = 1".
5. "/PAPU = 1" disables "Weak Pull-Up" for all PAX. There are no equivalent bits for PCx.
6. /MCLR enabled: PA5's Weak Pull-Up enabled (WPUA[5] ignored); PORTA[5] read "0".
7. Writing the PORTx Data Out registers will output the logic level to the corresponding I/O. Write operations are 'Read-Modify-Write' operations, meaning PORTx latch (output or input) are read first, then modified and written back, as up to 8 I/O share the same register.
8. Digital Output and Digital Input can be inclusive. Some applications need both enabled simultaneously.
9. The IDE can globally choose which PORT latch (output or input) to READ when TRISx = 0.
10. In Full-Reset or System-Reset PORTx will not reset, but TRISx will reset to "1", disabling output.
11. Weak Pull-Up enabled, Weak Pull-Down disabled when they are opened simultaneously.

See [Section 9](#) "Interrupts" for setting up PC1-INT and PORTA Interrupt-on-Change.

3. POWER-ON-RESET (POR)

During Power-On, V_{DD} increases from below the Power-On-Reset Voltage (V_{POR}) to above it. V_{DD} may not have completely discharged to 0V when the CPU is Power-On again.

1. The CPU is in a Full-Reset state when V_{DD} is below V_{POR} .
 - a. All Calibrated Data registers are not reset. Special Function Registers (SFR) are in Reset, except TMR0, PORTx, Z, HC, C, FSR, INDF, ADRESL, ADRESH, TMRxL, TMRxH, CCP1L, CCP1H and SRAM (see [Section 17](#) Special Function Registers). Registers not reset, such as SRAM, will hold their values until V_{DD} drops below 0.6V (typical). Data of those registers with V_{DD} below 0.6V are undetermined.
 - b. Program Counter = 0x00, Instruction Register = "NOP", Stack Pointer = "TOS" (Top of Stack).
2. BOOT commences when V_{DD} raises above V_{POR} .
3. Instruction execution begins with Program Counter = 0x00 after BOOT completion.

V_{POR} is ~1.6V at 25°C (typical), increasing to ~1.9V at -40°C. For $V_{DD} \geq V_{POR}$, the CPU can function at a reduced speed of 8 MHz / 2T. POR alone can safeguard against a low V_{DD} failure, giving a self-regulated wider V_{DD} operating range with temperature. This is important for battery-powered system as the CPU can function down even to ~1.6V at typical battery operating environments, greatly extending useful battery life.

Notes:

1. V_{POR} is not configurable.
2. The POR circuit is always on and will perform a Power-On-Reset any time V_{DD} voltage is below V_{POR} , not just during Power-On.

3.1 BOOT Sequence

| Name | Functions | default |
|---------|--|----------|
| PWRTEB | Additional ~64ms delay after BOOT load | disabled |
| CSUMENB | Array Checksum test | disabled |

Table 3-1 BOOT configurations

There are 2 BOOT configurations. Their values are set at the IDE, not by instructions. during BOOT:

1. CPU Idles for ~4ms.
2. The BOOT Level registers are loaded from the non-volatile memory. It takes ~24us. These registers are pre-set at the IDE and not affected by instructions.
3. If Power-On-Timer (PWRT) is enabled, the CPU will idle for ~64ms.
4. If the Checksum (CSUM) is enable, it will do a Checksum of the whole program array.
 - a. If Checksum fail, it will BOOT again, starting with the ~4ms idle time.
 - b. If Checksum pass, instructions execution will begin as long as there are no other Reset conditions.

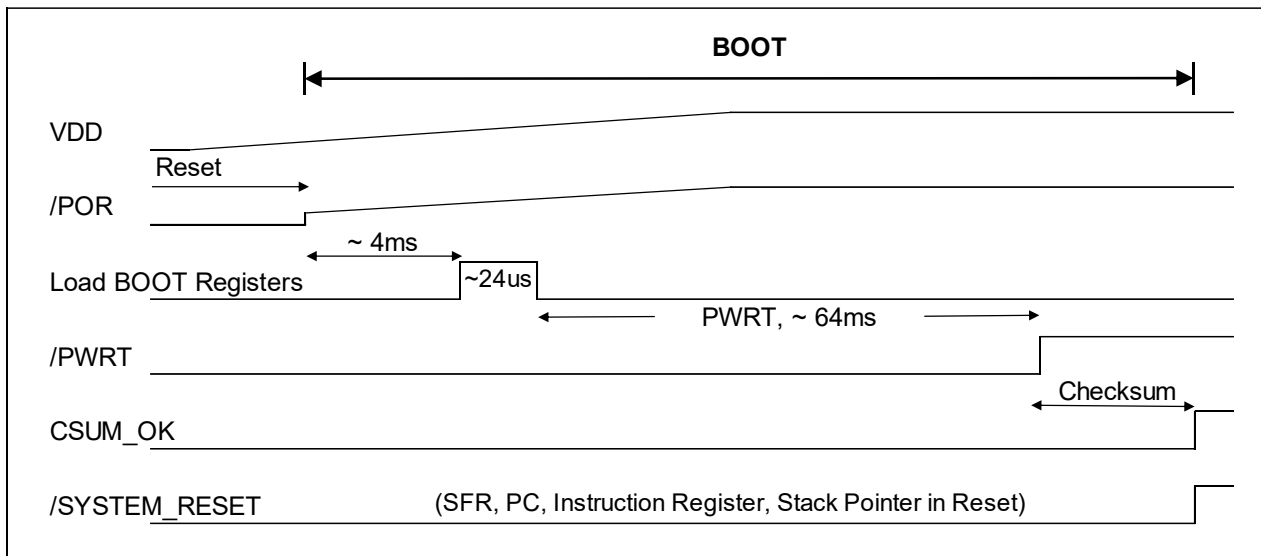


Figure 3-1 Power-On Sequence with PWRT and Checksum enabled

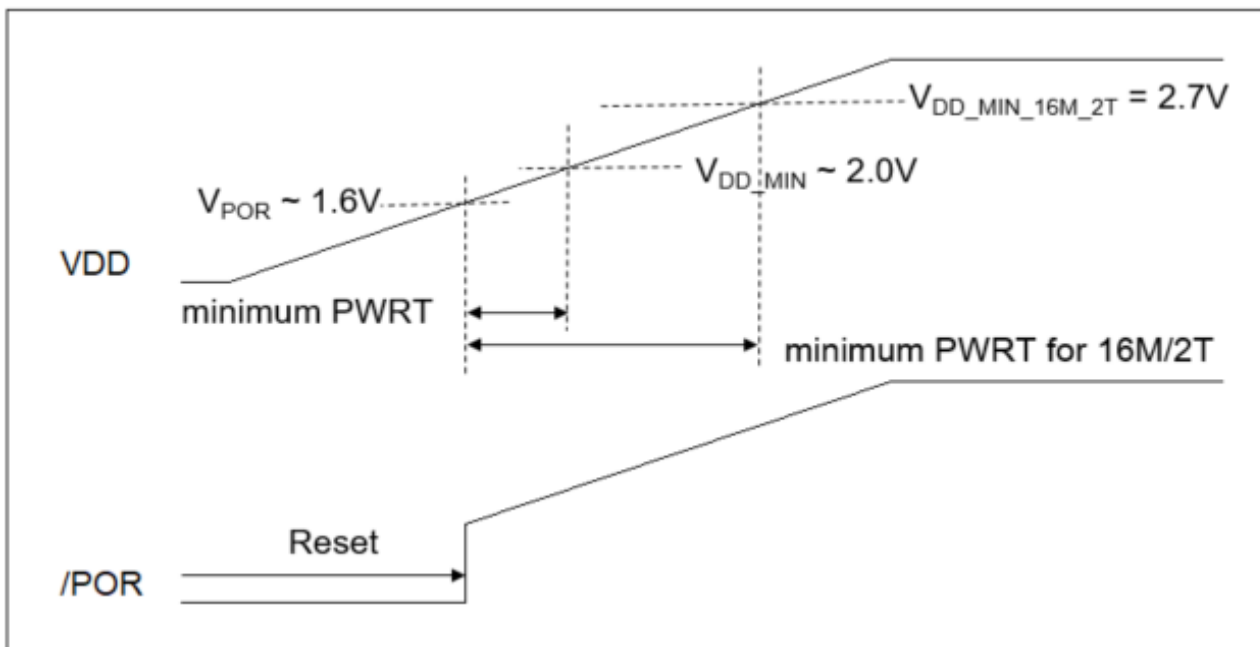


Figure 3-2 Minimum required PWRT during Power-On

V_{DD} must be higher than 2.5V by the end of BOOT if the CPU is to run at 16MHz / 2T. The total BOOT time can increase from ~4ms to ~68ms by enabling the PWRT, giving more time for the power system to stabilize.

Enables LVR with V_{BOR} ≥ 2.5V for operation at 16MHz / 2T. LVR can be set to instruction controlled to monitor V_{DD} sporadically, instead of always on (see “LVREN”, “SLVREN”) to reduce power consumption.

Notes:

1. V_{DD} should not rise too slowly. C_{VDD} ≥ 22 μF is discouraged.
2. V_{DD} capacitor of 1 to 10μF is preferred. C_{VDD} < 1μF capacitor may be too small for EFT considerations.
3. If a delay in startup is acceptable, enables PWRT and CSUM to improve CPU stability.

4. SYSTEM-RESET

System-Reset differs from POR in that it is not a Full-Reset. Depending on the trigger type and configurations, CPU may or may not BOOT. BOOT will wait ~4ms, reload the BOOT registers, and further delay system start by ~64ms if PWRT is enabled. In a System-Reset

- Registers reset in POR are reset, except BOOT registers.
- Program Counter = 0x00, Instruction Register = "NOP", Stack Pointer = "TOS" (Top of Stack).

The following 4 events besides debugger OCD can be configured to trigger a System-Reset:

1. Brown-Out (LVR / BOR) – always BOOT.
2. Illegal Instructions – BOOT if "IRBTE" is set.
3. Watch-Dog Timer (WDT) – BOOT if CPU not in SLEEP.
4. External I/O (/MCLR) – BOOT if "MRBTE" is set.

Note: If a longer system restart time is acceptable, enable BOOT will improve system stability.

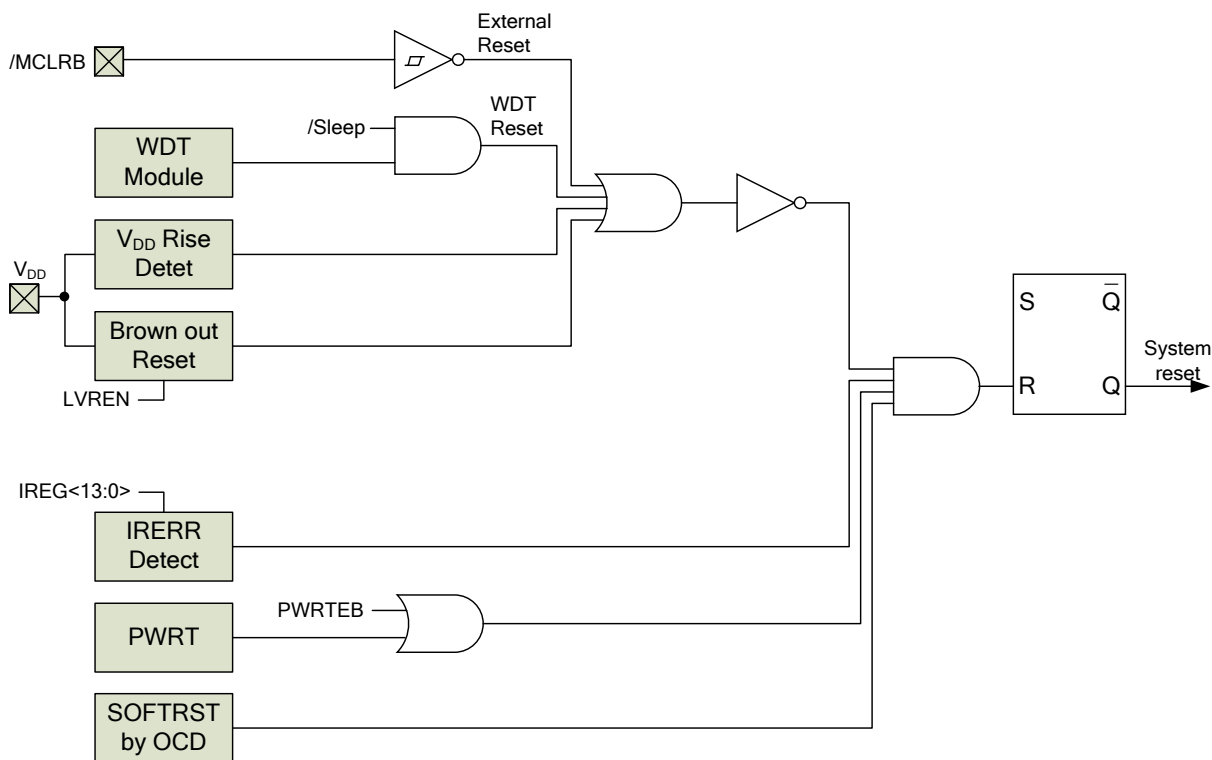


Figure 4-1 Reset circuit block diagram

4.1 Summary of SYSTEM-RESET Related Registers

Most settings for System-Reset are configured at the IDE, and cannot be changed by instructions.

| Name | Functions | default |
|-------|--|----------------|
| LVRS | <u>7 V_{BOR} Voltage levels (V):</u> 2.0 / 2.2 / 2.5 / 2.8 / 3.1 / 3.6 / 4.1 | 2.0 |
| LVREN | <u>LVR</u> <ul style="list-style-type: none"> • Enabled • Disabled • Enabled except in SLEEP • Instruction controlled (SLVREN) | disabled |
| WDTE | <u>WDT</u> <ul style="list-style-type: none"> • Enabled (overrides instructions disable) • Instruction controls (SWDTEN) | SWDTEN control |
| MCLRE | Reset by External I/O | disabled |

Table 4-1 BOOT Level RESET related configurations

4.2 Brown-Out Reset (LVR / BOR)

Brown-Out occurs when V_{DD} falls below a pre-configured Brown-Out Voltage (V_{BOR}) for a time longer than T_{BOR}. T_{BOR} takes 3 to 4 LIRC clock cycles (~94 – 125µs, LIRC will turn on automatically if not already). CPU System-Reset as long as V_{DD} ≤ V_{BOR}. Once V_{DD} > V_{BOR} CPU will BOOT.

While V_{POR} is fixed, V_{BOR} can be set to 2.0, 2.2, 2.5, 2.8, 3.1, 3.6, 4.1V (see “LVRS” in [Table 4-1](#)).

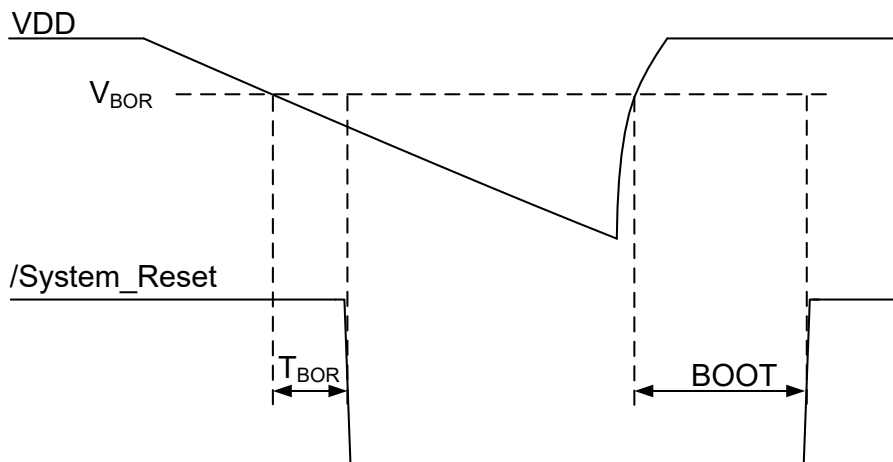


Figure 4-2 LVR BOOT Timing Diagram

LVR function can have four different settings configured by BOOT (see “LVREN” in [Table 4-1](#)).

1. LVR enabled.
2. LVR disabled.
3. LVR enabled, except in SLEEP.

4. Let instructions enable or disable LVR (SLVREN, see [Table 4-2 Instruction Level LVR registers](#))

Note: SLVREN can be cleared by any system reset except BOR

5.).

Note: LVR can be instructions disabled in SLEEP to reduce power consumption. The CPU should wake up and enable LVR periodically to monitor V_{DD} if system V_{DD} is unstable.

| Name | Status | Register | Addr. | Reset |
|--------|--|------------|-------|-------|
| SLVREN | Applies only when LVREN cedes control to SLVREN 1 = Enables LVR 0 = Disables LVR | MSCKCON[4] | 0x1B | RW-0 |

Table 4-2 Instruction Level LVR registers

Note: SLVREN can be cleared by any system reset except BOR

4.3 Illegal Instruction Reset

There are many reasons a CPU fetches an instruction incorrectly, with interference and V_{DD} instability the most common. When such an event occurs System-Reset and/or BOOT.

4.4 Watch Dog Timer, WDT Reset

WDT overflows during SLEEP will result in a Wake-Up.

WDT overflows not during SLEEP will trigger a System-Reset. The IDE preset if a BOOT follows (see “WDTE” in [Table 4-1](#)). This can reset a hanged CPU. Clear WDT from time to time in the program to avoid false reset.

For details on WDT operation and setting see [Section 7.1](#) Watch Dog Timer (WDT).

4.5 External System-Reset /MCLR

The CPU can be reset by a low voltage applied to the /MCLR (PA5) pin if so configured by BOOT. The /MCLR pin is usually soft pullup to V_{DD} with a resistor instead of directly, as shown in [Figure 4-3](#). The external RC network also provides glitches filtering and over-current protection.

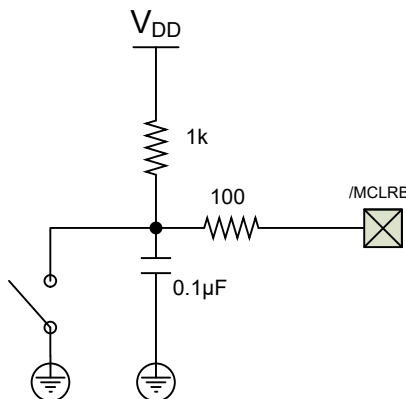


Figure 4-3 /MCLR reset circuit

4.6 Detecting the Type of Reset Last

Four status flags /POR, /BOR, Time Out (/TF), Power Down (/PF) together can trace the type of last System-Reset, except between “/MCLR System-Reset during normal operation” and “Illegal Instruction Reset”. Use instructions to set the flags to “1”. In a Reset, the corresponding flag(s) latches to “0”.

| Reset Source | /POR | /BOR | /TF | /PF |
|--|---------|-----------|--------------------------|-----------|
| | PCON[1] | PCON[0] | STATUS[4] | STATUS[3] |
| | 0x8E | | 0x03, 0x83, 0x103, 0x183 | |
| POR | 0 | (unknown) | 1 | 1 |
| LVR | - | 0 | 1 | 1 |
| WDT overflows while not in SLEEP (Reset) | - | - | 0 | - |
| WDT overflows while in SLEEP (Resume) | - | - | 0 | 0 |
| /MCLR Reset during SLEEP | - | - | 1 | 0 |
| /MCLR Reset during normal operation | - | - | - | - |
| Illegal Instruction | - | - | - | - |
| On-Chip Debugger (OCD) | - | - | - | - |

Table 4-3 Reset Related Status Flags (“-“ no change)

5. LOW VOLTAGE DETECT / COMPARATOR (LVD)

LVD works similarly to a LVR except for the followings:

- None of the control and setting parameters are set by BOOT. They are set by instructions.
- It will write LVDW instead of /BOR.
- The input to the LVD module can be configured to V_{DD}. The latter allows the LVD to function as a single input comparator to one of the six LVDL levels.
- Debouncing Time (T_{LVD}) is much shorter than T_{BOR} at 3 – 4 HIRC cycles (~94 – 125µs, LIRC turns on automatically if not already so).

5.1 Summary of LVD Related Registers

| Name | Status | Register | Addr. | Reset |
|--------|---|-----------|-------|--------|
| LV DEN | <u>LVD</u> 1 = Enables 0 = <u>Disables</u> | PCON[3] | 0x8E | RW-0 |
| LV DL | <u>V_{LVD-REF}</u> 000 = <u>Reserved</u> 001 = Reserved 010 = 2.0 011 = 2.4 100 = 2.8 101 = 3.0 110 = 3.6 111 = 4.0 | PCON[6:4] | | RW-000 |
| LV DW | <u>LVD triggered?</u> 1 = Yes (no latch) 0 = No | PCON[2] | | RO-x |

Table 5-1 Instruction Level LVD Settings and Flags

6. OSCILLATORS and SYSClk

Instruction chooses whether SysClk is the internal oscillator HIRC, internal oscillator LIRC, or one of the three external oscillators (EC, LP, XT, see “SCS” in [Table 6-2](#)). If external oscillator is chosen, BOOT level “FOSC” ([Table 6-1](#)) will determine which one of the three external oscillators is used. Instructions also select the frequency step down divider for internal oscillator (see IRCF in [Table 6-2](#)). SysClk is used to derive the Instruction Clock:

$$\text{Instruction Clock} = \text{SysClk} / N; N = 2 \text{ for } 2T, 4 \text{ for } 4T.$$

The pin assignments for external clock inputs and Instruction Clock output are set by BOOT (see FOSC).

Timers and ADC have their own oscillators. More than one oscillator can be active simultaneously.

Oscillators will turn on automatically when the Timers using them are enabled. They will remain active as long as the corresponding Timers are active. The oscillators can be configured to shutdown or be active in SLEEP. By keeping the corresponding oscillator active in SLEEP, ADC, Timer functions and PWM can also be active in SLEEP.

As instructions are halted in SLEEP, so will Instruction Clock. Any peripherals using Instruction Clock will also halt in SLEEP.

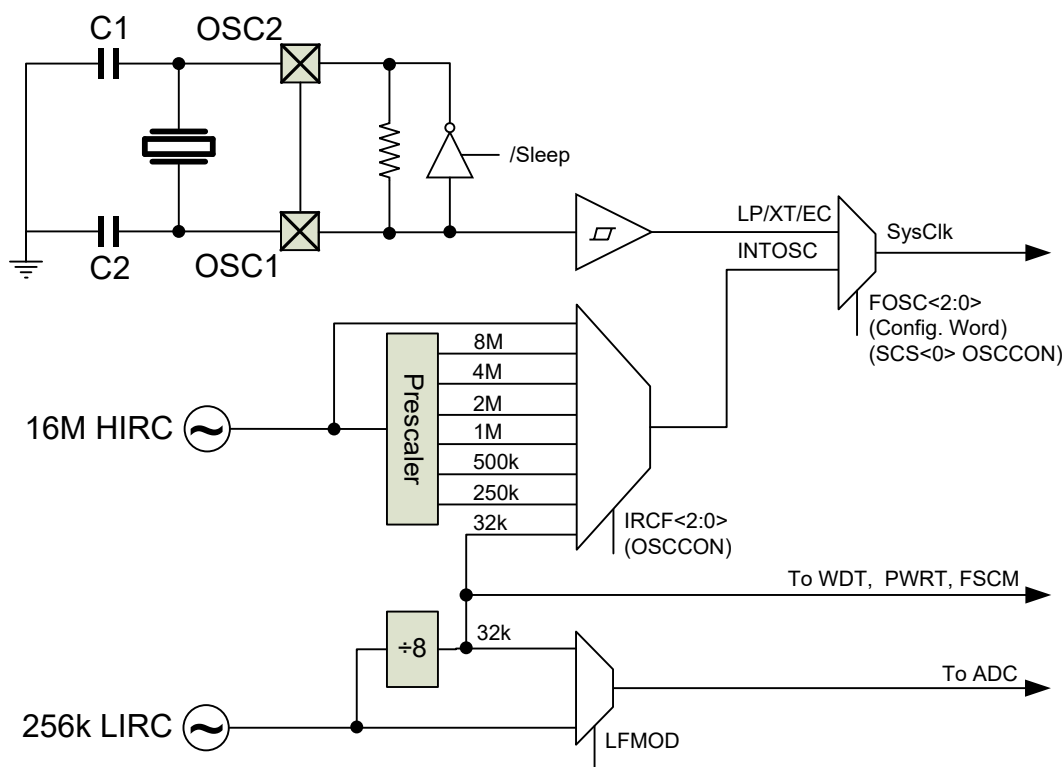


Figure 6-1 Clock source block diagram for SysClk

6.1 Summary of Oscillator Modules Related Registers

| Name | Functions | default |
|-------|---|----------|
| FOSC | <ul style="list-style-type: none"> LP external oscillator across PA7 (+) and PA6 (-) XT external oscillator across PA7 (+) and PA6 (-) EC external oscillator at PA7 (+), PA6 as I/O pin INTOSC mode: PA6 output "Instruction Clock", PA7 as I/O pins INTOSCIO mode: PA7 and PA6 as I/O pins | INTOSCIO |
| IESO | <u>Two-speed Startup for XT and LP</u> <ul style="list-style-type: none"> Enabled Disabled | Enabled |
| FCMEN | <u>Fail-Safe Clock Monitor</u> <ul style="list-style-type: none"> Enabled Disabled | Enabled |
| TSEL | <u># of SysClk per Instruction (2T or 4T)</u> <ul style="list-style-type: none"> 2 (Instruction Clock = SysClk/2) 4 (Instruction Clock = SysClk/4) | 2 |

Table 6-1 BOOT Level FOSC and 2-speed Start-Up configurations

| SysClk Source | | configuration | | | | |
|---------------|------|----------------------|-------------|-----------|---------|---|
| | | SCS | IRCF | LFMOD | OST | |
| | | OSCCON[0] | OSCCON[6:4] | OSCCON[7] | (fixed) | |
| | | 0x8F | | | | |
| | | RW-0 | RW-101 | RW-0 | | |
| External | EC | 0 | - | - | - | |
| | XT | 0 | - | - | 1,024 | |
| | LP | 0 | - | - | 32,768 | |
| Internal | HIRC | 16 MHz | 1 | 111 | - | - |
| | | 8 MHz | 1 | 110 | - | - |
| | | 4 MHz | 1 | 101 | - | - |
| | | 2 MHz | 1 | 100 | - | - |
| | | 1 MHz | 1 | 011 | - | - |
| | | 500 kHz | 1 | 010 | - | - |
| | LIRC | 256 kHz ¹ | 1 | 000 | 1 | - |
| | | 32 kHz ² | 1 | 000 | 0 | - |

Table 6-2 Instruction Level SysClk source setup

¹ 256 kHz LIRCs used only for ADC (see ADCS and LFMOD in [Table 12-2](#)).

² Sysclk source (IRCF=000), LIRC and HIRC Cross Calibration, PWRT and FSCM all use the 32kHz LIRC, regardless of the LFMOD value.

| Name | Status | Register | Addr. | Reset |
|--------|---|--------------|-------------------|--------|
| OSTS | <u>Oscillator Start-Up Time-out (latched)?</u> 1 = Running from the external clock (start-up successful) 0 = Running from the internal oscillator | OSCCON[3] | 0x8F | RO-x |
| HTS | <u>HIRC ready (latched)?</u> 1 = Yes 0 = <u>No</u> | OSCCON[2] | | RO-0 |
| LTS | <u>LIRC ready (latched)?</u> 1 = Yes 0 = <u>No</u> | OSCCON[1] | | RO-0 |
| CKMAVG | <u>4x averaging for LIRC and HIRC Cross Calibration</u> 1 = Enables 0 = <u>Disables</u> | MSCKCON[2] | 0x1B | RW-0 |
| CKCNTI | <u>Initiate LIRC and HIRC Cross Calibration</u> 1 = Start 0 = <u>Finished (auto-cleared)</u> | MSCKCON [1] | | RW-0 |
| SOSCPR | <u>LIRC Period Calibrated by # of HIRC clocks</u> | SOSCPR[11:0] | 0x1D[3:0] 0x1C | RW-FFF |

Table 6-3 Oscillators Control/Status

| Name | Status | Register | Addr. | Reset |
|---------|--|-----------|-----------------------|-------|
| GIE | Global Interrupt 1 = Enables (PEIE, CKMEAIE, OSFIE applies) 0 = Global Disables (Wake-Up not affected) | INTCON[7] | 0x0B 0x8B 0x10B | RW-0 |
| PEIE | Master Peripheral Interrupt 1 = Enables (CKMEAIE, OSFIE applies) 0 = <u>Disables</u> (no Wake-Up) | INTCON[6] | | RW-0 |
| CKMEAIE | LIRC Calibration Completed Interrupt 1 = Enables 0 = <u>Disabled</u> (no Wake-Up) | PIE1[6] | 0x8C | RW-0 |
| OSFIE | External Oscillator Failed Interrupt 1 = Enables 0 = <u>Disabled</u> (no Wake-Up) | PIE1[2] | | RW-0 |
| CKMEAIF | LIRC Calibration completed? 1 = Yes (latched) 0 = <u>No</u> | PIR1[6] | 0x0C | RW-0 |
| OSFIF | External Oscillator Failed interrupt? 1 = Yes (latched) 0 = <u>No</u> | PIR1[2] | | RW-0 |

Table 6-4 Oscillators Interrupt enable/Status

6.2 Internal Clock Modes (HIRC and LIRC)

Internal high frequency clock (HIRC) is factory calibrated to 16 MHz @ 2.5V/25°C. Typical die to die variation is < ±2.0% at 2.5 – 5.5V, 25°C. The typical temperature variation from -40 – +85 °C is < ±3.0%.

HIRC is calibrated at the wafer level. Packaging may cause the HIRC frequency to drift. There is an option at the downloader to re-calibrate the HIRC.

Internal low frequency clock (LIRC) is factory calibrated to 32 kHz. Typical die to die variations is <±9.0% at 2.5 – 5.5V, 25°C. The temperature variation from -40 – +85 °C is < ±2.0%.

LIRC and HIRC can be used to cross calibrate each other – A build in hardware uses Timer2 to measure the number of Instruction Clocks (set SysClk to HIRC at 16MHz) in one LIRC period (32 kHz). Since LIRC has a lower temperature coefficient, the HIRC can be calibrated to the LIRC when the temperature fluctuates, thereby achieving the same ±2.0% temperature coefficient.

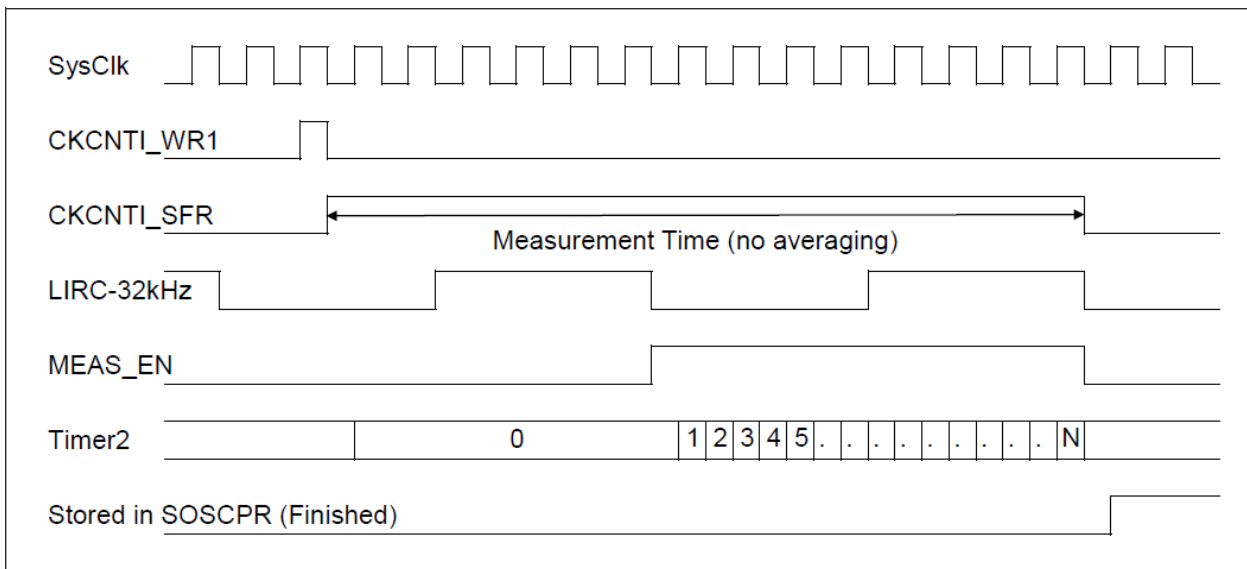


Figure 6-2 Single measurement timing diagram

To enable LIRC and HIRC Cross Calibration:

1. Set IRCF = 111, SCS = 1 ; select SysClk at 16MHz HIRC (other settings will have a lower accuracy).
2. Set CKMAVG = 1 ; 4 times averaging, choose 0 for no averaging.
3. Set TMR2ON = 1 ; enable Timer2.
4. Set CKCNTI = 1 ; start calibration, automatically Timer2 prescaler = 1, postscaler = 1, T2CKSRC = SysClk for 2T; SysClk/2 for 4T
5. At the end of the calibration “CKCNTI =0”, “CKMEAIF = 1” automatically.
6. Measured value is stored at SOS CPR;
7. LIRC is 32kHz and CPU is running at 16MHz / 2T, the ideal matching number is 500.

Notes:

- Do not write SOS CPRH/L during LIRC and HIRC Cross Calibration.

- Timer2 cannot be used by other peripherals during LIRC and HIRC Cross Calibration.
- LIRC and HIRC Cross Calibration is incompatible with Single Step Debugger mode.

6.3 External Clock Modes (EC / LP / XT)

6.3.1 EC mode

External digital signal connected to OSC1 is the clock source (OSC2 is available for I/O). There is no set up or transition time delay when EC is used for SysClk after a POR or a wake-up from sleep.

6.3.2 LP and XT modes

A quartz crystal resonator or ceramic resonator is connected between OSC1 and OSC2 in LP or XT modes.

LP Oscillator mode has the lowest gain setting and current consumption of the three modes (EC, LP and XT). This mode is designed to drive only 32.768 kHz tuning-fork type crystals (watch crystals).

XT Oscillator mode selects the highest gain setting of the internal inverter-amplifier.

After a BOOT or a Wake-Up from Sleep, program execution is suspended during OST counting if the clock source is XT or LP mode. This allows the XT or LP clock to stabilize. OST counts 1,024 or 32,768 counts of OSC1 (+ve terminal of the crystal input) for XT and LP respectively. For a 32.768 kHz tuning-fork type crystals the OST time is at least 1 second.

- Notes: WDT is held in cleared until OST finished counting. Do not write WDTCON / OPTION during OST counting, otherwise unexpected behavior will occur.

Two-Speed Clock Start-up (see “IESO” in [Table 6-1](#)) allows instructions execution while OST counts, using the internal oscillator INTOSC as SysClk. It removes the external oscillator start-up time from the time spent awake and can reduce the overall power consumption, especially in cases of frequent SLEEP mode usage. The CPU wakes up from Sleep, performs a few instructions using the INTOSC as SysClk and return to Sleep without having to wait for the primary oscillator to become stable.

Note: Two-Speed Start-up is disabled for EC mode, as the oscillator does not require stabilization time.

Two Speed Start-up sequence

1. After a BOOT or Wake-up from Sleep.
2. INTOSC is used as SysClk for Instructions execution until OST time out.
3. SysClk is held low from the falling edge of INTOSC until the falling edge of the new clock (LP or XT mode).
4. SysClk switches to the external clock source.

The Oscillator Start-up Time-out Status (OSTS) indicates whether the SysClk is running from the external clock source or from the internal clock source. This is an indirect way to find out if the Oscillator Start-up Timer (OST) has timed out for the LP or XT mode when the Two-Speed Clock Start-up mode is on.

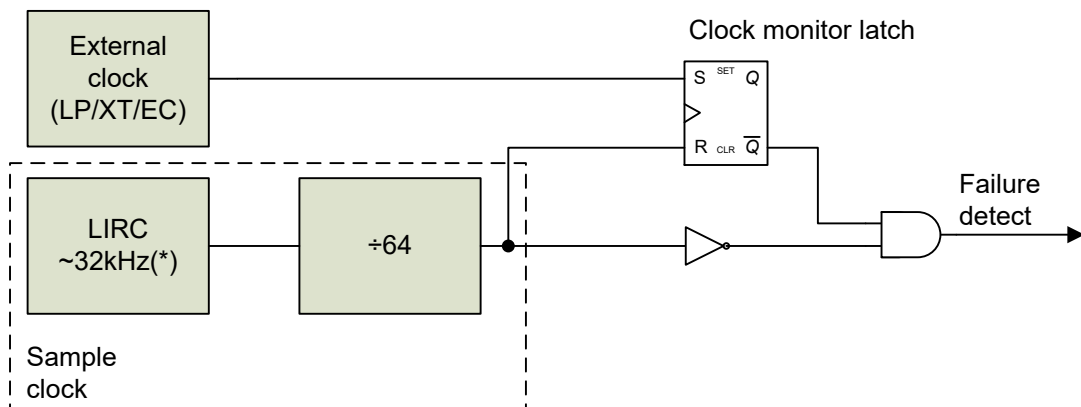
Executing a SLEEP instruction will abort the OST, and OSTS will remain “0”.

Fail-Safe Clock Monitor (FSCM, enabled by “FCMEN”, see **Table 6-1**) allows the device to continue operating should the external oscillator fails. The FSCM can detect oscillator failure any time after the Oscillator Start-up Timer (OST) has expired. The FSCM is applicable to all external oscillator modes (EC, LP and XT). It is recommended that FSCM be enabled if an external oscillator is used.

An external oscillator is considered fail if it oscillates at ~1 kHz or below. A sample clock is generated by dividing the LIRC by 64. The external clock sets a latch on each falling edge of the external clock. The sample clock clears the latch on each rising edge of the sample clock. A failure is when an entire half-cycle of the sample clock elapses without the primary clock goes low.

When the external clock fails, the FSCM switches the device clock to an internal clock source and sets OSFIF. Setting this flag will generate an interrupt if OSFIE is also set. The device hardware can then take steps to mitigate the problems that may arise from a failed clock. The SysClk will continue to be sourced from the internal clock source until the device hardware successfully restarts the external oscillator.

The internal clock source chosen by “FSCM” is determined by “IRCF”. This allows the internal oscillator to be configured before a failure occurs.



Note: LFMOD does not affect the sample clock.

Figure 6-3 FSCM block diagram

The Fail-Safe condition is cleared after a Reset, executing a SLEEP instruction or toggling the SCS. When SCS is toggled, OST is restarted. While OST is running, the device continues to operate from INTOSC. When OST times out, the Fail-Safe condition is cleared and the device will be operating from the external clock source. The Fail-Safe condition must be resolved before the OSFIF flag is cleared.

Note: Any automatic clock switch, which may occur from Two-Speed Start-up or Fail-Safe Clock Monitor, will not update SCS. The program can monitor OSTs to determine the current SysClk source.

6.4 HIRC, LIRC and EC inter-switching

Figure 6-4 shows the timing during inter-switching. If either HIRC or LIRC is shutdown prior to switching (to save power) there is an extra oscillator setup delay time, HTS and LTS indicate the status of the corresponding oscillator respectively.

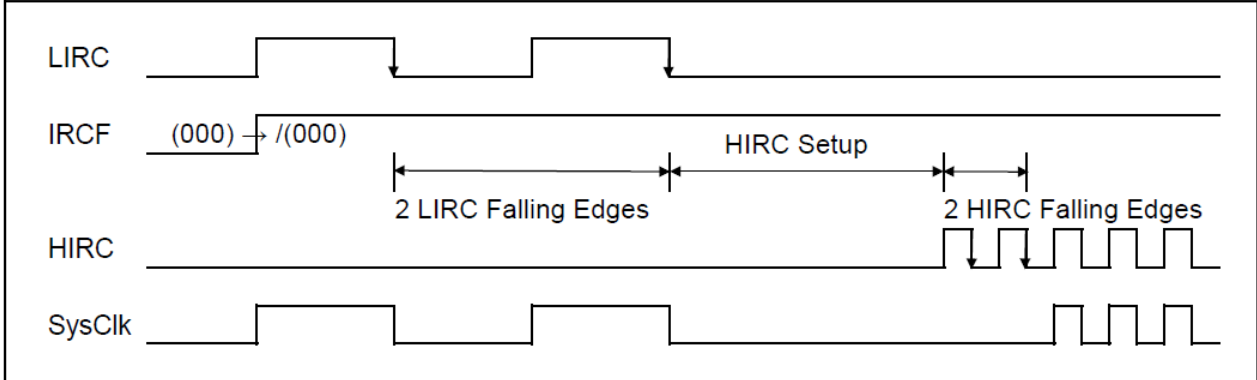


Figure 6-4 Switching from LIRC to HIRC (same principle applies switching among EC, LIRC, HIRC)

7. TIMERS and PWMx

There are 7 Timers including the Watch Dog Timer (WDT).

| | WDT | Timer0 | Timer1 | Timer2 | Timer3/4/5 |
|------------------|---|--|---|--|--|
| Prescaler (bit) | – | 8 (WDT shared) | 3 (1x, 2x, 4x, 8x) | 4 (1x, 4x, 16x) | 7 (1x, 2x, 4x, 8x, 16x, 32x, 64x, 128x) |
| Counter (bit) | 16 | 8 | 16 | 8 | 12 |
| Postscaler (bit) | 7 (Timer0 shared) | – | – | 4 (1 – 16x) | – |
| Clock Sources | <ul style="list-style-type: none"> • <u>LIRC</u> | <ul style="list-style-type: none"> • <u>Instruction Clock</u> • PA2/T0CKI (transition counter) | <ul style="list-style-type: none"> • <u>Instruction Clock</u> • LP • PA7/T1CKI (rising edge counter) | <ul style="list-style-type: none"> • <u>2x Instruction Clock</u> • 2x HIRC | <ul style="list-style-type: none"> • HIRC • <u>2x Instruction Clock</u> • PA2/T0CKI (transition counter) • PA7/T1CKI (rising edge counter) |

Table 7-1 Timers’ Resources

Notes: If a Timer’s clock is not the instruction Clock, set “TMRxON = 0” before changing TMRx.

Any Timer enabled will turn on its clock source automatically. Instruction Clock is disabled at SLEEP so it cannot be used for WDT. When LP or XT Oscillator is selected, FOSC must be configured correspondingly or to INTOSCIO mode, otherwise the oscillator is off and no counting will occur.

WDT postscaler and Timer0 prescaler shares the same hardware. The hardware is Instruction Level assigned to one, but not both. The Timer not assigned the scaler will have a scaler value of “1”.

In a POR or System-Reset, all Timers’ counter, prescaler, postscaler are reset except Timer0 counter. The followings will also reset a Timer’s counter and scaler(s):

| | WDT | Timer0 | Timer1 | Timer2 | Timer3/4/5 |
|------------|---|---|---|--|---|
| Prescaler | – | <ul style="list-style-type: none"> • TMR0 write • PSA switching | <ul style="list-style-type: none"> • TMR1ON = 0 • TMR1L/H write | <ul style="list-style-type: none"> • LIRC and HIRC Cross Calibration start • T2CON, TMR2L/H write • Any Reset | <ul style="list-style-type: none"> • TMRxL/H write |
| Counter | <ul style="list-style-type: none"> • WDT, OST overflow • Enters/Exits SLEEP • CLRWDT • WDTCON write | <ul style="list-style-type: none"> • Timer0 overflows | <ul style="list-style-type: none"> • TMR1 = PR1 (matches, special event trigger) • ECCP trigger special event | <ul style="list-style-type: none"> • TMR2 = PR2 (matches) | <ul style="list-style-type: none"> • TMRx = PRx (matches in BUZZER mode) |
| Postscaler | <ul style="list-style-type: none"> • All Above except WDTCON write • PSA switching | – | – | <ul style="list-style-type: none"> • T2CON, TMR2L/H write • Any Reset | – |

Table 7-2 Events resetting a Timer’s Counter and Scaler(s)

7.1 Watch Dog Timer, WDT

WDT is used to “Wake-Up from SLEEP” or “System-Reset if the CPU stalls”. WDT counts the number of clock cycles to a pre-set number until overflow.

- In SLEEP mode, a WDT overflow will trigger a Wake-up. The CPU will resume operation from where it is before SLEEP. This is not an Interrupt nor System-Reset event.
- In non-SLEEP mode, a WDT overflow will trigger a System-Reset (see [Section 4 System-Reset](#)).

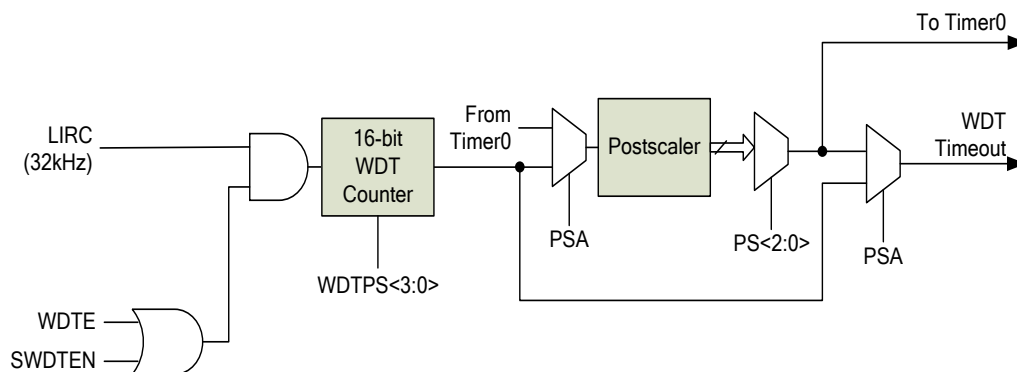


Figure 7-1 Block diagram of WDT

The WDT will overflow after a WatchDog-Time: $\text{WDT-Period} \times \text{WDT-Postscaler} / \text{WDT Clock Frequency}$.

For a given Clock Source, WatchDog-Time step doubles successively due to the binary nature of the WDT Postscaler. Using LIRC as clock source, the maximum settable time before WDT overflows is

$$2^{16} \times 2^7 / 32\text{kHz} = \sim 262 \text{ seconds.}$$

7.1.1 Summary of WDT Related Registers

| Name | Status | Register | Addr. | Reset | | | | |
|--------------|---|----------------|------------------|-------------|------|--------|----------------|----|
| WDTPS | <u>WDT Period</u> | | 0x18 | RW-0100 | | | | |
| | 0000 = 32 | 0111 = 4,096 | | | | | | |
| | 0001 = 64 | 1000 = 8,192 | | | | | | |
| | 0010 = 128 | 1001 = 16,384 | | | | | | |
| | 0011 = 256 | 1010 = 32,768 | | | | | | |
| | 0100 = <u>512 (Default)</u> | 1011 = 65,536 | | | | | | |
| | 0101 = 1,024 | 11xx = 65,536 | | | | | | |
| 0110 = 2,048 | | | | | | | | |
| SWDTEN | 1 = WDT Enables 0 = <u>WDT Disables</u> (WDTE = 0) | WDTCON[0] | | RW-0 | | | | |
| PSA | 1 = <u>Scalar assigned as WDT Postscalar</u> 0 = Scalar assigned as Timer0 Prescalar | OPTION[3] | | RW-1 | | | | |
| PS | | WDT Postscalar | Timer0 Prescalar | OPTION[2:0] | 0x81 | RW-111 | | |
| | 000 | | 1 | | | | 2 | |
| | 001 | | 2 | | | | 4 | |
| | 010 | | 4 | | | | 8 | |
| | 011 | <u>(PSA=1)</u> | 8 | | | | <u>(PSA=0)</u> | 16 |
| | 100 | | 16 | | | | 32 | |
| | 101 | | 32 | | | | 64 | |
| | 110 | | 64 | | | | 128 | |
| | 111 | | <u>128</u> | | | | <u>256</u> | |
| xxx | <u>(PSA =0)</u> | 1 | <u>(PSA =1)</u> | 1 | | | | |

Table 7-3 Instruction Level WDT Related Registers

| Name | Functions | default |
|------|---|----------------|
| WDTE | <u>WDT</u> <ul style="list-style-type: none"> Enabled (overrides Instructions disable) <u>Instruction controlled (SWDTEN)</u> | SWDTEN control |

Table 7-4 BOOT Level WDT Selectors

7.1.2 Setting up and using the WDT

WDTE (BOOT Level) and/or SWDTEN (Instruction Level) enable the WDT. A WDT triggered Reset will also BOOT

WDT clock source is 32kHz LIRC, WDTPS, PSA and PS together set the Postscalers. Clock source will turn on automatically when the WDT using it is enabled, and will remain active in SLEEP mode.

To stop a WDT overflow, the WDT must be cleared before time expires. Refer to [Table 7-2](#) for events that will clear the WDT. Counting continues after WDT is cleared.

7.1.3 Switching scaler between Timer0 and WDT

As a result of having the same scaler assigned to either Timer0 or the WDT, it is possible to generate an unintended System-Reset when switching scaler between Timer0 and WDT.

When switching scaler assignment from Timer0 to WDT, the instruction sequence below must be followed.

```

BANKSEL TMR0           ; Can skip if already in TMR0 bank
CLRWDW                 ; Clear WDT
CLRR TMR0              ; Clear TMR0 and scaler
BANKSEL OPTION
BSR OPTION, PSA        ; Select WDT

LDWI b'11111000'      ; Mask scaler bits (PS2-0)
ANDWR OPTION, W
IORWI b'00000101'     ; Set WDT scaler bits to 32 (or any value desired)
STR OPTION
    
```

When switching scaler assignment from WDT to Timer0, the instruction sequence below must be followed.

```

CLRWDW                 ; Clear WDT and scaler
BANKSEL OPTION
LDWI b'11111000'      ; Mask TMR0 select and scaler bits (PSA, PS2-0)
ANDWR OPTION, W
IORWI b'00000011'     ; Set Timer0 scale to 16 (or any value desired)
STR OPTION
    
```

7.2 TIMER0

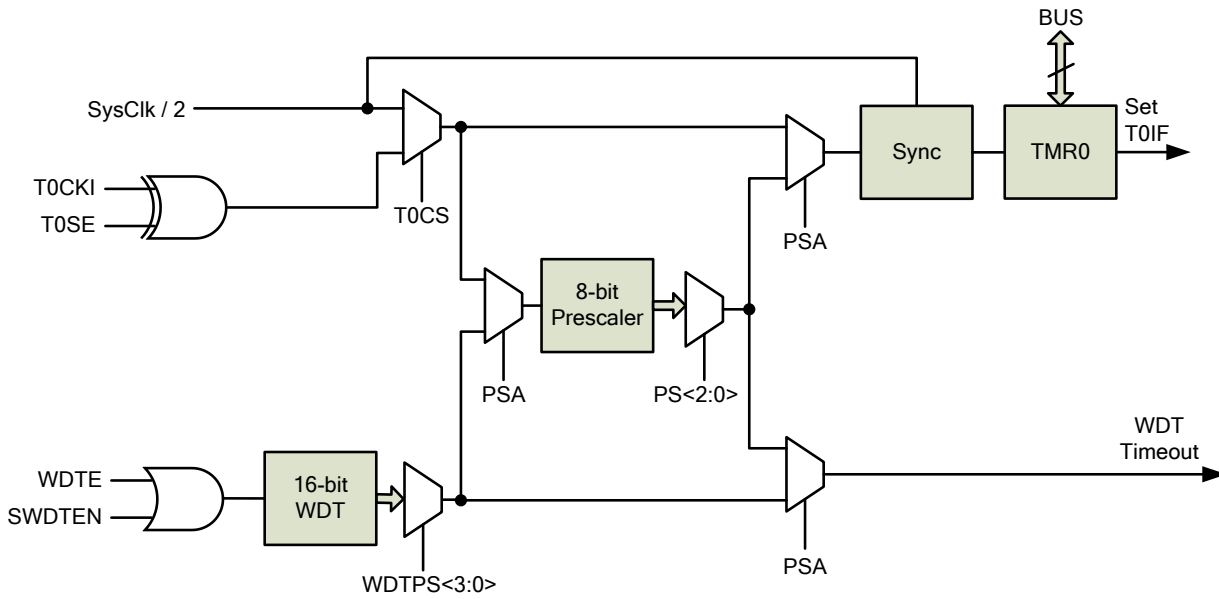


Figure 7-2 Block diagram of Timer0

Timer0 is used to count transitions at an I/O “PA2–T0CKI”, or as a timer to keep time (Clock source is Instruction clock).

Timer0 counts and overflows upon reaching a time = $TMR0[7:0] * Timer0_Prescaler$

An Interrupt flag (T0IF) is set. Depends on the enable controls (T0IE and GIE)

Notes:

1. Timer0 stops for two instruction cycles immediately following writing TMR0.
2. Timer0 will be disabled in SLEEP mode and will retain the value before entering SLEEP.
3. If Timer0 is used to count T0CKI, there are minimum period, high and low pulse width requirements relative to Timer0. However unless T0CKI is very fast and T_{T0CK} is very slow, the restrictions will usually be satisfied.

| T0CKI | Minimum | Units | Conditions |
|-------------------------|----------------------------------|-------|--|
| High or Low Pulse Width | $0.5 * T_{T0CK} + 20$ | ns | no Prescaler |
| | 10 | ns | with Prescaler |
| Period | $maximum(20, (T_{T0CK}+40)/N)$ | ns | N = 1, 2, 4, ..., 256 (with Prescaler) N = 1 (no Prescaler) |

4. See [Section 7.1.3](#) regarding “Switching scaler between Timer0 and WDT modules”

7.2.1 Summary of Timer0 Related Registers

| Name | Status | Register | Addr. | Reset |
|-----------|---|----------------|------------|------------------|
| T0CS | <u>Timer0 Input Source</u> 1 = PA2/T0CKI (Counter) 0 = Instruction Clock (Timer) | OPTION[5] | 0x81 | RW-1 |
| T0SE | <u>Counter Trigger</u> 1 = <u>Falling Edge</u> 0 = Rising Edge | OPTON[4] | | RW-1 |
| PSA | 1 = <u>Scalar assigned as WDT Postscalar</u> 0 = Scalar assigned as Timer0 Prescalar | OPTION[3] | | RW-1 |
| PS | | WDT Postscalar | | TIMER0 Prescalar |
| | 000 | 1 | 2 | |
| | 001 | 2 | 4 | |
| | 010 | 4 | 8 | |
| | 011 | (PSA=1) 18 | (PSA=0) 16 | |
| | 100 | 16 | 32 | |
| | 101 | 32 | 64 | |
| 110 | 64 | 128 | | |
| 111 | 128 | 256 | | |
| xxx | (PSA =0) 1 | (PSA =1) 1 | | |
| TMR0[7:0] | Timer0 Count Value | TMR0[7:0] | 0x01 | RW-xxxx xxxx |

Table 7-5 Instruction Level Timer0 Related Control Registers

| Name | Status | Register | Addr. | Reset |
|------|--|-----------|---------------|-------|
| GIE | Global Interrupt 1 = Enables (T0IE applies) 0 = <u>Global Disables</u> (Wake-Up not affected) | INTCON[7] | 0x0B | RW-0 |
| T0IE | Timer0 Overflow Interrupt 1 = Enables 0 = <u>Disables</u> (no Wake-Up) | INTCON[5] | 0x8B 0x10B | RW-0 |
| T0IF | Timer0 Overflow Interrupt? 1 = Yes (latched) 0 = <u>No</u> | INTCON[2] | | RW-0 |

Table 7-6 Timer0 Interrupt Enable and Status Bits

7.3 TIMER1

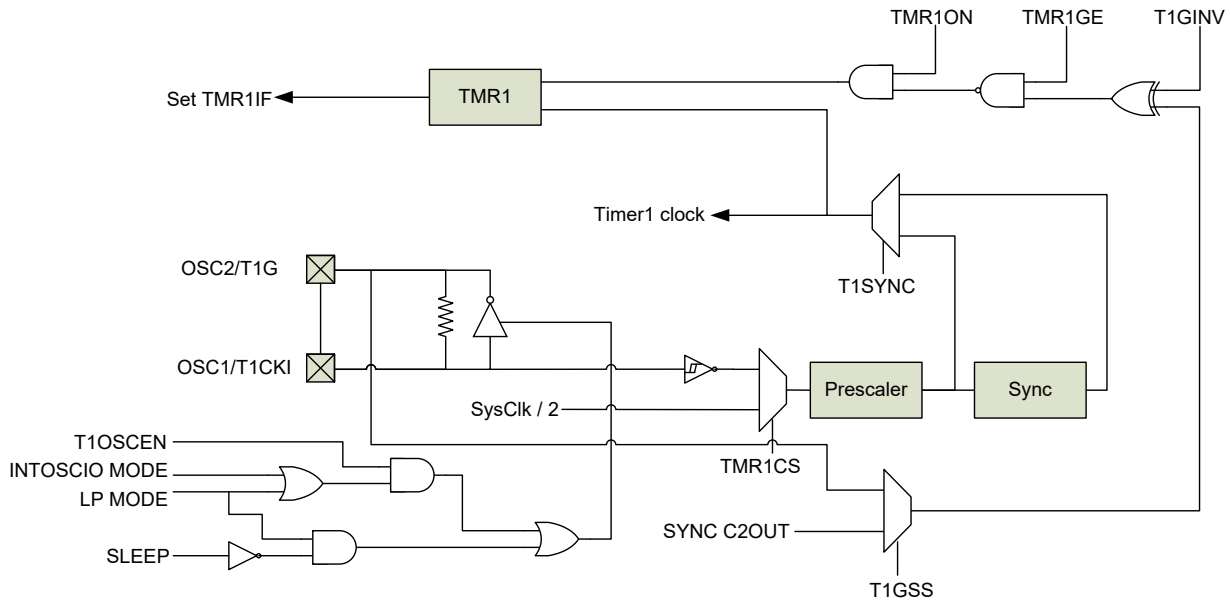


Figure 7-1 Block diagram of Timer1

Timer1 is used to count rising edge at an I/O “PA7–T1CKI” (Synchronization/ Asynchronization), or as a timer to keep time (Clock source is Instruction clock/ LP oscillator). Timer1 can also used for gate mode (Timer1 gate source is software configurable to be the /T1G pin or the output of Comparator C2), or used as time base of Enhanced Capture /Compare/PWM Module (See [Section 10](#)).

Timer1 counts and overflows upon reaching a time = TMR1 * Timer1_Prescaler

An Interrupt flag (TMR1IF) is set. Depends on the enable controls (TMR1IE, GIE and PEIE) it may result in an AWAKE from SLEEP and/or Interrupt.

Note:

1. In Counter mode, a falling edge must be register by the counter prior to the first incrementing rising edge after any one or more of the following condition:
 - Timer1 Timer1 enabled after POR reset
 - Timer1 is disabled(TMR1ON=0) when T1CKI is high then Timer1 is enabled(TMR1ON=1) when T1CKI is low.
 - Write to TMR1H or TMR1L
2. If T1SYNC, TMR1CS, TMR1ON is set, the external clock input is not synchronized. The timer increments asynchronously to the internal phase clocks. If external clock source is selected (T1OSCEN = 1) then the timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake-up the processor. Otherwise Timer1 will be disabled in SLEEP mode and will retain the value before entering SLEEP.
3. If Timer1 is used to count T1CKI, there are minimum period, high and low pulse width requirements relative to Timer1. However unless T1CKI is very fast and T_{T1CK} is very slow, the restrictions will usually be satisfied.

| T1CKI | Mode | Minimum | Units | Conditions |
|-------------------------|------------------|-----------------------------|-------|---------------------------------|
| High or Low Pulse Width | Synchronization | $(T_{sysclk} + 20) / N$ | ns | N = 1, 2, 4, 8 (with Prescaler) |
| | Asynchronization | maximum (10 , 30 / N) | ns | |
| Period | Synchronization | $2 * (T_{sysclk} + 20) / N$ | ns | |
| | Asynchronization | maximum (20 , 60 / N) | ns | |

7.3.1 Summary of Timer1 Related Registers

| Name | Status | Register | Addr. | Reset |
|---------------------|---|------------|-------|------------------|
| T1GINV | <u>Gate Invert bit</u> 1 = Timer1gate is active high 0 = <u>Timer1 gate is active low</u> | T1CON[7] | 0x10 | RW-0 |
| TMR1GE | <u>Timer1 Gate Enable bit (TMR1ON = 1)</u> 1 = Timer1 is on if Timer 1 gate is active 0 = <u>Timer1 is on</u> | T1CON[6] | | RW-0 |
| T1CKPS | <u>Timer1 prescaler</u> 00 = <u>1</u> 10 = 4 01 = 2 11 = 8 | T1CON[5:4] | | RW-00 |
| T1OSCEN | <u>LP Oscillator Enable Control bit</u> 1 = Enables (*) 0 = <u>Disables</u> (*)FOSC in LP or INTOSCIO mode, and TMR1CS = 1, Otherwise the oscillator will not active | T1CON[3] | | RW-0 |
| T1SYNC ¹ | <u>Timer1External Clock Input Synchroniaztion Control bit</u> 1 = Asynchronization 0 = <u>Synchronization</u> Note: TMR1CS = 1, this bit is active | T1CON[2] | | RW-0 |
| TMR1CS | <u>Timer1 clock source</u> 1 = External PA7/T1CKI(rising edge) or LP oscillator 0 = <u>Internal instruction clock</u> | T1CON[1] | | RW-0 |
| TMR1ON | Timer1 1 = Enables 0 = <u>Disables</u> | T1CON[0] | | RW-0 |
| T1GSS | Timer1 Gate Source 1 = T1G pin (pin should be configured as digital input) 0 = Comparator C2 output | CMCON1[1] | | 0x1A |
| C2SYNC | <u>Comparator C2 Output Synchronization bit</u> 1 = Output is synchronized with falling edge of Timer1 clock 0 = <u>Output is asynchronous</u> | CMCON1[0] | RW-0 | |
| TMR1L | Least Significant Byte of the 16-bit TIMER1 Register | TMR1L[7:0] | 0x0E | RW- 0000 0000 |
| TMR1H | Most Significant Byte of the 16-bit TIMER1 Register | TMR1H[7:0] | 0x0F | |

Table 7-1 Instruction Level Timer1 Related Control Registers

¹ When switching from synchronous to asynchronous operation, it is possible to skip an increment. When switching from asynchronous to synchronous operation, it is possible to produce an additional increment.

| Name | Status | Register | Addr. | Reset |
|--------|-------------------------------|-----------|-----------------------|-------|
| GIE | Global Interrupt | INTCON[7] | 0x0B 0x8B 0x10B | RW-0 |
| PEIE | Master Peripheral Interrupt | INTCON[6] | | RW-0 |
| TMR1IE | Timer1 matched PR1 Interrupt | PIE1[0] | 0x8C | RW-0 |
| TMR1IF | Timer1 matched PR1 Interrupt? | PIR1[0] | 0x0C | RW-0 |

Table 7-7 Timer1 Interrupt Enable and Status Bits

7.3.2 R/W operation of Timer1 register

TMR1H and TMR1L cannot be READ or WRITE simultaneously. The following Read and Write sequences must be followed:

- To READ TMR1, in order to avoid the timer overflow or carry out of TMR1L to TMR1H between the reads, it is recommended to set “TMR1ON =0” first, then read TMR1L and TMR1H.
- To WRITE TMR1, in order to avoid write contentain, it is recommended to set “TMR1ON =0” first, then write TMR1L and TMR1H.

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read(take care of hardware).

7.3.3 Timer1 Gate

Timer1 gate source is software configurable to be the /T1G pin or the output of Comparator C2. (see T1GSS, [Table 7-1](#)), and Timer1 gate can be inverted (see T1GINV, [Table 7-1](#)). This feature can simplify the software for a Δ-Σ A/D converter and many other application.

Note:

1. When the LP oscillator is configured as Timer1 clock source, T1G always output “1”, thus do not use it to gate control Timer1.
2. It is recommended to synchronize Comparator with Timer1 by setting the C2SYNC bit when the comparator is used as the Timer1 gate source. This ensures Timer1 does not miss an increment if the comparator changes during an increment.

7.4 TIMER2

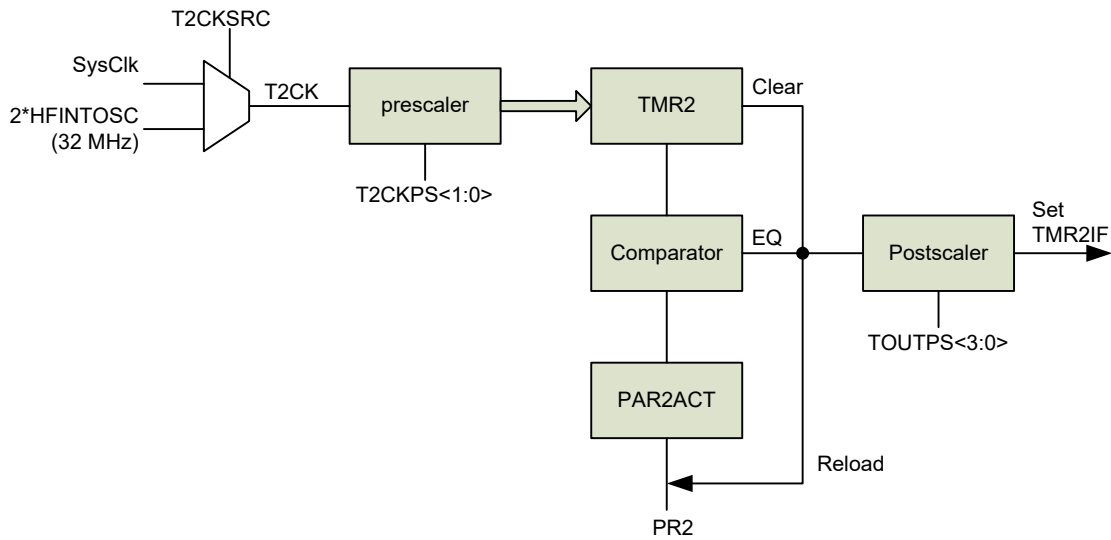


Figure 7-3 Timer2 block diagram

Timer2 is used as a timer. It is also for generating the enhanced PWM (without Postscaler, see [Section 10](#) PWM), and for LIRC and HIRC Cross Calibration counting (CKCNTI=1). Counter matches and postscaler overflows function can be used simultaneously.

Timer2 clock is fed into Timer2 Prescaler (options of 1, 4 or 16). The Prescaler output increments TMR2 from 0x00 until it matches PR2. Upon matching:

1. TMR2 resets to 0x00 on the next increment cycle
2. Timer2 Postscaler increments.
3. Timer2 overflows when Timer2 post-scaler output is equal to the post-scaler setting (1, 2 15 or 16).
4. An Interrupt flag TMR2IF is set to 1. Depends on the enable controls (GIE, PEIE and TMR2IE) it may result in Interrupt.

Notes:

1. TMR2 is not cleared when T2CON0 is written.
2. Both TMR2 and PR2 are R/W. They are 0x0000 and 0xFFFF respectively when reset.
3. Timer2 will be disabled in SLEEP mode and will retain the value before entering SLEEP.

7.4.1 Summary of Timer2 Related Registers

| Name | Status | Register | Addr. | Reset | | |
|---------|--|------------------------------------|------------|-----------|-----------------|-----------|
| TOUTPS | <u>Timer2 Post-scaler</u> | | 0x12 | RW-0000 | | |
| | 0000 = 1 | 0100 = 5 | | | 1000 = 9 | 1100 = 13 |
| | 0001 = 2 | 0101 = 6 | | | 1001 = 10 | 1101 = 14 |
| | 0010 = 3 | 0110 = 7 | | | 1010 = 11 | 1110 = 15 |
| | 0011 = 4 | 0111 = 8 | 1011 = 12 | 1111 = 16 | | |
| TMR2ON | Timer2 | 1 = Enables 0 = <u>Disables</u> | T2CON[2] | RW-0 | | |
| T2CKPS | Timer2 Prescaler | 00 = 1 01 = 4 1x = 16 | T2CON[1:0] | RW-00 | | |
| T2CKSRC | <u>Timer2 Clock Source</u> | | MSCKCON[5] | 0x1B | | |
| | 1 = 2 x HIRC (32MHz, Effective only in ECCP mode) 0 = <u>2 x Instruction Clock</u> | | | | | |
| TMR2 | TMR2 count register | | TMR2[7:0] | 0x11 | RW-0000 0000 | |
| PR2 | PR2 period register | | PR2[7:0] | 0x92 | RW-1111 1111 | |

Table 7-8 Instruction Level Timer2 Related Control Registers

| Name | Status | Register | Addr. | Reset | |
|--------|-------------------------------|---|-----------|-----------------------|------|
| GIE | Global Interrupt | 1 = Enables (PEIE, TMR2IE applies) 0 = <u>Global Disables</u> (Wake-Up not affected) | INTCON[7] | 0x0B 0x8B 0x10B | RW-0 |
| PEIE | Master Peripheral Interrupt | 1 = Enables (TMR2IE applies) 0 = <u>Disables</u> (no Wake-Up) | INTCON[6] | | RW-0 |
| TMR2IE | Timer2 matched PR2 Interrupt | 1 = Enables 0 = <u>Disables</u> (no Wake-Up) | PIE1[1] | 0x8C | RW-0 |
| TMR2IF | Timer2 matched PR2 Interrupt? | 1 = Yes (latched) 0 = <u>No</u> | PIR1[1] | 0x0C | RW-0 |

Table 7-9 Timer2 Interrupt Enable and Status Bit

7.5 TIMER3/4/5 and PWM3/4/5

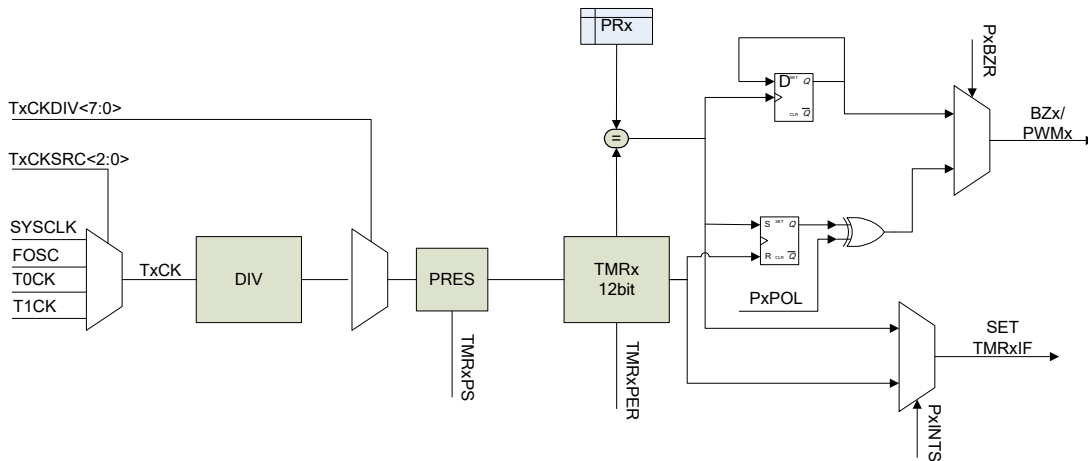


Figure 7-2 Timerx/PWMx (x = 3, 4, 5) block diagram

Timer3/4/5 is used to count transitions at an I/O “PA2–T0CKI” or “PA7–T1CKI”, or as a timer to keep time (Clock source is Instruction clock). And it can generate 3 independent Duty Cycles PWMx with selectable polarity.

PxCKSRC chooses the Timerx/PWMx clock source, and the clock source is optional 1-256 frequency division (see TxCKDIV), The divided clock is fed into 7-bit Prescaler (options of 1-128). The Prescaler output increments TMRx

Timerx can configure Overflow or match interrupt (see “PxINTS”).

Overflow: overflow time = $TMRx[11:0] * Timerx_prescaler$, the effective bit of TMRx specified by PxPER

Match: TMRx increase to setting time = $PRx * Timerx_prescaler / (Timerx_divider)$, TMRx matches PRx.

When Timerx overflow or TMRx matches PRx, Interrupt flag TMRxIF will be set, TMRx will returns to 0x000 after a count clock. Depends on the enable controls (GIE, PEIE and TMRxIE) it may result in an AWAKE from SLEEP and/or Interrupt.

Note:

1. HIRC will be enabled automatically when HIRC is selected as Timerx/PWMx clock source except in SLEEP mode;
2. Both TMRx and PRx are R/W. PRx is 0xFFFF when reset., TMRx is uncertain, it should be cleared by software or write other initial value.
3. If “PxCKSRC = 010 / 011”, the I/O “PA2–T0CKI” or “PA7–T1CKI” is selected, then the Timerx/PWMx/BUZZERx will continue to run during Sleep, which will wake-up the processor. Otherwise Timer1 will be disabled in SLEEP mode and will retain the value before entering SLEEP.
4. If Timerx is used to count T0CKI or T1CKI, the requirement of T0CKI/T1CKI see [Section 7.2](#) and [Section 7.3](#).

7.5.1 Summary of Timer3/4/5b Related Registers

| Name | Status | Register | Addr. | Reset |
|----------------------|--|--------------|-------|-----------------|
| P3PER | <u>TMRx period select bit(PxINTS = 0)</u> ² 000 = <u>4 bits</u> 100 = 9 bits 001 = 5 bits 101 = 10 bits 010 = 6 bits 110 = 11 bits 011 = 8 bits 111 = 12 bits | PWM3CR0[6:4] | 0x10F | RW-000 |
| P4PER | | PWM4CR0[6:4] | 0x115 | |
| P5PER | | PWM5CR0[6:4] | 0x11B | |
| P3CKSRC | <u>TIMERx / PWMx clock select bits</u> 000 = <u>2x instruction clock / (TxCKDIV + 1)</u> 001 = HIRC / (TxCKDIV + 1) 010 = T0CKI / (TxCKDIV + 1) 011 = T1CKI / (TxCKDIV + 1) 100 = HIRC / (TxCKDIV + 1), PWMx output low 101 = HIRC / (TxCKDIV + 1), PWMx output high 110 = HIRC / (TxCKDIV + 1), PWMx modulates PxCK according to high pulse (see Table 7-4) 111 = HIRC / (TxCKDIV + 1), PWMx modulates PxCK according to high pulse (see Table 7-4) | PWM3CR0[3:1] | 0x10F | RW-000 |
| P4CKSRC | | PWM4CR0[3:1] | 0x115 | |
| P5CKSRC | | PWM5CR0[3:1] | 0x11B | |
| P3BZR | <u>PWM / BUZZER select</u> 1 = BUZZER output 0 = <u>PWM output</u> | PWM3CR0[0] | 0x10F | RW-0 |
| P4BZR | | PWM4CR0[0] | 0x115 | |
| P5BZR | | PWM5CR0[0] | 0x11B | |
| P3EN | <u>TIMERx / PWMx Operating Mode</u> 1 = PWM / BUZZER Mode 0 = <u>Timer Mode</u> | PWM3CR1 [7] | 0x110 | RW-0 |
| P4EN | | PWM4CR1 [7] | 0x116 | |
| P5EN | | PWM5CR1 [7] | 0x11C | |
| P3POL | <u>PWMx Output Polarity Select</u> 1 = Active-low 0 = <u>Active-high</u> | PWM3CR1[6] | 0x110 | RW-0 |
| P4POL | | PWM4CR1[6] | 0x116 | |
| P5POL | | PWM5CR1[6] | 0x11C | |
| TMR3PS | <u>PWMx Prescaler</u> 000 = <u>1</u> 100 = 16 001 = 2 101 = 32 010 = 4 110 = 64 011 = 8 111 = 128 | PWM3CR1[5:3] | 0x110 | RW-000 |
| TMR4PS | | PWM4CR1[5:3] | 0x116 | |
| TMR5PS | | PWM5CR1[5:3] | 0x11C | |
| TMR3ON | <u>TIMERx</u> 1 = Enables 0 = <u>Disables</u> | PWM3CR1[2] | 0x110 | RW-0 |
| TMR4ON | | PWM4CR1[2] | 0x116 | |
| TMR5ON | | PWM5CR1[2] | 0x11C | |
| T3CKDIV ³ | TMR3 clock frequency is $F_{T3CK}/(T3CKDIV+1)$ (see "P3CKSRC") | T3CKDIV[7:0] | 0x111 | RW-0000 0000 |

² Set TMRxON = 0 before write PxPER

³ The divider is automatically cleared when writing to the TxCKDIV register.

| Name | Status | Register | Addr. | Reset |
|----------------------|--|--------------|-------|-----------------|
| T4CKDIV ³ | TMR4 clock frequency is $F_{T4CK}/(T4CKDIV+1)$ (see "P4CKSRC") | T4CKDIV[7:0] | 0x117 | RW-0000 0000 |
| T5CKDIV ³ | TMR5 clock frequency is $F_{T5CK}/(T5CKDIV+1)$ (see "P5CKSRC") | T5CKDIV[7:0] | 0x11D | RW-0000 0000 |
| TMR3L | TIMER3 Counter Low Byte | TMR3L[7:0] | 0x10C | RW-xxxx xxxx |
| TMR3H | Upper 4 bits of TIMER3 Counter | TMR3H[7:4] | 0x10D | RW-xxxx |
| PR3L | PR3 Register Low Byte | PR3L[7:0] | 0x10E | RW-1111 1111 |
| PR3H | Upper 4 bits of PR3 | TMR3H[3:0] | 0x10D | RW-1111 |
| TMR4L | TIMER4 count result low Byte | TMR4L[7:0] | 0x112 | RW-xxxx xxxx |
| TMR4H | upper 4 bits of TIMER4 count result | TMR4H[7:4] | 0x113 | RW-xxxx |
| PR4L | Match register PR4 of the PWM4 low Btyle | PR4L[7:0] | 0x114 | RW-1111 1111 |
| PR4H | Upper 4bits of PR4 | TMR4H[3:0] | 0x113 | RW-1111 |
| TMR5L | TIMER5 count result low byte | TMR5L[7:0] | 0x118 | RW-xxxx xxxx |
| TMR5H | upper 4 bits count result of TIMER5 | TMR5H[7:4] | 0x119 | RW-xxxx |
| PR5L | match register PR5 of the PWM5 low Btyle | PR5L[7:0] | 0x11A | RW-1111 1111 |
| PR5H | upper 4 bits of PR5 | TMR5H[3:0] | 0x119 | RW-1111 |

Table 7-2 Instruction Level Timer3/4/5 Related Control Registers

| Name | Status | Register | Addr. | Reset |
|--------|---|------------|-----------------------|-------|
| GIE | <u>Global Interrupt</u> 1 = Enables (PEIE, TMRxIEapplies) 0 = <u>Global Disables</u> (Wake-Up not affected) | INTCON[7] | 0x0B 0x8B 0x10B | RW-0 |
| PEIE | <u>Master Peripheral Interrupt</u> 1 = Enables (TMRxIE applies) 0 = <u>Disables</u> (no Wake-Up) | INTCON[6] | | RW-0 |
| P3INTS | <u>Timerx Interrupt select bit</u> 1 = TMRx matches PRx 0 = TMRx overflow | PWM3CR0[7] | 0x10F | RW-0 |
| P4INTS | | PWM4CR0[7] | 0x115 | RW-0 |
| P5INTS | | PWM5CR0[7] | 0x11B | RW-0 |
| TMR3IE | <u>Timerx Interrupt</u> 1 = Enables 0 = <u>Disables</u> (no Wake-Up) | PWM3CR1[1] | 0x110 | RW-0 |
| TMR4IE | | PWM4CR1[1] | 0x116 | RW-0 |
| TMR5IE | | PWM5CR1[1] | 0x11C | RW-0 |
| TMR3IF | Timerx Interrupt flag 1 = Yes (latched) 0 = <u>No</u> | PWM3CR1[0] | 0x110 | RW-0 |
| TMR4IF | | PWM4CR1[0] | 0x116 | RW-0 |
| TMR5IF | | PWM5CR1[0] | 0x11C | RW-0 |

Table 7-3 Timerx (x = 3, 4, 5) Interrupt Enable and Status Bit

7.5.2 R/W operation of Timer3/4/5 register

TMRxH and TMRxL cannot be READ or WRITE simultaneously. It is recommended to set “TMRxON =0” first, then read/write TMRxL and TMRxH.

7.5.3 PWMx Mode

PWMx Mode — The duty cycle of the PWM3/4/5 are independent

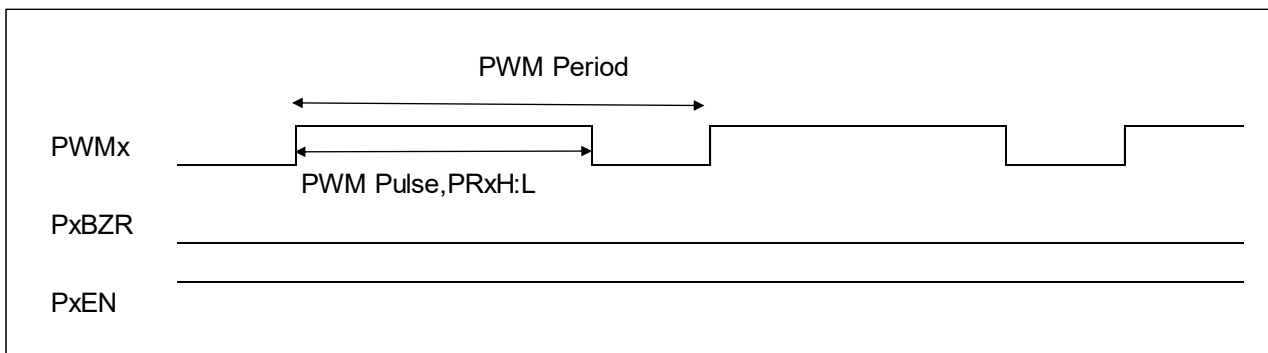


Figure 7-3 PWMx operating mode (Positive output)

PWMx period is specified by the PxPER, like [Equation 7-1](#). The PWM duty cycle is specified by PRxH:L, like [Equation 7-2](#) and [Equation 7-3](#).

Equation 7-1 $PWMx\ period = 2^N * T_{PCK} * (TMRxprescaler)$ (N is effective bit configured by PxPER)

Equation 7-2 $PWMx\ pulse = (PRx) * T_{PCK} * (TMRxprescaler)$

Equation 7-3 $PWMxduty\ cycle = (PRx) / 2^N;$ (N is effective bit configured by PxPER)

TIMERx have 8 perscale option, PxCK can be divided by 1, 2, 4, 8, 16, 32, 64, 128. Perscaler:

| PxCKSRC | Clock source and divider | PWMx / BUZZERx output |
|---------|--------------------------------------|---|
| 000 | 2x Instruction clock / (TxCKDIV + 1) | Normal |
| 001 | HIRC / (TxCKDIV + 1) | Normal |
| 010 | T0CKI / (TxCKDIV + 1) | Normal |
| 011 | T1CKI / (TxCKDIV + 1) | Normal |
| 100 | HIRC / (TxCKDIV + 1) | Low |
| 101 | HIRC / (TxCKDIV + 1) | High |
| 110 | HIRC / (TxCKDIV + 1) | PWMx modulates PxCK according to high pulse |
| 111 | HIRC / (TxCKDIV + 1) | PWMx modulates PxCK according to low pulse |

Table 7-4 PWM output mode

Note:

1. In PWMx mode, when TMRxH:L = 2^N (N is effective bit configured by PxPER), TMRxH:L automatically cleared;
2. PRxH and PRxL cannot be WRITE simultaneously. it immediately effects PWM duty cycle when writing to PRxH:L, it is recommended to write target value to PRx before TIMERx running.
3. ECCP priority is higher than PWM3/PWM4/PWM5, If it want to use both ECCP's PWM and PWM3/4/5, P1M<1:0> should be configured "00", that is single output mode (see [Section 10](#))

BUZZERx mode — PWMx output 50% duty cycle square wave, the period decided by PRxH:L like [Equation 7-4](#).

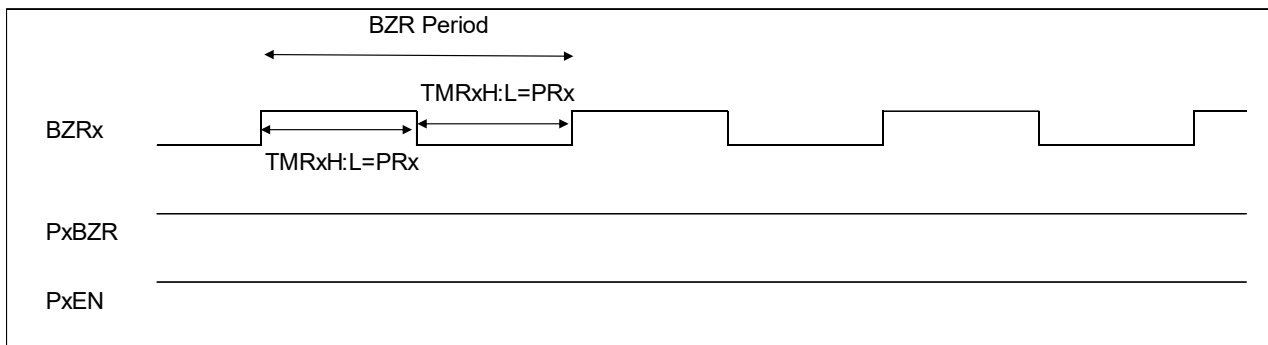


Figure 7-4 50% duty cycle of the BUZZER square wave

Equation 7-4 $BUZZERxperiod = 2 * PRx * T_{PxCK} * (TMRxprescaler)$

Note:

1. When operating BUZZER mode, TIMERx automatically operates in 12-bit mode, no matter what the value of PxPER. When TMRxH:L is equal to PRx, TMRxH:L is automatically cleared;
2. In BUZZER mode, if PRx=0x000, PWMx always outputs 0, TMRxIF will be set when 12-bit TIMERx overflows.

8. SLEEP (POWER-DOWN)

During SLEEP Instruction Clock is inactive and instructions execution is halted. Most modules are powered down to conserve power. As listed in [Table 8-1](#), FT61FC2x can selectively turn on individual modules in SLEEP so that functions, LVR, LVD, WDT, Timers, Comparator, PWM and ADC, can be maintained during SLEEP if desired without instruction interventions. Some modules can configure automatic power down upon SLEEP to save the need to turn them off by instructions.

| Module | Condition in SLEEP | |
|----------------------------|---|-------------------------|
| | RUN | RUN |
| Instruction Clock | (always power down) | Yes |
| LVR (Configure the LVREN) | Enabled or Instruction controlled (SLVREN=1) | Enabled except in SLEEP |
| LVD | LVDEN = 1 | No |
| WDT | WDTE or SWDTEN | No |
| TIMER0 | (always power down) | Yes |
| TIMER1 | TMR1ON = 1 & T1SYNC = 1 & TMR1CS = 1 & T1OSCEN = 1 | TMR1ON = 0 |
| TIMER2 | (always power down) | Yes |
| PWM3/4/5 | PxCKSRC = 010 / 011 & TMRxON = 1 | No |
| Enhanced ECCP | (follows TIMER2) | |
| HIRC / LIRC / EC / LP / XT | (follow peripherals that are using them) | |
| ADC | (Runs if ADON = 1 and the ADC clock source is running) | |
| Comparator | (CM ≠ 000 or 111, comparator maintain running) | |
| Voltage Regulator | (VREG_OE = 1, Voltage regulator maintain running) | |
| I/O | (maintain their states before SLEEP unless PWM SLEEP enabled) | |

Table 8-1 All except Instruction Clock can remain active in SLEEP if so desired

8.1 Entering into SLEEP

A SLEEP command puts the CPU to SLEEP.

1. If WDT is enabled, it will clear its Postscalar (if assigned) and counter, and start counting.
2. Time Out Flag (/TF) = 1
3. Power Down Flag (/PF) = 0
4. Clock sources
 - Instruction Clock shuts down automatically.
 - HIRC, LIRC, external oscillators (EC, LP, XT) are active if the Timer that uses them remains active. If a certain Timer auto-shutdown in SLEEP, its clock source will auto-shutdown too unless it is used by another Timer that remains active.
 - Instruction Clock will stop, and therefore output will not update anymore even if configured so.
5. I/O PORTS
 - PWM output continue if Timer3/4/5 is active in SLEEP. PWM auto-shutdown if Timer3/4/5 auto-shutdown.
 - For other digital outputs, they will maintain the state before SLEEP ((Tri-state, “0” or “1”)

- ADC is active if “ADON = 1” and the ADC clock source is active. It will auto-shutdown if its clock source auto-shutdown.

For more information about how peripherals work in SLEEP please refer to the corresponding chapters.

8.2 Waking-Up from SLEEP

There are 2 general principles to Wake-up from sleep:

- Time based, in which the CPU wakes up after a certain amount of time. LIRC is the clock choice for keeping time as it has lower power consumption than HIRC.
- Events based that triggers POR, System-Reset, Wake-up without Interrupt, and Interrupts, such as LVD, ADC, Interrupt-on-change, PC1-INT.

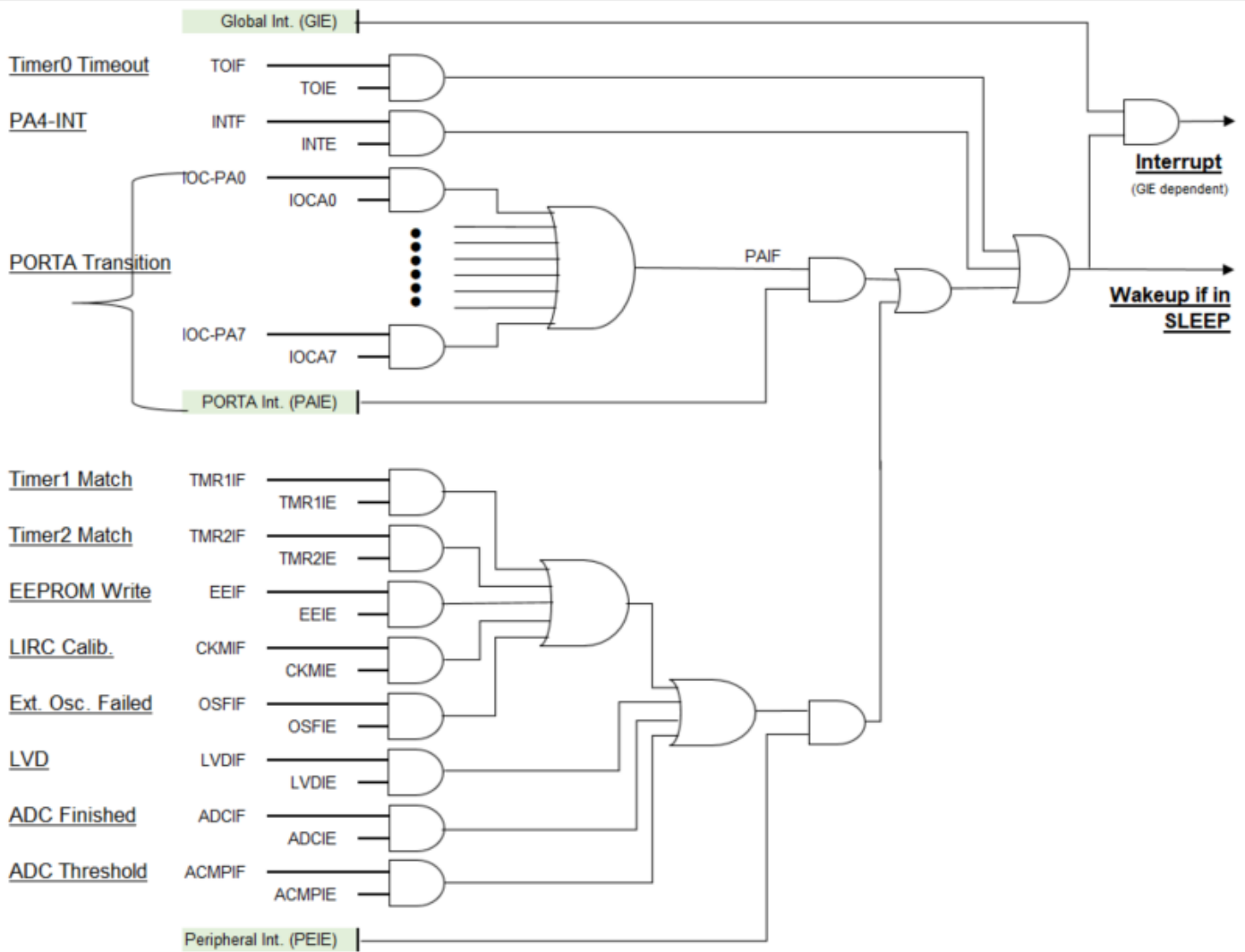
The situations Wake-up from sleep as follows:

1. Watchdog Timer Wake-up if enabled (see [Section 7.1](#) Watchdog Timer).
2. Full-Reset and System-Reset
 - POR Full-Reset (cannot be disabled)
 - External System-Reset by the /MCLR if enabled
 - LVR Reset if enabled
3. Enabled Interrupts (Disabling the “Global Interrupt Enable” will not stop Wake-up). Please see [Section 9](#) Interrupts.

Notes:

1. Waking up will also clear WDT.

9. INTERRUPTS



Note: Instruction Clock stops during sleep, only peripherals that do not select the Instruction Clock as the clock source can wake the device from sleep.

Figure 9-1 Interrupt Block Diagram

The CPU supports 15 sources of Interrupt in 2 groups:

- 1) Non-Peripherals (Timer0 and I/O)
 - Timer0 Overflows
 - PC1-INT (automatic rising or falling edge interrupt)
 - PORTA Interrupt-on-Change (software controlled)
- 2) Peripherals
 - Timer1 overflows
 - Timer2 matches PR2
 - DATA EEPROM Write Completion
 - LIRC and HIRC Cross Calibration Completion
 - Fail-Safe Clock Monitor

- Timer1 capture/compare
- ADC Conversion Completion
- Comparator1/comparator2 output changed
- Timer3/ Timer4/ Timer5 matches

WDT overflows, unlike other Timers, will not result in an Interrupt. For other interrupts besides external I/O interrupts please see the corresponding chapters.

In an Interrupt the PC jumps to and executes the “Interrupt Service Routine (ISR)”. There are multiple levels of Interrupt Disable/Enable.

- Each interrupt source has a local interrupt enable: T0IE, INTE, IOCAx, TMRxIE(x=1,2,3,4,5), EEIE, CKMEAIE, CxIE(x=1,2), OSFIE, ADIE, CCP1IE
- The 8 PAX Interrupt Inputs have a group PORT interrupt enable: PAIE (PORTA Interrupt Enable)
- The Peripheral interrupts has a master interrupt enable: PEIE (PERipheral Interrupt Enable).
- All controls above, if disabled, will not execute a Wake-Up from SLEEP.
- All interrupts are controlled by a global enable: GIE (Global Interrupt Enable). This enable differs from the others by allowing a Wake-Up from SLEEP even when disabled.
- Disabling the interrupts does not affect the setting of the interrupt flags.
- Timer0 and Timer2 interrupt can not wake up CPU from SLEEP.

The following sequences occur upon an Interrupt:

- Automatic set “GIE = 0”, disabling further interrupts.
- The return address is pushed onto the stack and the PC (program counter) is loaded with 0x0004.
- Jump to the “Interrupt Service Routine” 1 – 2 instruction cycles after the interrupt.
- “Return from Interrupt (RETI)” instruction exits ISR. Prior to RETI must clear the interrupt flag currently being processed.
- At the completion of the ISR, the PC returns to the address before the interrupt, which in SLEEP, is the address immediate after SLEEP.
- Automatic set GIE = 1 upon executing RETI, enabling future interrupts.

Note: Only the return PC is saved on the stack during an interrupt. Users desiring to have other registers (e.g., W and STATUS) saved must use instructions to write them into temporary registers explicitly. Use the last 16 bytes of SRAM for temporary storages as they are common to all banks and do not require bank swithing.

9.1 Summary of Interrupt Related Registers

| Name | Address | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Reset (RW) |
|---------|---------|----------------------------------|------------|-------------|-------|--------------|--------|--------|--------|------------|
| INTCON | 0x0B | GIE | PEIE | T0IE | INTE | PAIE | T0IF | INTF | PAIF | 0000 0000 |
| PIE1 | 0x8C | EEIE | CKMEAIE | - | C2IE | C1IE | OSFIE | TMR2IE | TMR1IE | 0000 0000 |
| PIR1 | 0x0C | EEIF | CKMEAIF | - | C2IF | C1IF | OSFIF | TMR2IF | TMR1IF | 0000 0000 |
| PIE2 | 0x8D | - | - | - | - | - | - | ADIE | CCP1IE | ---- --00 |
| PIR2 | 0x0D | - | - | - | - | - | - | ADIF | CCP1IF | ---- --00 |
| PWM3CR0 | 0x10F | P3INTS | P3PER[2:0] | | | P3CKSRC[2:0] | | | P3BZR | 0000 0000 |
| PWM3CR1 | 0x110 | P3EN | P3POL | TMR3PS[2:0] | | | TMR3ON | TMR3IE | TMR3IF | 0000 0000 |
| PWM4CR0 | 0x115 | P4INTS | P4PER[2:0] | | | P4CKSRC[2:0] | | | P4BZR | 0000 0000 |
| PWM4CR1 | 0x116 | P4EN | P4POL | TMR4PS[2:0] | | | TMR4ON | TMR4IE | TMR4IF | 0000 0000 |
| PWM5CR0 | 0x11B | P5INTS | P5PER[2:0] | | | P5CKSRC[2:0] | | | P5BZR | 0000 0000 |
| PWM5CR1 | 0x11C | P5EN | P5POL | TMR5PS[2:0] | | | TMR5ON | TMR5IE | TMR5IF | 0000 0000 |
| OPTION | 0x81 | /PAPU | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 |
| TRISA | 0x85 | PORTA direction select | | | | | | | | 1111 1111 |
| IOCA | 0x96 | Interrupt on PORTA Logic-Changes | | | | | | | | 0000 0000 |

Table 9-1 Interrupt Related Register Addresses and Default

| Name | Status | Register | Addr. | Reset |
|------|---|-----------|-----------------------|-------|
| GIE | Global Interrupt 1 = Enables (PEIE, local settings applies) 0 = <u>Global Disables</u> (Wake-Up not affected) | INTCON[7] | 0x0B 0x8B 0x10B | RW-0 |
| PEIE | Master Peripheral Interrupt 1 = Enables (local settings applies) 0 = <u>Disables</u> (no Wake-Up) | INTCON[6] | | RW-0 |
| T0IE | Timer0 Overflow Interrupt | INTCON[5] | | RW-0 |
| INTE | PC1-INT External Interrupt | INTCON[4] | | RW-0 |
| PAIE | PORTA Interrupt-on-Change | INTCON[3] | | RW-0 |
| T0IF | Timer0 Overflow Interrupt? | INTCON[2] | | RW-0 |
| INTF | PC1-INT External Interrupt? | INTCON[1] | | RW-0 |
| PAIF | PORTA Interrupt-on-Change? | INTCON[0] | | RW-0 |

Table 9-2 INTCON register

| Name | Status | Register | Addr. | Reset |
|---------|--------------------------------------|----------|-------|-------|
| EEIE | EE Write Completed Interrupt | PIE1[7] | 0x8C | RW-0 |
| CKMEAIE | LIRC Calibration Completed Interrupt | PIE1[6] | | RW-0 |
| C2IE | Comparator2 Interrupt | PIE1[4] | | RW-0 |
| C1IE | Comparator1 Interrupt | PIE1[3] | | RW-0 |
| OSFIE | External Oscillator Failed Interrupt | PIE1[2] | | RW-0 |
| TMR2IE | Timer2 matched PR2 Interrupt | PIE1[1] | | RW-0 |
| TMR1IE | Timer1 overflows interrupt | PIE1[0] | | RW-0 |
| ADIE | ADC Conversion Finished Interrupt | PIE2[1] | 0x8D | RW-0 |
| CCP1IE | CCP1 capture/matches interrupt | PIE2[0] | | RW-0 |

Table 9-3 PIE1 register

| Name | Status | Register | Addr. | Reset |
|---------|---------------------------------------|----------|-------|-------|
| EEIF | EEPROM Write operation completed? | PIR1[7] | 0x0C | RW-0 |
| CKMEAIF | LIRC Calibration completed? | PIR1[6] | | RW-0 |
| C2IF | Comparator2 interrupt? | PIR1[4] | | RW-0 |
| C1IF | Comparator1 interrupt? | PIR1[3] | | RW-0 |
| OSFIF | External Oscillator Failed interrupt? | PIR1[2] | | RW-0 |
| TMR2IF | Timer2 matching PR2 interrupt? | PIR1[1] | | RW-0 |
| TMR1IF | Timer1 overflows interrupt? | PIR1[0] | | RW-0 |
| ADIF | ADC Conversion Finished interrupt? | PIR2[1] | 0x0D | RW-0 |
| CCP1IF | CCP1 capture/matches interrupt? | PIR2[0] | | RW-0 |

Table 9-4 PIR1 register

| Name | Status | Register | Addr. | Reset |
|--------|-----------------------------|------------|-------|-------|
| P3INTS | Timer3 interrupt select bit | PWM3CR0[7] | 0x10F | RW-0 |
| P4INTS | Timer4 interrupt select bit | PWM4CR0[7] | 0x115 | RW-0 |
| P5INTS | Timer5 interrupt select bit | PWM5CR0[7] | 0x11B | RW-0 |
| TMR3IE | Timer3 interrupt enable bit | PWM3CR1[1] | 0x110 | RW-0 |
| TMR4IE | Timer4 interrupt enable bit | PWM4CR1[1] | 0x116 | RW-0 |
| TMR5IE | Timer5 interrupt enable bit | PWM5CR1[1] | 0x11C | RW-0 |
| TMR3IF | Timer3 interrupt flag | PWM3CR1[0] | 0x110 | RW-0 |
| TMR4IF | Timer4 interrupt flag | PWM4CR1[0] | 0x116 | RW-0 |
| TMR5IF | Timer5 interrupt flag | PWM5CR1[0] | 0x11C | RW-0 |

Table 9-1 Timer3/4/5 Interrupt register

| Name | Status | Register | Addr. | Reset |
|--------|--|------------|-------|-------------|
| /PAPU | <u>PORTA Pull-Up</u> 1 = <u>Global Disables</u> 0 = Enables WPUA settings | OPTION[7] | 0x81 | RW-1 |
| INTEDG | <u>PC1 Interrupt Edge</u> 1 = <u>Rising</u> 0 = <u>Falling</u> | OPTION[6] | | RW-1 |
| TRISA | <u>PORTA I/O Digital Output (Direction)</u> 1 = <u>Input (Disables Digital Output)</u> 0 = Disables Pull-Up/Down | TRISA[7:0] | 0x85 | RW-11111111 |
| IOCA | <u>PORTA Interrupt-on-Change</u> 1 = Enables 0 = <u>Disables</u> | IOCA[7:0] | 0x96 | RW-00000000 |

Table 9-2 OPTION, TRISA and IOCA registers

9.2 PC1-INT and PORTA Interrupt-on-Change

| Name | PC1-INT | PORTA Logic-Changes |
|----------------------|--|--|
| Channel(s) | PC1 only | PA0 – PA7 (up to 8 channels) |
| I/O Setup | TRISC[1] = 1; ANSEL[4] = 0; CMCON0[2:0] = 111 | TRISA[x] = 1; ANSEL[x] = 0; CMCON0[2:0] = 111 |
| Other settings | INTEDG, INTE, GIE, INTF | IOCA, PAIE, GIE, PAIF |
| Trigger | either Rising or Falling, not both | 0 → 1 or 1 → 0 |
| Software Monitoring? | No | Required |

Table 9-3 Differences between PC1-INT and PORTA Interrupt-on-Change

PC1-INT and PORTA Interrupt-on-Change are the external I/O interrupts. PC1 can be as both. PC1-INT will run unsupervised in the background once setup properly. PORTA Interrupt-on-Change will need continuous software monitoring. For PORTA Interrupt-on-Change:

1. Latches Input Register into an Interrupt-On-Change latch (READ PORTA).
2. When input logic level changes, the difference in Input Register and latched data will set PAIF.
3. Latching Input Register will update compare reference, and if done immediately after PAIF is set have the effect of removing the Interrupt-On-Change trigger condition. PAIF can be instruction cleared when the Interrupt-On-Change condition is no longer valid.

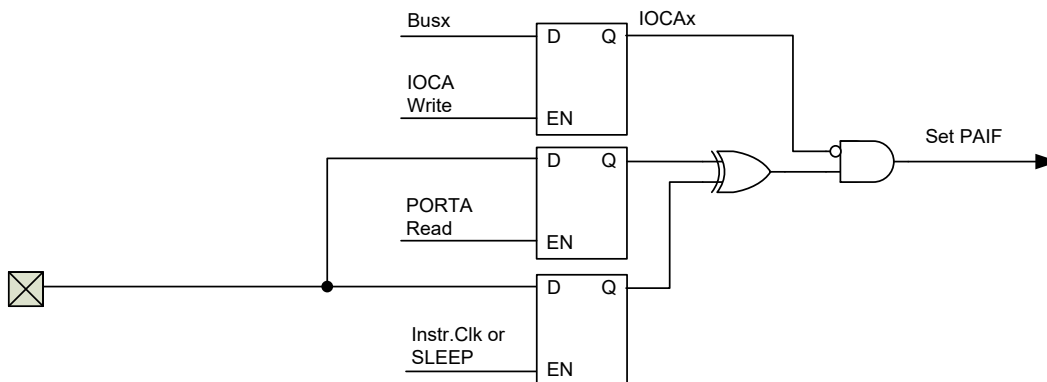


Figure 9-2 PORTA Transition interrupts

10. Enhanced Capture /Compare/PWM Module

The Enhanced Capture/Compare/PWM module is a peripheral which allows the user to time and control different events.

- Capture mode: In Capture mode, the peripheral allows the timing of the duration of an event
- Compare mode: The Compare mode allows the user to trigger an external event when a predetermined amount of time has expired.
- PWM mode (Enhanced): Single Output, Half-bridge, Full-bridge (Forward/Reverse mode).

| ECCP | Timer |
|----------------|---|
| Capture | Timer1 (must operating in timer mode or synchronous counter mode) |
| Compare | Timer1 (must operating in timer mode or synchronous counter mode) |
| PWM (Enhanced) | Timer2 |

Table 10-1 Timer source of different ECCP modes

10.1 Summary of ECCP Related Registers

| Name | Addr. | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Reset | |
|---------|-------|--|-------------|-------------|-------|------------|--------|-------------|-----------|-----------|-----------|
| T1CON | 0x10 | T1GINV | TMR1GE | T1CKPS[1:0] | | T1OSCEN | T1SYNC | TMR1CS | TMR1ON | 0000 0000 | |
| T2CON | 0x12 | - | TOUTPS[3:0] | | | | TMR2ON | T2CKPS[1:0] | | -000 0000 | |
| TMR1L | 0x0E | Least Significant Byte of the 16-bit TIMER1 Register | | | | | | | | xxxx xxxx | |
| TMR1H | 0x0F | Most Significant Byte of the 16-bit TIMER1 Register | | | | | | | | xxxx xxxx | |
| TMR2 | 0x11 | Timer 2 count result register | | | | | | | | xxxx xxxx | |
| PR2 | 0x92 | PR2 period register | | | | | | | | 1111 1111 | |
| CCPR1L | 0x13 | Least Significant Byte of the ECCP1 register | | | | | | | | xxxx xxxx | |
| CCPR1H | 0x14 | Most Significant Byte of the ECCP1 Register | | | | | | | | xxxx xxxx | |
| CCP1CON | 0x15 | P1M[1:0] | | DC1B[1:0] | | CCP1M[3:0] | | | 0000 0000 | | |
| PWM1CON | 0x16 | PRSEN | PDC[6:0] | | | | | | | | 0000 0000 |
| ECCPAS | 0x17 | ECCPASE | ECCPAS[2:0] | | | PSSAC[1:0] | | PSSBD[1:0] | | 0000 0000 | |
| PWM1AUX | 0x90 | AUX1EN | P1OS | P1FOE | P1EOE | P1DOE | P1COE | P1BOE | P1AOE | 0000 0000 | |

Table 10-2 ECCP Related Register Addresses and Default

| Name | Status | | Register | Addr | Reset |
|--------|--|------------------------------------|--|--------------|--------------|
| TMR1L | Least Significant Byte of the 16-bit TIMER1 Register | | TMR1L[7:0] | 0x0E | RW-0000 0000 |
| TMR1H | Most Significant Byte of the 16-bit TIMER1 Register | | TMR1H[7:0] | 0x0F | RW-0000 0000 |
| CCPR1L | Least Significant Byte of the ECCP1 register | | CCPR1L[7:0] | 0x13 | RW-xxxx xxxx |
| CCPR1H | Most Significant Byte of the ECCP1 Register | | CCPR1H[7:0] | 0x14 | RW-xxxx xxxx |
| CCP1M | <u>ECCP Mode Select bits</u> | | | CCP1CON[3:0] | RW-0000 |
| | Value | Mode | Description | | |
| | 0000 | Off | Resets ECCP module | | |
| | 0001/0011 | Unused | (Unused) | | |
| | 0100 | Capture mode (Caputer pin CCP1) | every falling edge | | |
| | 0101 | | every rising edge | | |
| | 0110 | | every 4th rising edge | | |
| | 0111 | | every 16th rising edge | | |
| | 0010 | Compare mode (Matches) | CCP1 toggle output on match | | |
| | 1000 | | CCP1 output high | | |
| | 1001 | | CCP1 output low | | |
| | 1010 | | CCP1 pin is unaffected | | |
| | 1011 | | trigger special event (CCP1 pin is unaffected) | | |
| | 1100 | PWM mode | P1A, P1C active-high; P1B, P1D active-high | | |
| | 1101 | | P1A, P1C active-high; P1B, P1D active-low | | |
| 1110 | P1A, P1C active-low; P1B, P1D active-high | | | | |
| 1111 | P1A, P1C active-low; P1B, P1D active-low | | | | |

Table 10-3 ECCP Capture/Compare/PWM mode register

| Name | Status | | Register | Addr | Reset | |
|--|--|----------------------------|--------------|------|-----------------|---|
| TMR2 | Timer 2 count result register | | TMR2[7:0] | 0x11 | RW-0000 0000 | |
| PR2 | PR2 period register | | PR2[7:0] | 0x92 | RW-1111 1111 | |
| DC1B | PWM Duty Cycle Least Significant bits (CCP1M = 11xx) | | CCP1CON[5:4] | 0x15 | RW-00 | |
| CCPR1L | Most Significant Byte of the PWM Duty Cycle | | CCPR1L[7:0] | 0x13 | RW-xxxx xxxx | |
| CCPR1H | Most Significant Byte of the PWM Duty Cycle Latch | | CCPR1H[7:0] | 0x14 | RO-xxxx xxxx | |
| P1M | <u>PWM Output Configuration bits (CCP1M = 11xx)</u> | | CCP1CON[7:6] | 0x15 | RW-00 | |
| | 00 | Single output | | | | P1A modulated; P1B, P1C, P1D assigned as port pins |
| | 01 | Full-bridge output forward | | | | P1D modulated; P1A active; P1B, P1C inactive |
| | 10 | Half-bridge output | | | | P1A, P1B modulated with dead-band control; P1C, P1D assigned as port pins |
| | 11 | Full-bridge output reverse | | | | P1B modulated; P1C active; P1A, P1D inactive |
| Note: CCP1M ≠ 11xx, P1A assigned as Capture/Compare input; P1B, P1C, P1D assigned as GPIO; | | | | | | |
| PRSEN | <u>PWM Restart enable bit</u> 1 = Enables (Upon auto-shutdown, ECCPASE clears automatically) 0 = Disables (Upon auto-shutdown, ECCPASE cleared by software) | | PWM1CON[7] | 0x16 | RW-0 | |
| PDC | <u>PWM Deadband Delay (Half-Bridge Mode)</u> Deadband = PDC[6:0] x Instruction clock | | PWM1CON[6:0] | | RW-000 0000 | |
| ECCPASE | <u>PWM Auto-Shutdown Event Status bit</u> 1 = A shutdown event has occurred; ECCP outputs are in shutdown state 0 = ECCP outputs are operating | | ECCPAS[7] | 0x17 | RW-0 | |
| ECCPAS | <u>ECCP Auto-shutdown Source Select bits</u> 000 = Auto-Shutdown is disabled 001 = Comparator 1 output high (C1OUT) 010 = Comparator 2 output high (C2OUT) 011 = Either Comparator 1 or 2 output high 100 = VIL on INT pin 101 = VIL on INT pin or Comparator 1 output high 110 = VIL on INT pin or Comparator 2 output high 111 = VIL on INT pin or Comparator 1 or 2 output high | | ECCPAS[6:4] | | RW-000 | |
| PSSAC | <u>Pins P1B and P1D Shutdown State Control bits</u> 00 = Drive pins P1A and P1C to '0' 01 = Drive pins P1B and P1D to '1' 1x = Tri-state | | ECCPAS[3:2] | | RW-00 | |

| Name | Status | Register | Addr | Reset |
|--------|--|-------------|------|-------|
| PSSBD | <u>Pins P1B and P1D Shutdown State Control bits</u> 00 = Drive pins P1B and P1D to '0' 01 = Drive pins P1B and P1D to '1' 1x = Tri-state | ECCPAS[1:0] | | RW-00 |
| AUX1EN | <u>PWM1 auxiliary function enable bit (Half-Bridge mode)</u> 1 = Enables 0 = <u>Disables</u> | PWM1AUX[7] | 0x90 | RW-0 |
| P1OS | <u>PWM One-pulse output (AUX1EN=1)</u> 1 = Enables (Automatically stopped after PWM output one-pulse, P1x as GPIO) 0 = <u>Disables</u> (PWM continuous output) | PWM1AUX[6] | | RW-0 |
| P1FOE | P1F output | PWM1AUX[5] | | RW-0 |
| P1EOE | P1E output | PWM1AUX[4] | | RW-0 |
| P1DOE | P1D output | PWM1AUX[3] | | RW-0 |
| P1COE | P1C output | PWM1AUX[2] | | RW-0 |
| P1BOE | P1B output | PWM1AUX[1] | | RW-0 |
| P1AOE | P1A output | PWM1AUX[0] | | RW-0 |

Table 10-4 Instruction Level PWM(Enhanced) Related Control Registers

| Name | Status | Register | Addr. | Reset |
|--------|--|-----------|-----------------------|-------|
| GIE | <u>Global Interrupt</u> 1 = Enables (PEIE, TMR1IE applies) 0 = <u>Global Disables</u> (Wake-Up not affected) | INTCON[7] | 0x0B 0x8B 0x10B | RW-0 |
| PEIE | <u>Master Peripheral Interrupt</u> 1 = Enables (CCP1IE applies) 0 = <u>Disables</u> (no Wake-Up) | INTCON[6] | | RW-0 |
| CCP1IE | <u>CCP1 Capture/Matches Interrupt control</u> 1 = Enables 0 = <u>Disables</u> (no Wake-Up) | PIE2[0] | 0x8D | RW-0 |
| CCP1IF | <u>CCP1 Capture/Matches Interrupt?</u> 1 = Yes (latched) 0 = <u>No</u> | PIR2[0] | 0x0D | RW-0 |

Table 10-5 ECCP Interrupt Enable and Status Bits

¹ P1OS = 1, this bit will be cleared automatically in the next PWM period;

10.2 Capture Mode

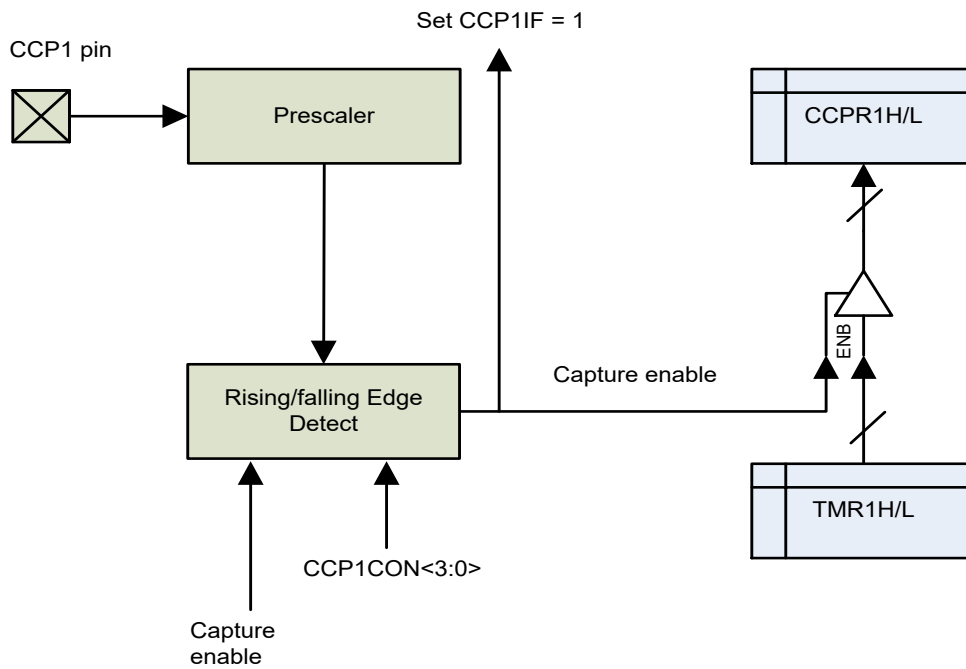


Figure 10-1 Capture mode block diagram

In Capture mode, CCPR1H:CCPR1L captures the 16-bit value of the TMR1 register when an event occurs on pin CCP1. An event is defined as one of the following and is configured by the CCP1M<3:0> bits of the CCP1CON register:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

When a capture is made, the Interrupt Request Flag bit CCP1IF of the PIR1 register is set. The interrupt flag must be cleared in software. Depends on the enable controls (GIE, PEIE and CCPIE) it may result in an AWAKE from SLEEP and/or Interrupt.

Note:

1. In Capture mode, the CCP1 pin should be configured as an input, If the CCP1 pin is configured as an output, a write to the PORTC[5] can cause a capture condition;
2. If another capture occurs before the value in the CCPR1H, CCPR1L register pair is read, the old captured value is overwritten by the new captured value;
3. When the Capture mode is changed, a false capture interrupt may be generated. The user should set CCP1M=0000 to turn off ECCP module to avoid false interrupts. Turn off ECCP module, any Reset or switching to other mode will clear the capture prescaler.

10.3 Compare Mode

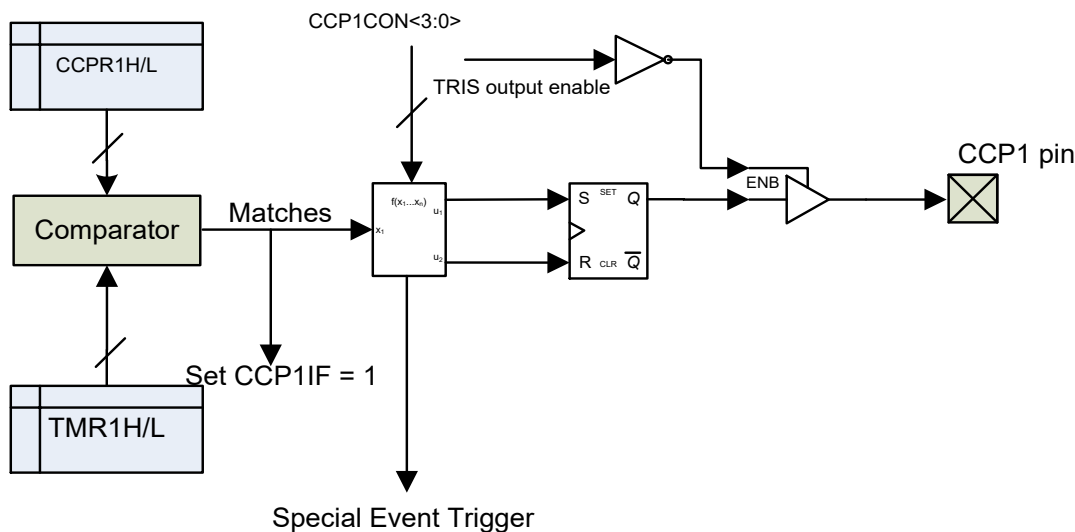


Figure 10-2 Compare mode block diagram

In Compare mode, the 16-bit CCPR1 register value is constantly compared against the TMR1 register pair value. When a match occurs, the CCP module may (see “CCP1M”):

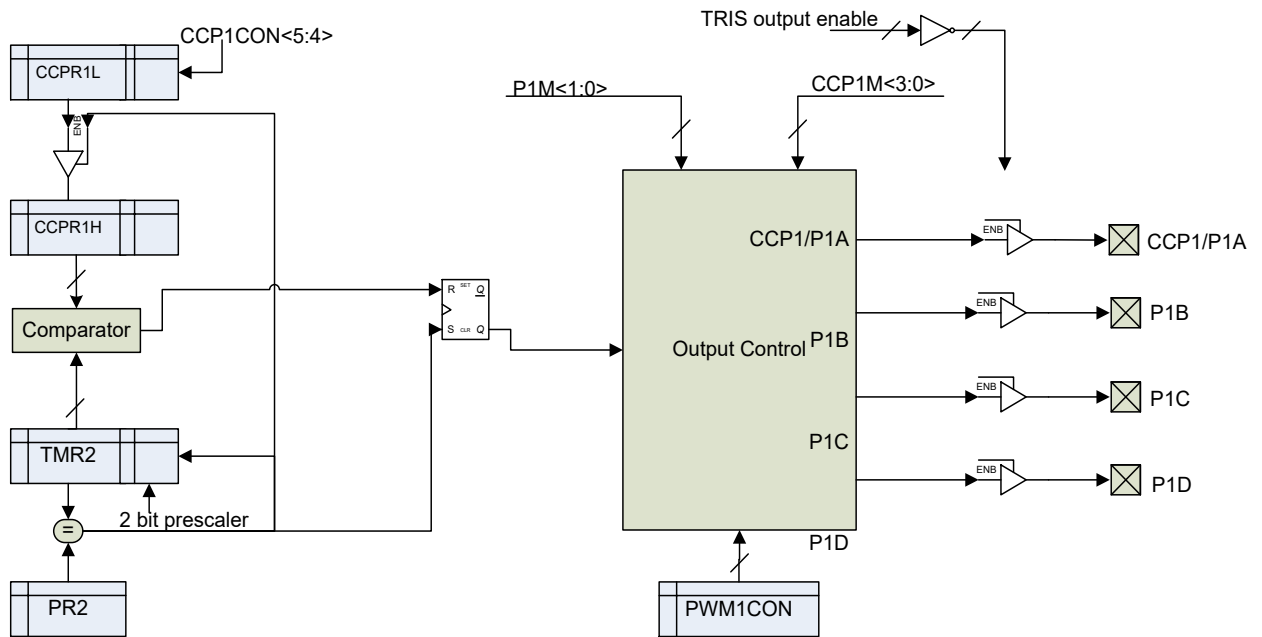
- Toggle the CCP1 output
- Set the CCP1 output
- Clear the CCP1 output
- CCP1 pin is unaffected
- Generate a Special Event Trigger (CCP1 pin is unaffected)
 - TMR1H:TMR1L cleared (TMR1IF will not be set “1”)
 - Starts an ADC conversion if ADC is enabled

An Interrupt flag (CCP1IF) is set. Depends on the enable controls (CCP1IE, GIE and PEIE) it may result in an AWAKE from SLEEP and/or Interrupt.

Note:

1. The user must configure the CCP1 pin(PC5) as an output in compare mode;
2. The TMR1H, TMR1L register pair is not reset until the next rising edge of the Timer1 clock. This allows the CCPR1H, CCPR1L register pair to effectively provide a 16-bit programmable period register for Timer1;
3. If TMR1H:TMR1L write operation and ECCP special event trigger simultaneous occur, the write operation has the higher priority .

10.4 PWM Enhanced Mode



Note: The 8-bit timer TMR2 register is concatenated with 2 bits of the prescaler, to create the 10-bit time base.

Figure 10-3 Enhanced PWM block diagram

Enhanced PWM features:

- Single PWM: P1A
- Half-Bridge PWM:
 - Deadband control with complementary output: P1A, P1B
 - Auxiliary function (3 pairs of deadband control with complementary output, one-pulse PWM output): P1A, P1B, P1C, P1D, P1E, P1F
- Full-Bridge PWM (Forward, Reverse): P1A, P1B, P1C, P1D
- 10-bit resolution ratio
- PWM output polarity selectable
- Auto-Shutdown mode, Auto-Restart Mode

Timer2 will be disabled in SLEEP mode and will retain the value before entering SLEEP.

Note:

1. Timer2 can be used for enhanced PWM mode or LIRC measurement, but not both.

10.4.1 Period

The PWM period is specified by the PR2 register of Timer2. The PWM period can be calculated using the Equation of [Equation 10-1](#):

$$\text{Equation 10-1} \quad \text{PWM Period} = (PR2+1) * 4 * T_{T2CK} * (\text{TMR2 prescaler value}) \quad (T2CK \text{ is Timer2 clock})$$

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

1. TMR2 is cleared (0x00);
2. The PWM duty cycle is latched from CCPR1L into CCPR1H;
3. PWM channel P1A~P1D is set or cleared depended on its polarity.

10.4.2 Duty Cycle

The PWM duty cycle is specified by (CCPR1L, DC1B), CCPR1L is the 8 MSbs, DC1B is the 2 LSbs. CCPR1L and DC1B can be written to at any time because the Double buffered designed

The PWM pulse width and duty cycle are calculated by:

Equation 10-2 $Pulse\ Width = (CCPR1L:DC1B) * T_{T2CK} * (TMR2\ prescaler\ value)$

Equation 10-3 $Duty\ Cycle\ ratio = (CCPR1L:DC1B) \div (4 * (PR2 + 1))$

10.4.3 PWM Output

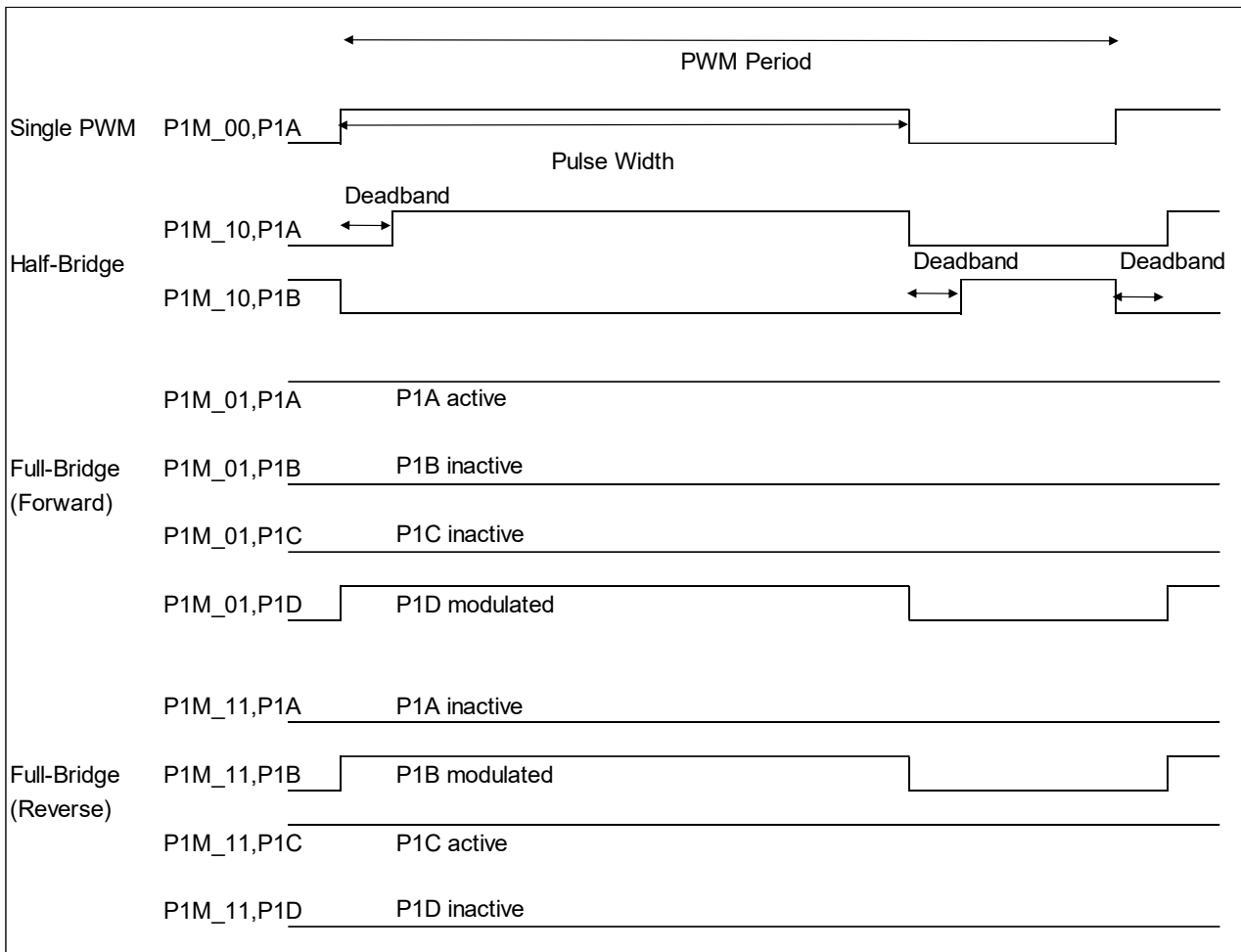


Figure 10-4 Example PWM Output relationships (P1A~P1D active high)

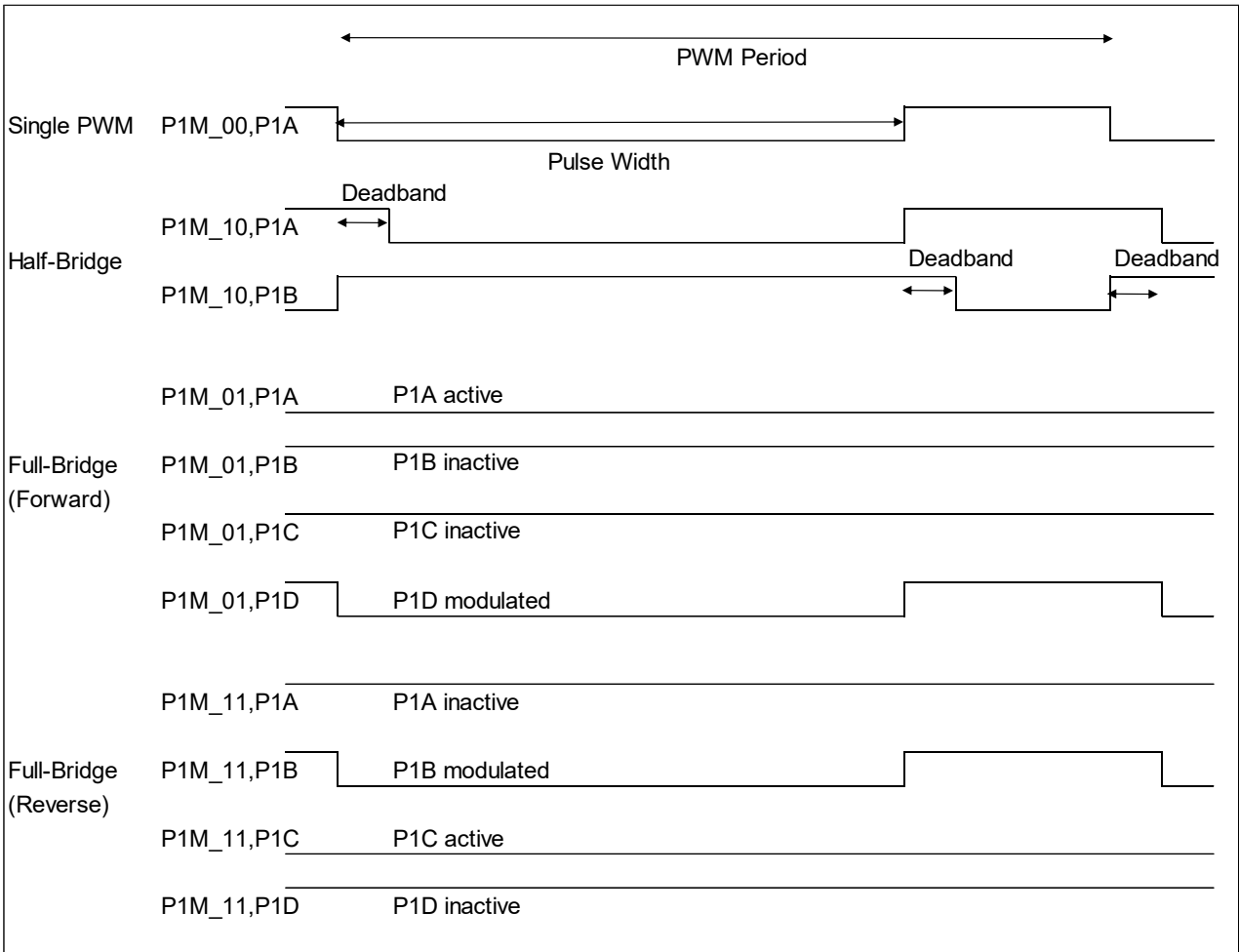


Figure 10-5 Example PWM Output relationships (P1A~P1D active low)

Single PWM — 1 PWM channel P1A;

Half-Bridge PWM — The 2 independent Deadband control with complementary PWM channels P1A and P1B. In Half-Bridge mode, the programmable dead-band delay can be used to prevent shoot-through current in half-bridge power devices (see “PDC”). Full-Bridge can be driven by add 4* NMOS or 2*PMOS and 2*NMOS. See [Figure 10-6](#), [Figure 10-7](#) and [Figure 10-8](#)

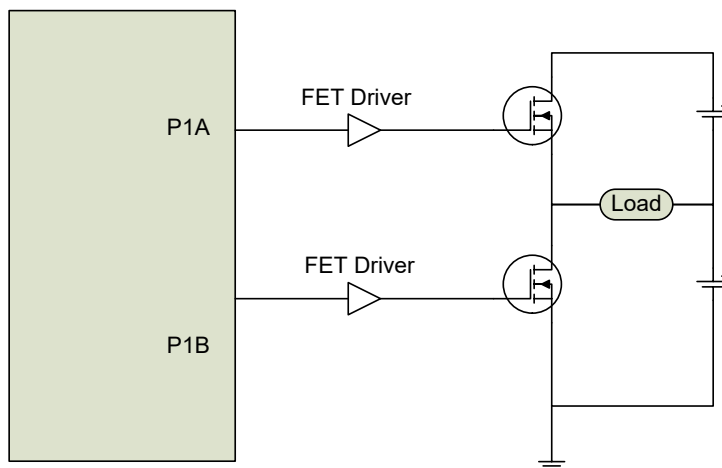


Figure 10-6 Standard Half-Bridge Circuit (Push-Pull, P1A~P1B active high)

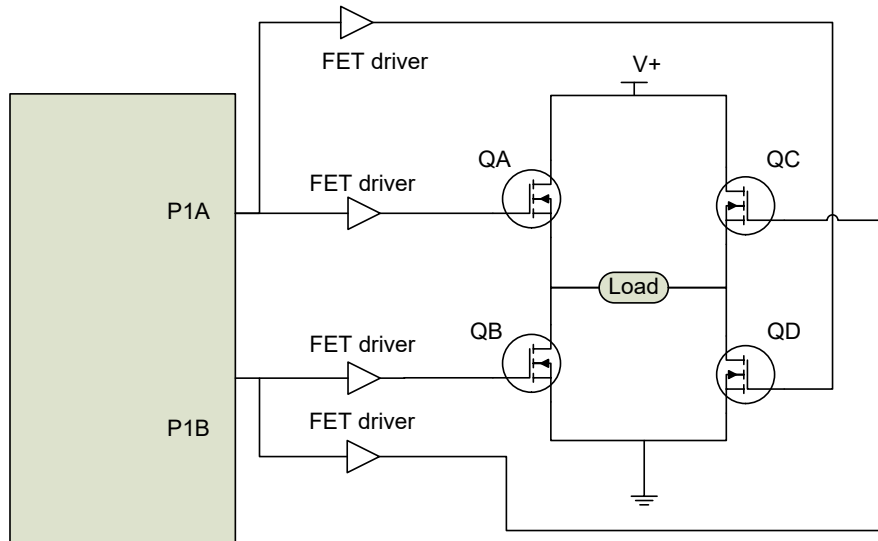


Figure 10-7 Half-Bridge Output Driving a Full-Bridge Circuit (4NMOS, P1A~P1B active high)

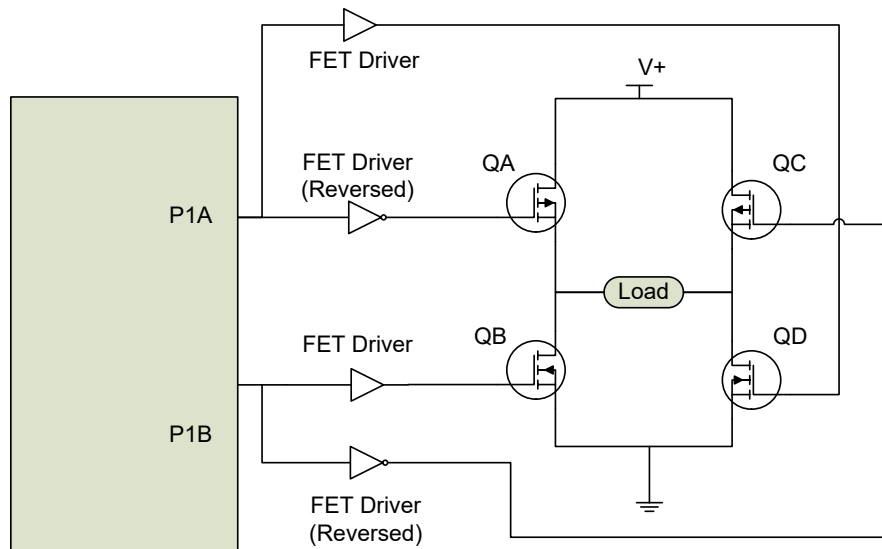


Figure 10-8 Half-Bridge Output Driving a Full-Bridge Circuit (2PMOS+2NMOS, P1A~P1B active high)

Full-Bridge PWM (Forward, Reversed) — 4 PWM channel P1A, P1B, P1C, P1D. See [Figure 10-9](#).

In the Full-Bridge mode, the P1M register allows users to control the forward/reverse direction. When the application firmware changes this direction control bit, the module will change to the new direction on the next PWM cycle. The modulated P1B and P1D signals are inactive at this time. The length of this time is $4 \cdot T_{T2CK}$, Circuit example see [Figure 10-10](#). Output wave see [Figure 10-11](#)

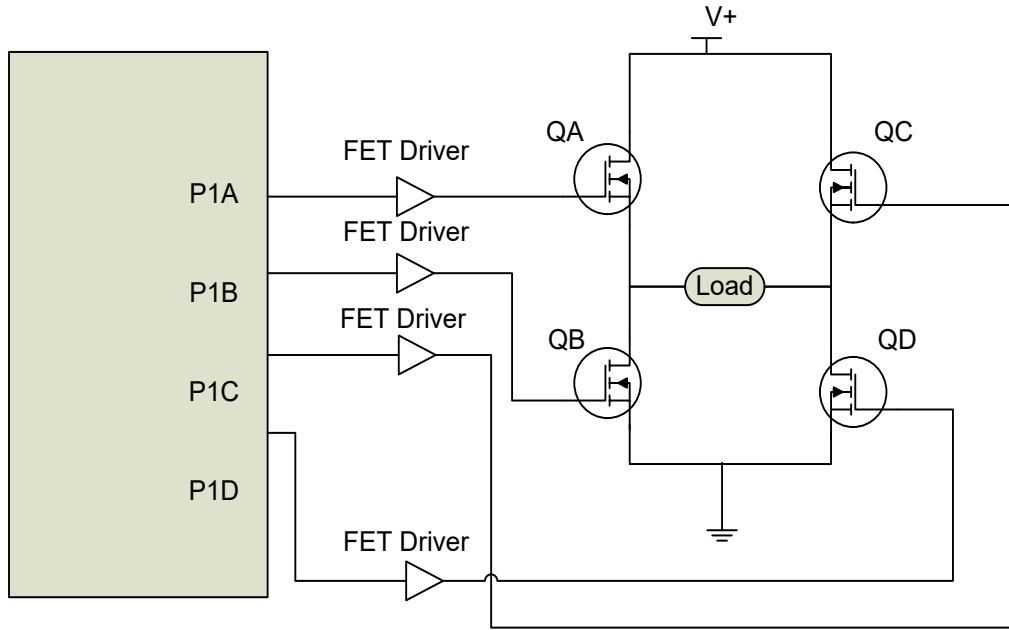


Figure 10-9 Example of Full-Bridge Application (4NMOS, P1A~P1D active high)

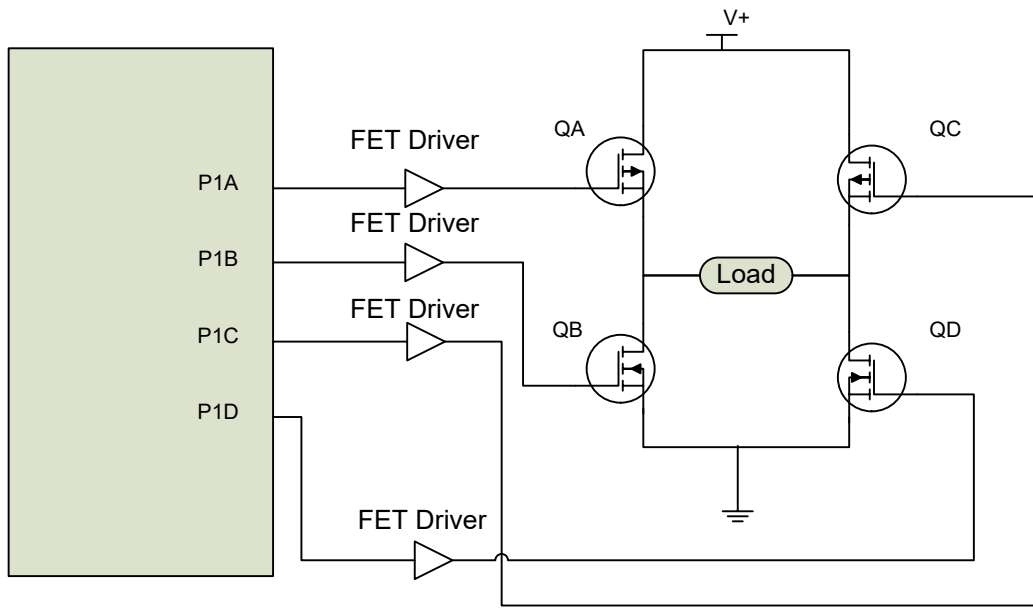


Figure 10-10 Example of Full-Bridge Application (2 PMOS+2NMOS, P1A and P1C active low, P1B and P1D active high)

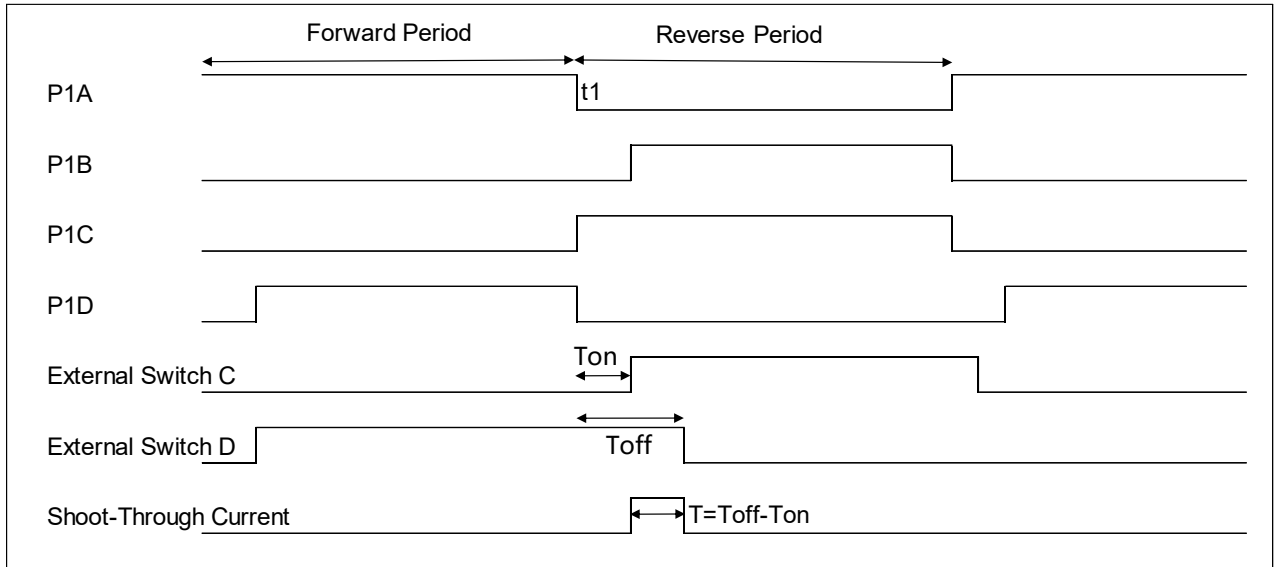


Figure 10-11 Full-Bridge PWM Output (P1A and P1C active low,P1B and P1D active high)

The Full-Bridge mode does not provide dead-band delay. As one output is modulated at a time, dead-band delay is generally not required. There is a situation where dead-band delay is required. This situation occurs when both of the following conditions are true:

1. The direction of the PWM output changes when the duty cycle of the output is at or near 100%.
2. The turn off time of the power switch, including the power device and driver circuit, is greater than the turn on time.

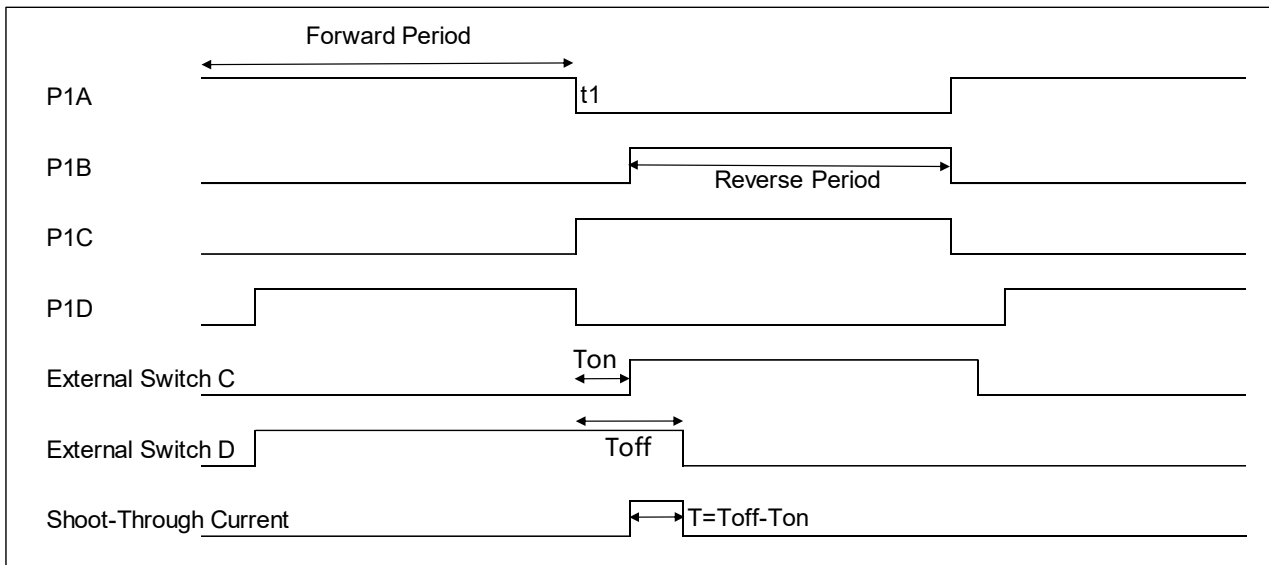


Figure 10-12 Example of PWM direction change at near 100% duty cycle (P1A~P1D active high)

Figure 10-12 shows an example of the PWM direction changing from forward to reverse, at a near 100% duty cycle. In this example, at time t_1 , the output P1A and P1D become inactive, while output P1C becomes active. Since the turn off time(T_{off}) of the power devices is longer than the turn on time(T_{on}), a shoot-through current will flow through power devices QC and QD (see **Figure 10-9**) for the duration of " T ($T_{off}-T_{on}$)". The same phenomenon will occur to power devices QA and QB for PWM direction change from reverse to forward.

If changing PWM direction at high duty cycle is required for an application, two possible solutions for eliminating the shoot-through current are:

1. Reduce PWM duty cycle for one PWM period before changing directions.
2. Use switch drivers that can drive the switches off faster than they can drive them on.

10.4.4 PWM Auto-Shutdown and Auto-Restart

Enhanced PWM support Auto-Shutdown and Auto-Restart(See"PRSEN").

The PWM mode supports an Auto-Shutdown mode that will disable the PWM outputs when an external shutdown event occurs. ECCP Auto-shutdown Source (See "ECCPAS[2:0]"):

- Comparator 1 output high (C1OUT)
- Comparator 2 output high (C2OUT)
- Either Comparator 1 or 2 output high
- VIL on INT pin
- VIL on INT pin or Comparator 1 output high
- VIL on INT pin or Comparator 2 output high
- VIL on INT pin or Comparator 1 or 2 output high

When a shutdown event occurs, two things happen:

1. The ECCPASE bit is set to '1'. The ECCPASE will remain set until cleared in firmware or an auto-restart occurs
2. Each PWM output pin pair may be placed into one of three states: (See "PSSAC", "PSSBD"):
 - Drive logic '1'
 - Drive logic '0'
 - Tri-state (high-impedance)

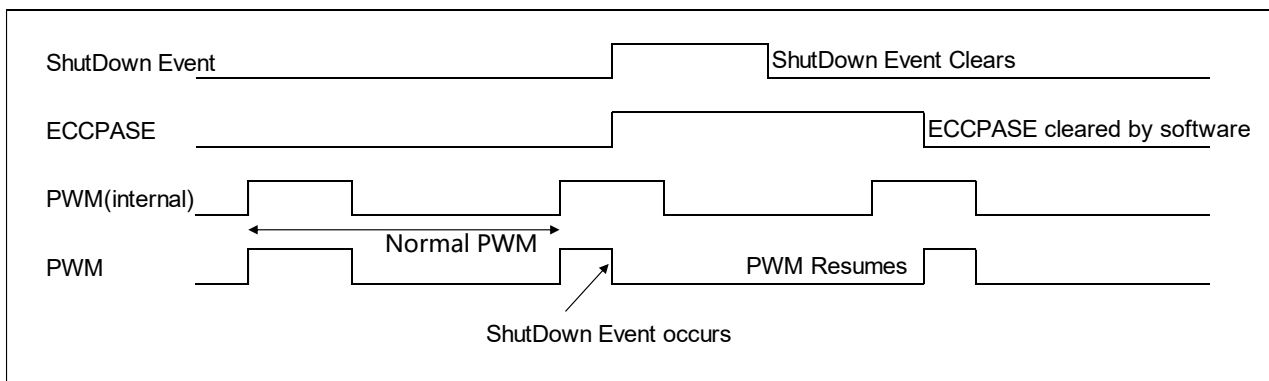


Figure 10-13 PWM Auto-Shutdown, not Auto-Restart

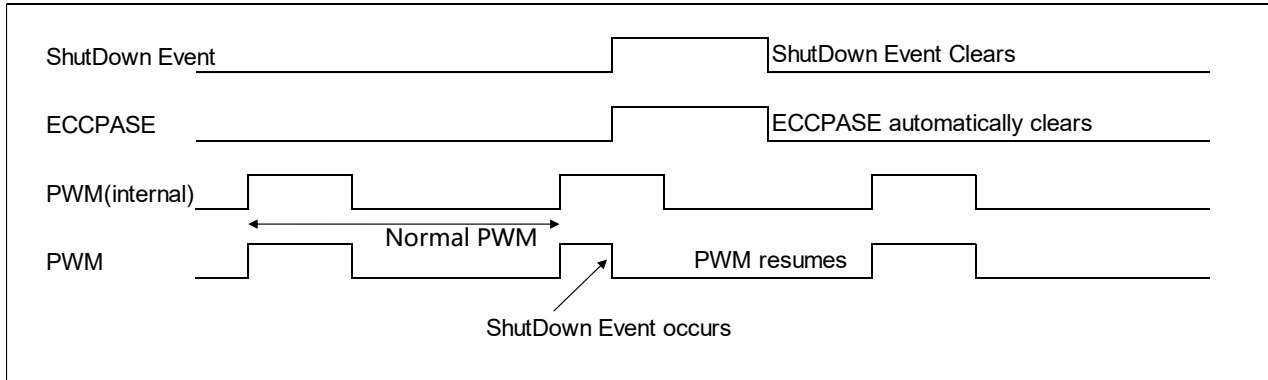


Figure 10-14 PWM Auto-Shutdown, Auto-Restart

Note:

1. The auto-shutdown condition is a level-based signal, not an edge-based signal. As long as the level is present, the auto-shutdown will persist;
2. When the auto-shutdown condition is effective, PWM stop output but Timer2 keep running, PWM resume immediately when auto-shutdown condition removed
3. The ECCPASE bit will remain set and can not be cleared by software as long as the auto-shutdown condition is active.
4. Once the auto-shutdown condition has been removed:
 - If Auto-Restart is enabled (PRSEN=1), ECCPASE cleared by hardware, PWM output auto-restart.
 - If Auto-Restart is disabled (PRSEN=0), ECCPASE must be cleared by software to restart PWM output.
5. Shutdown state is indicated by ECCPASE bit of ECCPAS register. If ECCPASE = 0, PWM outputs are operating, if ECCPASE = 1, PWM output shutdown.

10.4.5 PWM Auxiliary Function

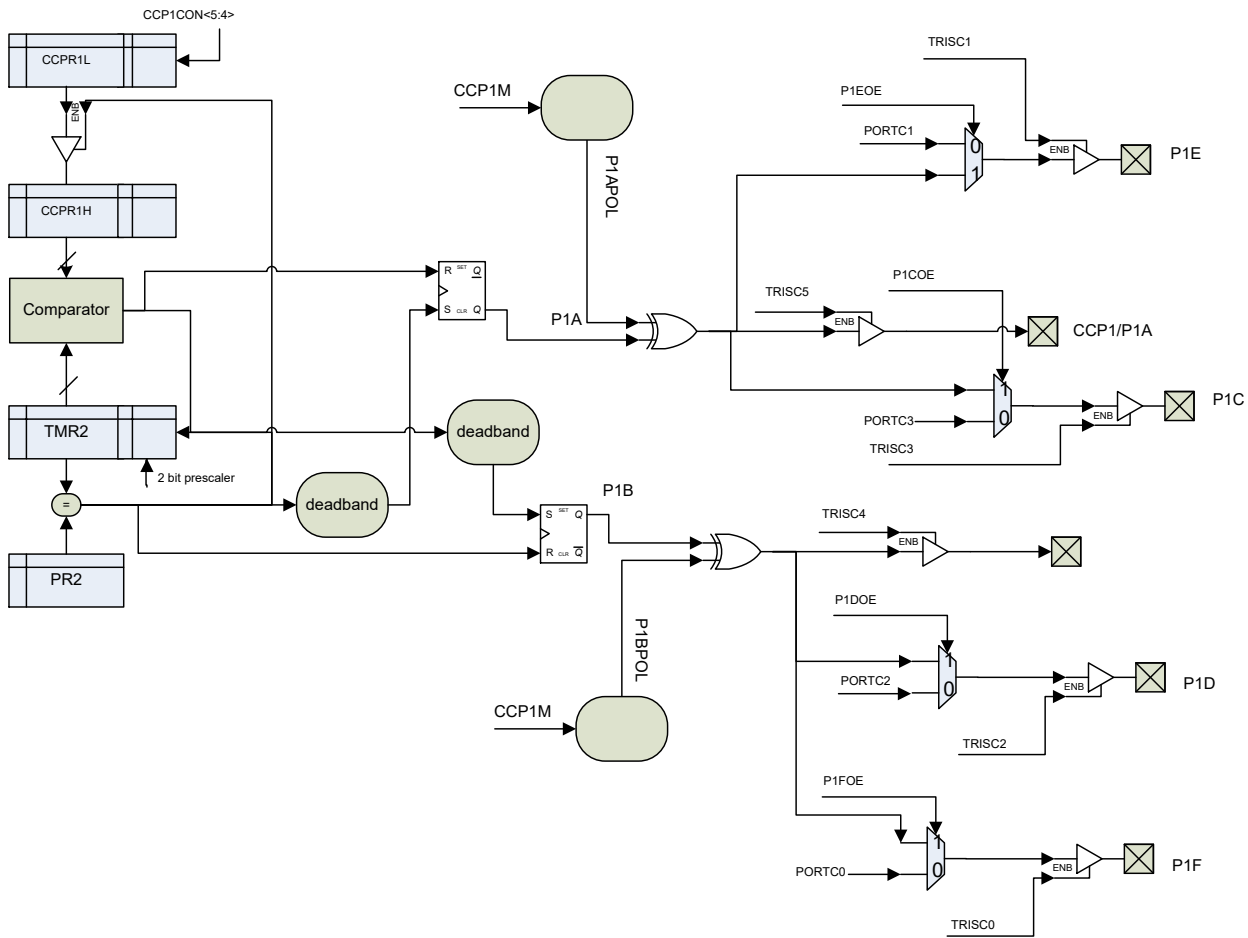


Figure 10-15 PWM auxiliary output block diagram

Loding the PWM1AUX register with the appropriate values, enhanced PWM which operating in half-bridge mode can do:

- Up to 3 pairs of 6 PWM signals complementary output with deadband control at the same time (P1xOE=1): P1A, P1B, P1C, P1D, P1E, P1F;
- One-pulse mode (P1OS=1, P1xOE=1): Automatically shuts down PWM output and clear P1xOE bit after output one PWM signal,;
- Configurable output polarity (See “CCP1M”).

Note:

1. P1A and P1B are first pair of complmentary half-bridge PWM output with deadband control, the other 2 pairs P1C and P1D, P1E and P1F have the same wave with the first pair, see [Figure 10-16](#);
2. It should be noted that that in this mode, P1xOE will be cleared when PWM output one pluse, PWM counter will keep counting, if software set P1xOE (x can be A~F) again, then pin P1x(x can be A~F) will output a PWM waveform in the next PWM cycle, see [Figure 10-17](#).

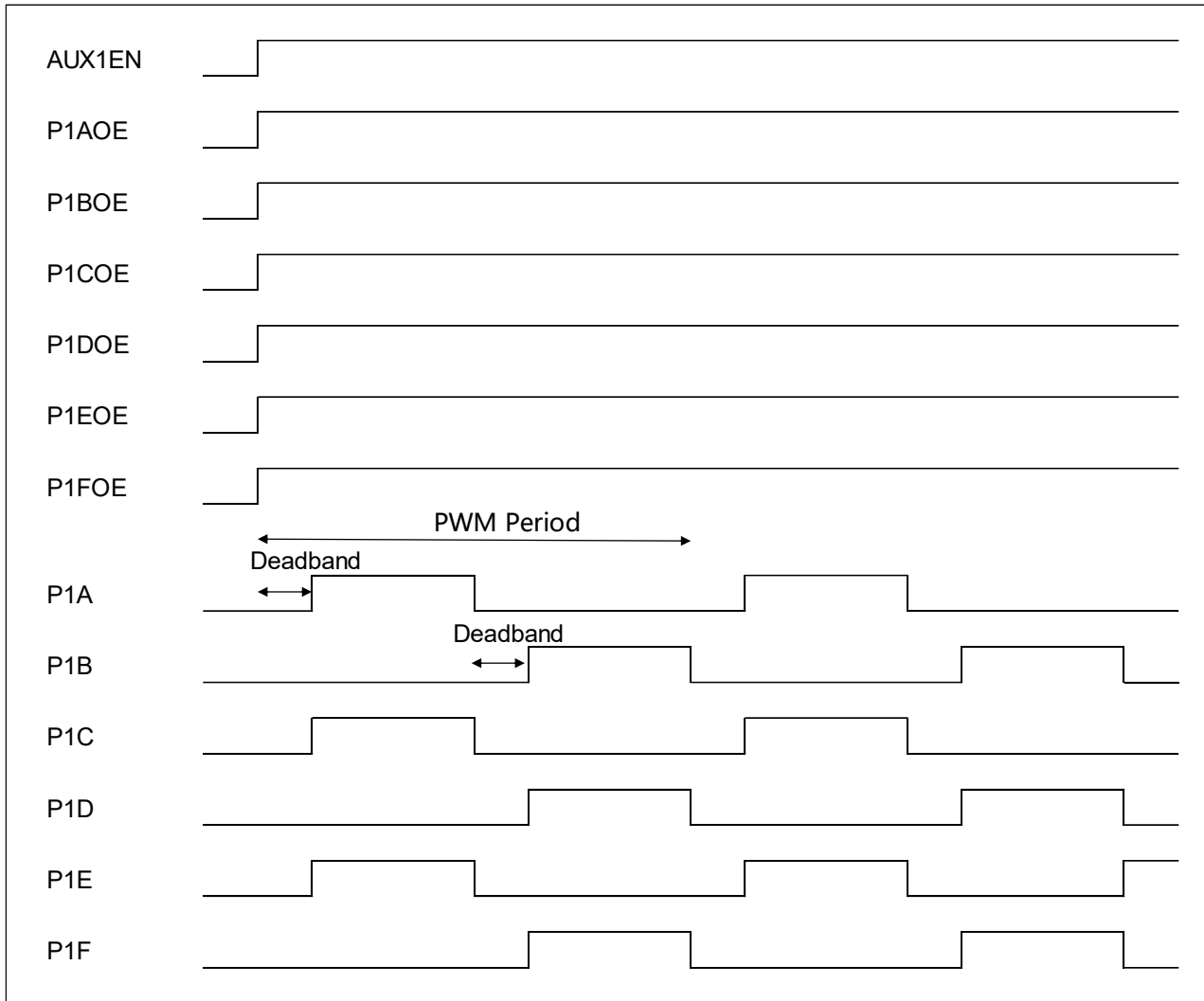


Figure 10-16 3 pairs of PWM Output (Auxiliary Function)

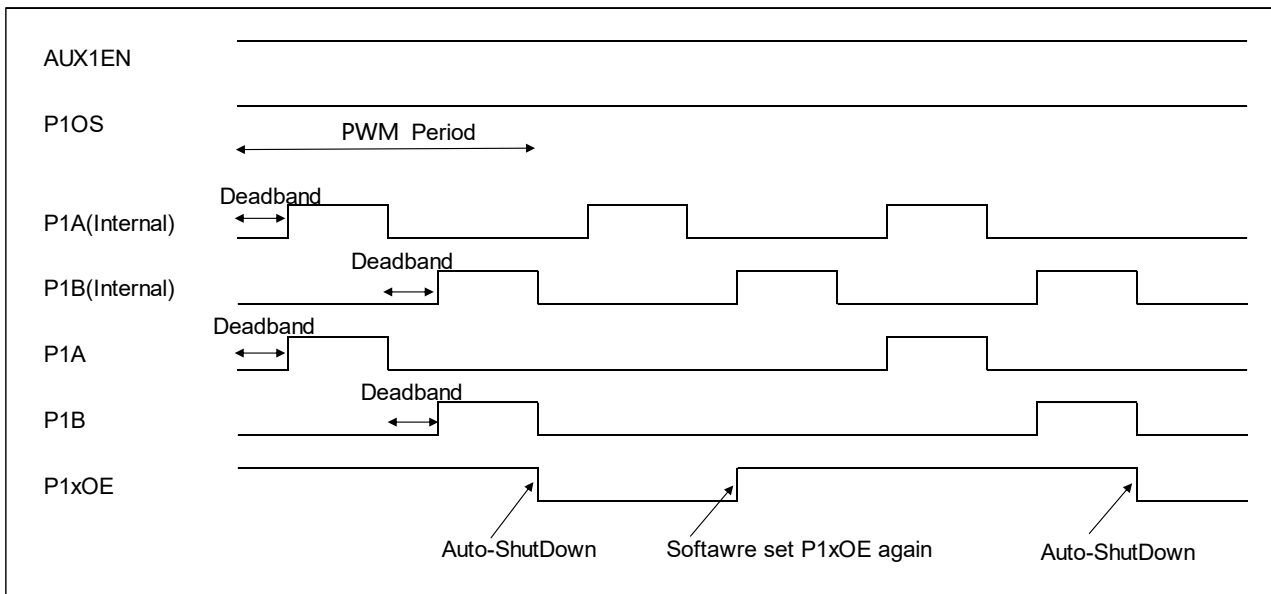


Figure 10-17 PWM one-pulse output (Auxiliary Function)

10.4.6 PWM Configure Procedure

1. Disable the PWM pin (CCP1) output driver by setting the associated TRIS bit. The circuit must connect with the appropriate pull-up/pull-down resistor to turn off power switches
2. Set the PWM period by loading the PR2 register. (See “PR2”)
3. Configure the ECCP module for the PWM mode , and select output mode and polarity.(See “P1M”, “CCP1M”);
4. Set the PWM duty cycle. (See “CCPR1L”, “DC1B”)
5. Configure and start Timer2:
 - Clear the TMR2IF interrupt flag bit of the PIR1 register.
 - Set the Timer2 prescale value. (See “T2CKPS”)
 - Select Timer2 clock source.(See “T2CKSRC”)
 - Enable Timer2 by setting the TMR2ON bit of the T2CON register.
6. Enable PWM output after a new PWM cycle has started:
 - Wait until Timer2 overflows (TMR2IF bit of the PIR1 register is set).
 - Configure PWM1AUX, set AUX1EN bit, other bits configured according to application
 - The PWM pin should be configured as digital input by setting TRISx = 1

Enable the CCP1 pin output driver by clearing the associated TRIS bit. le the PWM pin (CCP1) output driver by setting the associated TRIS bit.

Note:

1. Changing the polarity configuration while the PWM pin output drivers are enabled is not recommended since it may result in damage to the application circuits.
2. It can not stop PWM output by turn off ECCP mode because the I/O is in output mode and the value is uncertain. Two methods to stop PWM output:
 - a. The PWM pin configured as digital input by setting TRISx = 1 and connect pull-up/pull-down resistor.
 - b. Set ECCPASE = 1, ECCPAS[2:0] ≠ 000, shutdown ECCP output.

11. DATA EEPROM

FT61FC2x has a 256 x 8-bit non-volatile DATA EEPROM memory array separately from the main program. The array has a typical R/W endurance of 1 M cycles. It is R/W accessible by instructions. One byte (8-bit) is written or read. There is no page mode. Erase/program is self-timed, eliminating instruction queries and saving limited code space. This allows WRITE to take place in the background while the CPU runs unhindered, or even to enter SLEEP.

READ takes two instruction clock cycles, whereas WRITE takes $T_{WRITE-EEPROM}$ (2 ~ 4 ms if Auto-Erase is enabled, 0.7 ~ 1.3 ms if Auto-Erase is disabled). There is an on-chip charge pump so there is no need to supply an external high voltage for erase and program. An interrupt flag is set when WRITE finishes.

There is no sequential READ or sequential WRITE. The address must be updated every time.

Any voltage above V_{POR} , which can be as low as 1.5V from die to die and at high temperature, will be able to run the CPU at 8MHz, 2T. The $V_{DD-WRITE}$ for writing DATA EEPROM is higher. Minimum $V_{DD-WRITE}$ is 1.9V and 2.2V for Temperature Grade 2 and Grade 1 respectively. Reading DATA EEPROM has no such minimum V_{DD} restriction (see $V_{DD-READ}$).

11.1 Summary of DATA EEPROM Related Registers

| Name | Status | Register | Addr. | Reset |
|-------|--|------------|-------|--------------|
| EEDAT | DATA EEPROM data | EEDAT[7:0] | 0x9A | RW-0000 0000 |
| EEADR | DATA EEPROM address | EEADR[7:0] | 0x9B | RW-0000 0000 |
| WREN3 | <u>DATA EEPROM Write Enable</u> (bit 3) 111 = Enables, reset to 000 after finished (others) = Disables | EECON1[5] | 0x9C | RW-0 |
| WREN2 | DATA EEPROM Write Enable (bit 2) | EECON1[4] | | RW-0 |
| WRERR | <u>DATA EEPROM Write Error?</u> 1 = Premature terminated (MCLR or WDT Reset) 0 = No | EECON1[3] | | RW-x |
| WREN1 | DATA EEPROM Write Enable (bit 1) | EECON1[2] | | RW-0 |
| RD | <u>DATA EEPROM Reading?</u> 1 = Yes (remains for 4 SysClk cycles, then = 0) 0 = No | EECON1[0] | | RW-0 |
| WR | <u>DATA EEPROM Write Busy?</u> 1 = Programming (reset to 0 after finished) 0 = Finished | EECON2[0] | 0x9D | RW-0 |

Table 11-1 Instruction Level EEPROM Related Control Registers

| Name | Status | Register | Addr. | Reset |
|------|------------------------------------|-----------|--------------------------------|-------|
| GIE | Global Interrupt | INTCON[7] | 0x0B 0x8B 0x10B 0x18B | RW-0 |
| PEIE | Master Peripheral Interrupt | INTCON[6] | | RW-0 |
| EEIE | EEPROM program finished Interrupt | PIE1[7] | 0x8C | RW-0 |
| EEIF | EEPROM program finished Interrupt? | PIR1[7] | 0x0C | RW-0 |

Table 11-2 EEPROM Interrupt Enable and Status Bits

11.2 Writing DATA EEPROM

1. Set "GIE = 0";
2. If "GIE = 1", then repeat (1);
3. Write target address to EEADR;
4. Write target data EEDAT;
5. Set "WREN3, WREN2, WREN1" = "1, 1, 1" and maintain throughout the programming.
6. Must immediate set "WR = 1" to initiate write (otherwise will abort).
7. After programming completed (see T_{WRITE-EEPROM} for write time), "WR = 0" and "WREN3, WREN2, WREN1" = "0, 0, 0" set automatically;

Program Example:

```

BCR INTCON, GIE
BTSC INTCON, GIE
LJUMP $-2
BANKSEL EEADR
LDWI 55H
STR EEADR           ; address is 0x55
STR EEDAT           ; data is 0x55
LDWI 34H
STR EECON1         ; set WREN3/2/1 at the same time
BSR EECON2, 0      ; start writing
BSR INTCON, GIE    ; set GIE
    
```

Note:

1. Data EEPROM Read while the array is still in programming will yield an incorrect result.
2. If any one of WREN3, WREN2 or WREN1 clears before programming is finished, EEIF flag should be cleared before the next programming.

11.3 Reading DATA EEPROM

Set EEADR register, then initiate read (“RD = 1”). Data will be available in the EEDAT register after 2 instruction cycles, a NOP must be inserted after the read request. The EEDAT will be unchanged until the next READ or WRITE instruction.

The following is an example on how to read the DATA EEPROM:

```
BANKSEL EEADR  
LDWI dest_addr  
STR EEADR  
BSR EECON1, RD  
NOP ; Waiting to read  
LDR EEDAT, W ; Data is read by instruction
```

11.4 Auto-Erase Function

Writing data into a byte involves two steps: a byte erase followed by a byte program. Erase sets all the bits in the byte to “1” while program can selectively program individual bits to “0”. This device has a built in Auto-Erased function, where an erase always precede program. Except for high temperature it is recommended to turn on Auto-Erase.

If Auto-erase is enabled, Programming FF multiple times will erase the byte multiple times. However programming non-FF multiple times is the same as programming the byte once, as every time the bit programs it will be auto-erased first.

12. 10-bit ANALOG TO DIGITAL CONVERTER, ADC

The ADC converts an analog input signal to a 10-bit digital data. It can run at different clock speeds, and has a true 10-bit accuracy for clock speeds up to 1 MHz (or 60 kHz sampling rate, 16 μ s/sampling equivalent).

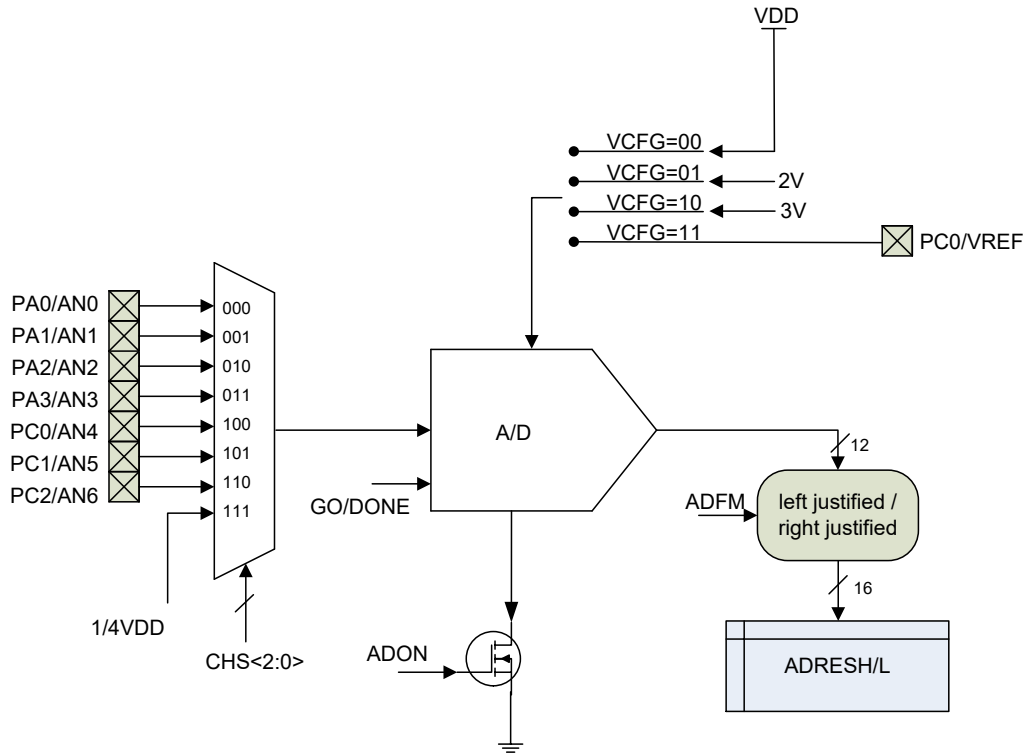


Figure 12-1 ADC block diagram

Analog Input can be one of 3 internal voltage references or any one of the 7 I/O. ADC can be triggered by an instruction or ECCP special event trigger. A delay can be added between triggering and ADC sampling.

The ADC can set interrupt flags upon completion of a conversion. The interrupt flags can be used to Wake-Up the CPU from SLEEP and/or executing an INTERRUPT.

The ADC voltage reference ($V_{ADC-REF}$) can be instructions selected to V_{DD} , one of 2 internal voltage references (2V, 3V), or an external voltage reference via an I/O.

The ADC runs in the background, freeing the CPU for other chores. It requires no calibration.

If ADC clock source is not the LIRC during SLEEP, ADC will turn off automatically.

If it is NOT software enabled, instruction GO/DONE will be ignored, GO/DONE will be updated by hardware.

There are three time points that an user need to pay attention to when using ADC when in high sampling rate situations.

1. When a channel starts sampling.
2. When sampling ends. This is the instance the voltage on the selected channel is to be measured.
3. When conversion data is ready.

12.1 Summary of ADC Related Registers

| Name | Status | Register | Addr. | Reset |
|------|--|-----------|-----------------------|-------|
| GIE | Global Interrupt 1 = Enables (PEIE, ADCIE apply) 0 = <u>Global Disables</u> (Wake-Up enable) | INTCON[7] | 0x0B 0x8B 0x10B | RW-0 |
| PEIE | Master Peripheral Interrupt 1 = Enables (ADCIE apply) 0 = <u>Disables</u> (no Wake-Up) | INTCON[6] | | RW-0 |
| ADIE | ADC Conversion Completed Interrupt 1 = Enables 0 = <u>Disables</u> (no Wake-Up) | PIE2[1] | 0x8D | RW-0 |
| ADIF | ADC Conversion Completed Interrupt? 1 = Yes (latched) 0 = <u>No</u> | PIR2[1] | 0x0D | RW-0 |

Table 12-1 ADC Interrupt Enable and Status bits

| Name | Status | Register | Addr. | Reset | |
|---------|--|-------------|-------|--------------|------|
| ADRESL | <u>ADC Conversion Result (LSB)</u> ADFM=0: ADRESL[7:6] = 2 LSB (rest are "0") ADFM=1: ADRESL[7:0] = 8 LSB | ADRESL[7:0] | 0x9E | RW-xxxx xxxx | |
| ADRESH | <u>ADC Conversion Result (MSB)</u> ADFM=0: ADRESH[7:0] = 8 MSB ADFM=1: ADRESH[3:0] = 4 MSB (rest are "0") | ADRESH[7:0] | 0x1E | RW-xxxx xxxx | |
| ADFM | <u>A/D Conversion Result Format (see "ADRESH")</u> 1 = Right justified 0 = <u>Left justified</u> | ADCON0[7] | 0x1F | RW-0 | |
| VCFG | <u>V_{ADC-REF}</u> 00 = V _{DD} 01 = Internal 2V 10 = Internal 3V 11 = External Reference (I/O) (*) (*) Effective only when ANSEL[4] = 1; | ADCON0[6:5] | | RW-00 | |
| CHS | <u>ADC Input</u> 000 = AN0 001 = AN1 010 = AN2 011 = AN3 100 = AN4 101 = AN5 110 = AN6 111 = Internal 1/4 V _{DD} (*) (*) Effective only when ANSEL[7] = 1; | ADCON0[4:2] | | RW-000 | |
| GO/DONE | <u>ADC Conversion Start and Status</u> 1 = Start initiates by Software or ECCP (automatic clear upon completion) 0 = <u>Completed / Not in progress</u> | ADCON0[1] | | RW-0 | |
| ADON | 1 = ADC Enables 0 = <u>ADC Disables</u> (consumes no current) | ADCON0[0] | | RW-0 | |
| DIVS | <u>ADC divide clock source select bit</u> 1 = LIRC 0 = <u>Sysclk</u> | ADCON1[7] | | 0x9F | RW-0 |

| Name | Status | Register | Addr. | Reset | |
|------|---|--|------------|-------------------------|--------|
| ADCS | <u>ADC Conversion Clock Source</u> DIVS = 0 DIVS = 1 TSEL = 2T TSEL = 4T TSEL = 2T/4T 000 = Sysclk/2 000 = Sysclk/4 000 = LIRC/2 001 = Sysclk/8 001 = Sysclk/16 001 = LIRC/8 010 = Sysclk/32 010 = Sysclk/64 010 = LIRC/32 100 = Sysclk/4 100 = Sysclk/8 100 = LIRC/4 101 = Sysclk/16 101 = Sysclk/32 101 = LIRC/16 110 = Sysclk/64 110 = Sysclk/128 110 = LIRC/64 x11 = LIRC (*) x11 = LIRC (*) x11 = LIRC (*) (*) LIRC = 32kHz/256kHz, depend on LFMOD | | | ADCON1[6:4] | RW-000 |
| | ANSEL | 1 = Disables Pull-Up / Pull-Down, Digital Input (8 ADC ports only) 0 = (no action) | ANSEL[7:0] | 0x91 RW-1111 1111 | |

Table 12-2 Instruction Level I/O related registers

| Name | Addr. | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | Bit 2 | bit 1 | bit 0 | Reset |
|--------|-------|-------------------------------|-----------|----------|-------|-------|---------|-------|--------------|-----------|
| ADRESL | 0x9E | A/D Result Register Low Byte | | | | | | | | xxxx xxxx |
| ADRESH | 0x1E | A/D Result Register High Byte | | | | | | | | xxxx xxxx |
| ADCON0 | 0x1F | ADFM | VCFG<1:0> | CHS<2:0> | | | GO/DONE | ADON | 0000 0000 | |
| ADCON1 | 0x9F | DIVS | ADCS<2:0> | | | - | | | 0000 ---- | |

Table 12-3 ADC related registers' addresses

12.1 ADC Configurations

Configuring the ADC involves setting (set ADON=0 to turn off triggering when changing configurations):

- Channel(s) selection
- ADC voltage reference
- ADC clock source
- Result formatting
- Triggering source
- Response (Interrupt settings)

Channel(s) Selection – The channel connected to the sample and hold circuit for ADC conversion is determined by the CHS register. The I/O should be configured as analog input by setting TRISx = 1 and ANSEL0x = 1.

ADC Voltage Reference (V_{ADC-REF}) – ADC measures the input analog voltage relative to two reference voltages: V_{REF+} and GND. The reference voltages can be

- VDD
- Internal voltage reference2V
- Internal voltage reference3V
- External voltage source (V_{REF} is PC0)

ADC Clock Selection –ADC has 13 instruction-selectable clock frequency (see “ADCS” in [Table 12-2](#)):

- DIVS = 0, SysClk/N (TSEL = 2T) or SysClk/2N(TSEL = 4T) or LIRC; N = 2, 4, 8, 16, 32, 64
- DIVS = 1, LIRC/N; N = 1, 2, 4, 8, 16, 32, 64
- LIRC (256 kHz or 32 kHz, see “LFMOD” in [Table 6-2](#))

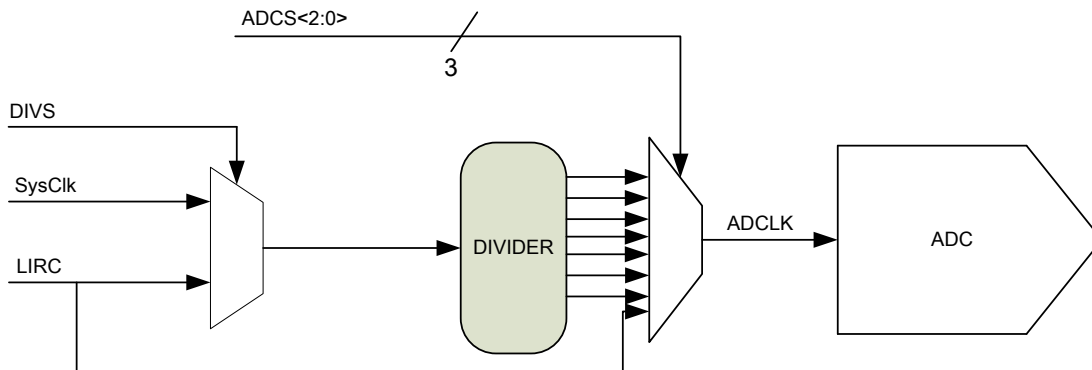


Figure 12-2 ADC clock configurations

Result formatting – A/D conversion result can be stored left or right justified (see “ADFM” in [Table 12-2](#)).

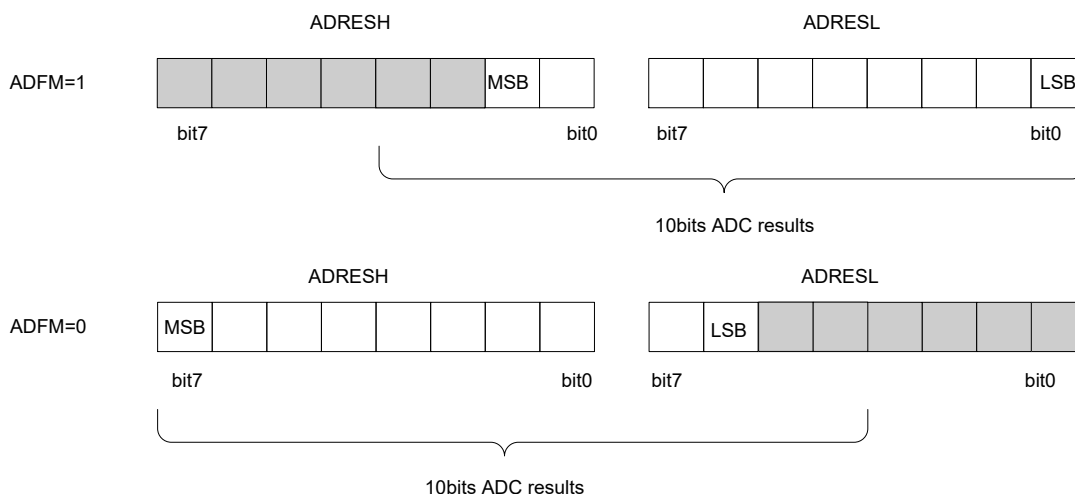


Figure 12-3 ADC conversion result format

12.1.1 ADC triggering

The ADC can be triggered by instruction (GO/DONE= 1) or ECCP special event trigger. GO/DONE is effective immediately if it is software written. If ADC triggered by ECCP special event, ADC conversion start automatically when TMR1H/L matches CCPR1H/L.

Note: Triggers arriving before the completion of ADC are ignored.

12.1.2 Aborting an ADC

Sometimes it needs to abortion an ADC. An example is to start a new ADC sampling.

- ADC can be aborted by software setting GO/DONE = 0.

- If ADC triggered by special event, the abortion must be done by disabling the ADC (ADON = 0)
- ADRESH and ADRESL are not update with the partially complete ADC conversion sample. It will retain the value of the previous conversion.
- A System-Reset will turn off the ADC module and ADC will abort, as registers reset.

12.1.3 Interrupt

Interrupt flag ADCIF is set to 1 when the ADC conversion is complete. Depends on the enable controls (GIE, PEIE and ADCIE) it may result in an AWAKE from SLEEP and/or Interrupt.

12.2 ADC Acquisition Time

The acquisition time, in this case the sample and hold time, must be long enough for the internal ADC voltage to be within 0.01% of the pad voltage to achieve 10 bits accuracy (0.097%). The relationship between acquisition time and external series resistance is as follow (**Table 12-4**):

$T_{ACQ} > 0.09 \times (R + 1) \mu s$; where R is in kW.

For a T_{ACQ} of 2 μs , the external series resistance should be ≤ 21 kW. T_{ACQ} is proportional higher if a larger series resistance is used. The largest series resistance allowed is junction leakage limited. For a junction leakage of 5nA, there is 0.25mV (0.0125% for a 2V reference) voltage drop across a 50 kW series resistor. The junction leakage current could be substantially higher for temperature above 100°C. As a result a much smaller series resistance should be used.

| Resistance | T_{ACQ} |
|-----------------|-------------------|
| > 50 k Ω | (not recommended) |
| 43 k Ω | $\geq 4.0 \mu s$ |
| 21 k Ω | $\geq 2.0 \mu s$ |
| < 21 k Ω | $\geq 2.0 \mu s$ |

Table 12-5 Minimum T_{ACQ} for different external series resistance

The sample and hold time is the time when the pad voltage is seen by the internal ADC.

Beginning of hold = end of channel switching (see “CHS”) or ADC ready (see T_{ST}), whichever is later.

End of hold = T_{SysClk} / N ¹ (N =2 for 2T, 4 for 4T) after the end of delay, at the moment the switch of the sample and hold circuit switches from close to open.

The sampling point = the instant right before the switch opens.

Conversion starts after the switch is opened, with data ready after a time of 13.5 – 14.5 T_{AD} . Hence from GO to data ready a time of 13.5 T_{AD} to 14.5 T_{AD} is required. The switch is re-closed after data is ready and the next cycle of sampling begins meanwhile, the switch have to remain closed for a minimum time T_{ACQ} to start A/D conversion again.

12.3 ADC Minimum Sampling Time

T_{AD} is the ADC clock period. A full 10-bit conversion takes at a minimum

¹ $T_{SysClk} / N = 0.125\mu s$ (16M/2T) or $0.250\mu s$ (16M/4T);

$$T_{ACQ} + 14.5 \times T_{AD}$$

The maximum conversion rate to guarantee a true 10-bit accuracy is 60 kHz (or ~16 μs per conversion).

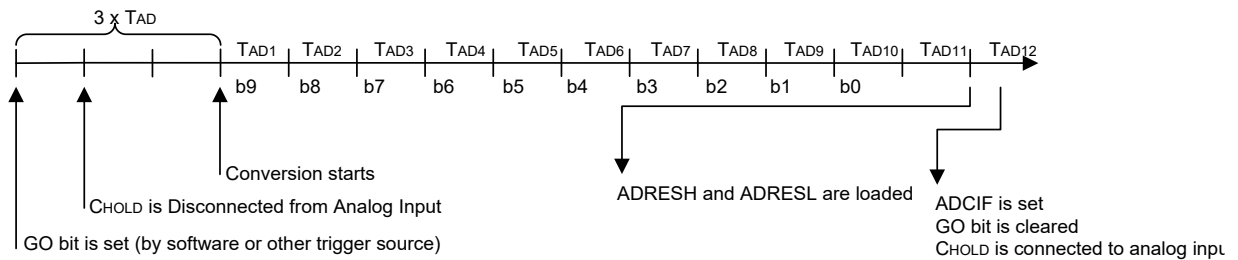


Figure 12-4 Analog to digital conversion T_{AD} period

12.4 Sample ADC Flow

Setting up the ADC:

1. Configure Port:
 - a. Disable pin output driver by setting $TRISx = 1$
 - b. Disable Digital Input, Weak Pull-Up and Weak Pull-Down by setting $ANSELx = 1$
2. Configure the ADC module:
 - a. Select ADC clock source
 - b. Select ADC voltage references
 - c. Select ADC trigger: GO/DONE or CCP1 special event trigger
 - d. Select data format
3. Configure ADC interrupt if necessary:
 - a. Enable ADC interrupt
 - b. Enable peripheral interrupt
 - c. Disable global interrupt (enable if Interrupt Service Routine is to be executed)
4. Turn on the ADC module. There is a ~15 μs setup time (T_{ST}) before the ADC is ready, and another setup time (T_{VRINT}) before the Internal voltage reference is ready if $V_{ADC-REF}$ choose it (see " T_{VRINT} ", [Section 18.7](#)), whichever is later.

The ADC is now ready to sample the different channels. To sample a channel:

1. Select the ADC input to be the channel measured (see "CHS").
2. Clear ADC interrupt flag(s) if necessary
3. There is a minimum required time, T_{ACQ} , to charge the ADC input capacitance to within 0.01% of the input pad voltage. Depending on the type of trigger, a delay may be required after switching channel or end of an ADC conversion, whichever is later, and the triggering.
 - a. For software trigger, an additional T_{ACQ} is required.
 - b. For ECCP special event trigger, an additional T_{ACQ} is required.
 - c. Same for PWM trigger.
5. After the required delay, set GO/DONE by instructions, or wait for hardware trigger to start conversion.

6. The completion of ADC can be find by:
 - a. Polling the GO/DONE
 - b. Waiting for the ADC interrupt (if enabled)
7. Read ADC Result
8. Clear the ADC or Threshold comparison interrupt flag if necessary.

Notes:

1. Although GO/DONE and ADON shares the same register, they should not be set simultaneously.
2. The configurations should not be changed during ADC conversion or awaiting external trigger.

The following is an ADC program example sampling PA0 and using LIRC as the ADC clock:

```
BANKSEL ADCON1
LDWI B'00110000' ; ADC LIRC clock
STR ADCON1

BANKSEL TRISA
BSR TRISA, 0 ; Set PA0 to input
BANKSEL ANSEL
BSR ANSEL, 0 ; Set-PA0 to analog

BANKSEL ADCON0
LDWI B'10000001' ; Right justify,
STR ADCON0 ; VDD, Vref, AN0, On

LCALL StableTime ; ADC stable time
LCALL SampleTime ; Acquisition delay, TACQ

BSR ADCON0, GO ; Start conversion
BTSC ADCON0, GO ; Conversion done?
LJUMP $-1 ; No, test again

BANKSEL ADRESH;
LDR ADRESH, W ; Read upper 2 bits
STR RESULTHI ; Store in SRAM space
BANKSEL ADRESL;
LDR ADRESL, W ; Read lower 8 bits
STR RESULTLO ; Store in SRAM space
```


13. COMPARATOR

FT61FC2x embeds two analog comparators, they are used to interface analog circuits to a digital circuit by comparing two analog voltages and providing a digital indication of their relative magnitudes. Comparator C1/C2 can configure as multiple comparator configurations in input and output connection, the output polarity is programmable and can output to I/O pin (PA2/PC4). The Internal programmable reference voltage V_{REF} can be used as comparator input. The output of Comparator C2 can be configured as Timer1 gate source

Comparator maintain running in SLEEP mode (CM≠000 or 111). The comparator interrupt flag is set whenever there is a change in the output value of the comparator, and it may result in an AWAKE from SLEEP and/or Interrupt.

13.1 Summary of Comparator Related Registers

| Name | Status | Register | Addr. | Reset |
|-------|--|--|-------------|--------------|
| C2OUT | <u>Comparator C2 output</u> | | | RW-0 |
| | C2INV = 0: 1 = $V_{IN+} > V_{IN-}$ 0 = $V_{IN+} < V_{IN-}$ | C2INV = 1: 1 = $V_{IN+} < V_{IN-}$ 0 = $V_{IN+} > V_{IN-}$ | | |
| C1OUT | <u>Comparator C1 output</u> | | | RW-0 |
| | C1INV = 0: 1 = $V_{IN+} > V_{IN-}$ 0 = $V_{IN+} < V_{IN-}$ | C1INV = 1: 1 = $V_{IN+} < V_{IN-}$ 0 = $V_{IN+} > V_{IN-}$ | | |
| C2INV | <u>Comparator C2 output polarity</u> | 1 = Inverted 0 = <u>Not inverted</u> | CMCON0[5] | RW-0 |
| C1INV | <u>Comparator C1 output polarity</u> | 1 = Inverted 0 = <u>Not inverted</u> | CMCON0[4] | RW-0 |
| CIS | <u>Comparator Input Switch</u> | | CMCON0[3] | 0x19 RW-0 |
| | CM = 001: 1 = C1 V_{IN-} connects to C1IN+(PA0) 0 = C1 V_{IN-} connects to C1IN- (PA1) CM = 010: 1 = C1 V_{IN-} connects to C1IN+(PA0), C2 V_{IN-} connects to C2IN+(PC0) 0 = C1 V_{IN-} connects to C1IN- (PA1), C2 V_{IN-} connects to C2IN-(PC1) | | | |
| CM | <u>Comparator mode</u> | | CMCON0[2:0] | RW-000 |
| | 000 = <u>Comparators off. CxIN pins are configured as analog</u> 001 = 2 comparators, common reference, 3 inputs 010 = 2 comparators, Internal reference V_{REF} , 4 inputs 011 = 2 comparators, common reference, 2 inputs 100 = 2 independent comparators 101 = 1 independent comparator 110 = 2 common reference comparators with outputs, common reference, 2 inputs 111 = Comparators off. CxIN pins are configured as digital I/O | | | |

| Name | Status | Register | Addr. | Reset |
|--------|---|------------|-------|--------|
| VREN | <u>CV_{REF}</u> 1 = CV _{REF} circuit powered on 0 = CV _{REF} circuit powered down, no IDD drain | VRCON[7] | 0x99 | RW-0 |
| VRR | <u>CV_{REF} Ranges</u> 1 = Low range 0 = High range | VRCON[5] | | RW-0 |
| VR | <u>CV_{REF} Value</u> VRR = 1: CV _{REF} = (VR<3:0>/24)*VDD VRR = 0: CV _{REF} = VDD/4 + (VR<3:0>/32)*VDD | VRCON[3:0] | | RW-000 |
| T1GSS | <u>Timer1 Gate Source</u> 1 = T1G pin (pin should be configured as digital input) 0 = Comparator C2 output | CMCON1[1] | 0X1A | RW-1 |
| C2SYNC | <u>Comparator C2 Output Synchronization</u> 1 = Output is synchronized with falling edge of Timer1 clock 0 = Output is asynchronous | CMCON1[0] | | RW-0 |

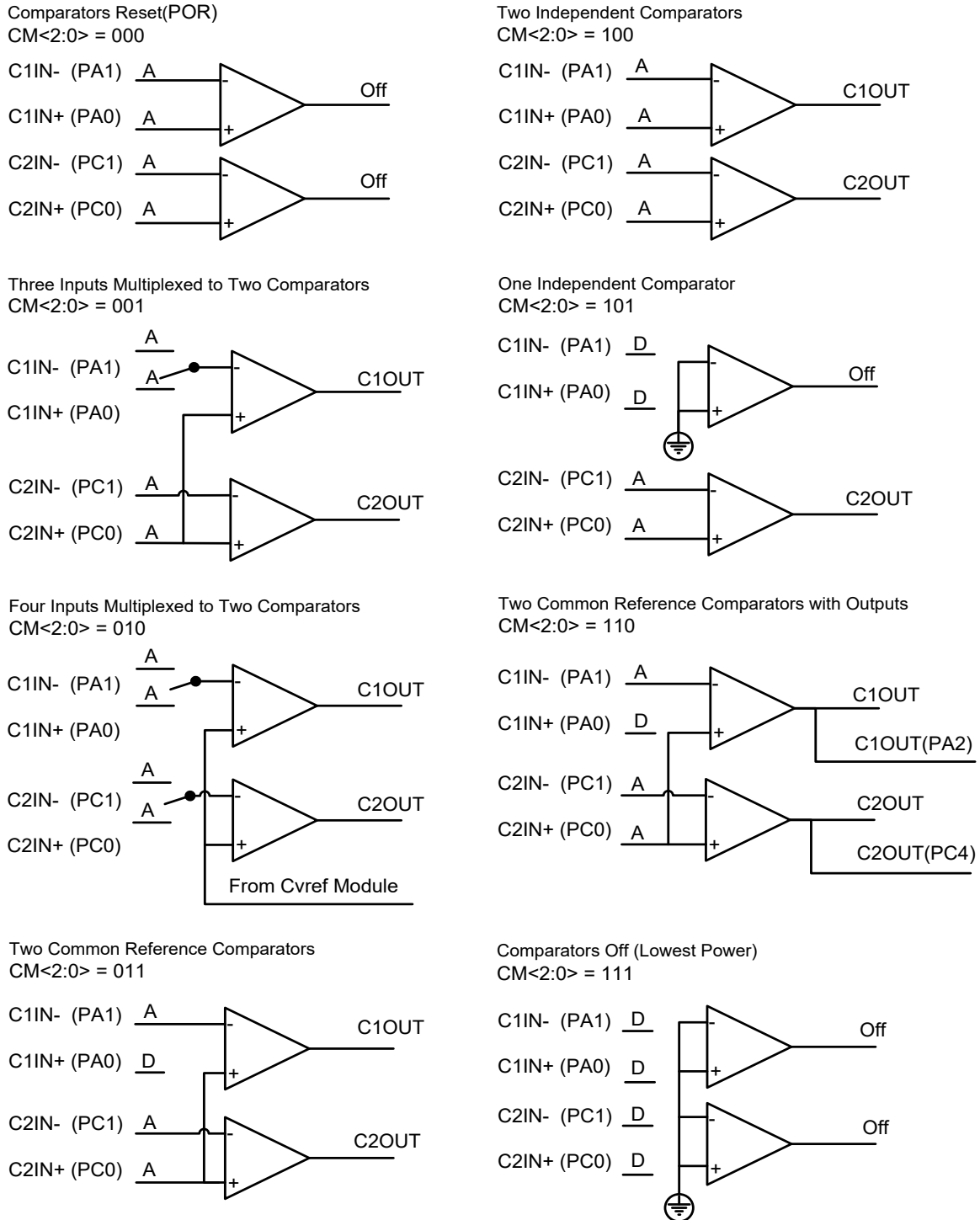
Table 13-1 Instruction Level Comparator Related Control Registers

| Name | Status | Register | Addr. | Reset |
|------|---------------------------------------|-----------|-----------------------|-------|
| GIE | Global Interrupt | INTCON[7] | 0x0B 0x8B 0x10B | RW-0 |
| PEIE | Master Peripheral Interrupt | INTCON[6] | | RW-0 |
| C2IE | Comparator 2 output changed interrupt | PIE1[4] | 0x8C | RW-0 |
| C2IF | Comparator 2 output changed? | PIR1[4] | 0x0C | RW-0 |
| C1IE | Comparator 1 output changed interrupt | PIE1[3] | 0x8C | RW-0 |
| C1IF | Comparator 1 output changed? | PIR1[3] | 0x0C | RW-0 |

Table 13-2 Comparator Interrupt Enable and Status Bit

13.2 Comparator Configuration

There are eight modes of operation for the comparator, see **Figure 13-1**. Comparator interrupts should be disabled during a Comparator mode change to prevent unintended interrupts.



Note:
A: Analog input(ANSELx = 1), Read as '0'
D: Digital input

Figure 13-1 Comparator 1/2 Operating modes

Analog input port — The I/O should be configured as analog input by setting TRISx = 1 and ANSEL0x = 1

The analog input pins share their connection with a digital input, they have reverse biased ESD protection diodes to VDD and VSS. The analog input, therefore, must be between VSS and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur. A maximum source impedance of 10 kΩ is recommended for the analog sources. Also, any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current to minimize inaccuracies introduced.

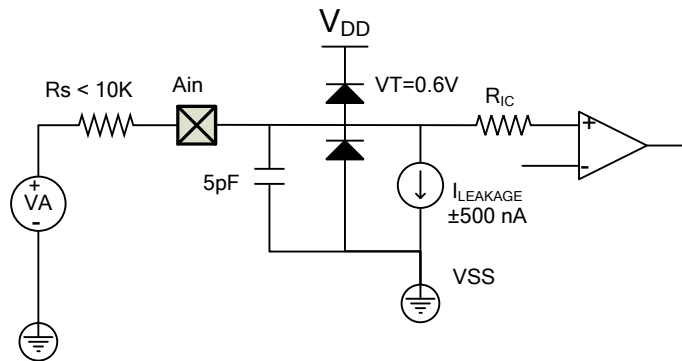


Figure 13-2 Comparator analog input mode

Compare result output — The comparator outputs are directed to the I/O pin PA2/PC4 (CM = 110), the TRIS bits for the associated CxOUT pins must be cleared to enable the output drivers.

Comparator Response Time — The comparator output is indeterminate for a period of time after the change of an input source or the selection of a new reference voltage. This period is referred to as the response time. The response time of the comparator differs from the settling time of the voltage reference. Therefore, both of these times must be considered when determining the total response time to a comparator input change. See [Section 18.8](#).

Note: When either comparator is first enabled, bias circuitry in the Comparator module may cause an invalid output from the comparator until the bias circuitry is stable. Allow about 1 μs for bias settling then clear the mismatch condition and interrupt flags before enabling comparator interrupts.

Programmable reference voltage CVREF —One of the comparator input can be configured as internal programmable reference voltage CVREF (CM = 010). See "VREN", The CVREF voltage reference has 2 ranges with 16 voltage levels in each range, which is directly proportional to VDD

High range (VRR = 0): $CV_{REF} = VDD/4 + (VR<3:0>/32)*VDD$

Low range (VRR = 1): $CV_{REF} = (VR<3:0>/24)*VDD$

See [Figure 13-3](#), The full range of VSS to VDD cannot be realized due to the construction of the module. The CVREF output voltage can be set to GND with no power consumption by configuring VRCON as follows, This allows the comparator to detect a zero-crossing while not consuming additional CVREF module current.:

```
BCR    VRCON,VREN    ;Close CVREF
```

```
CLRR   VRCON        ;VR<3:0> = 0000
```

```
BSRVRCON,VRR    ; CVREF low range
```

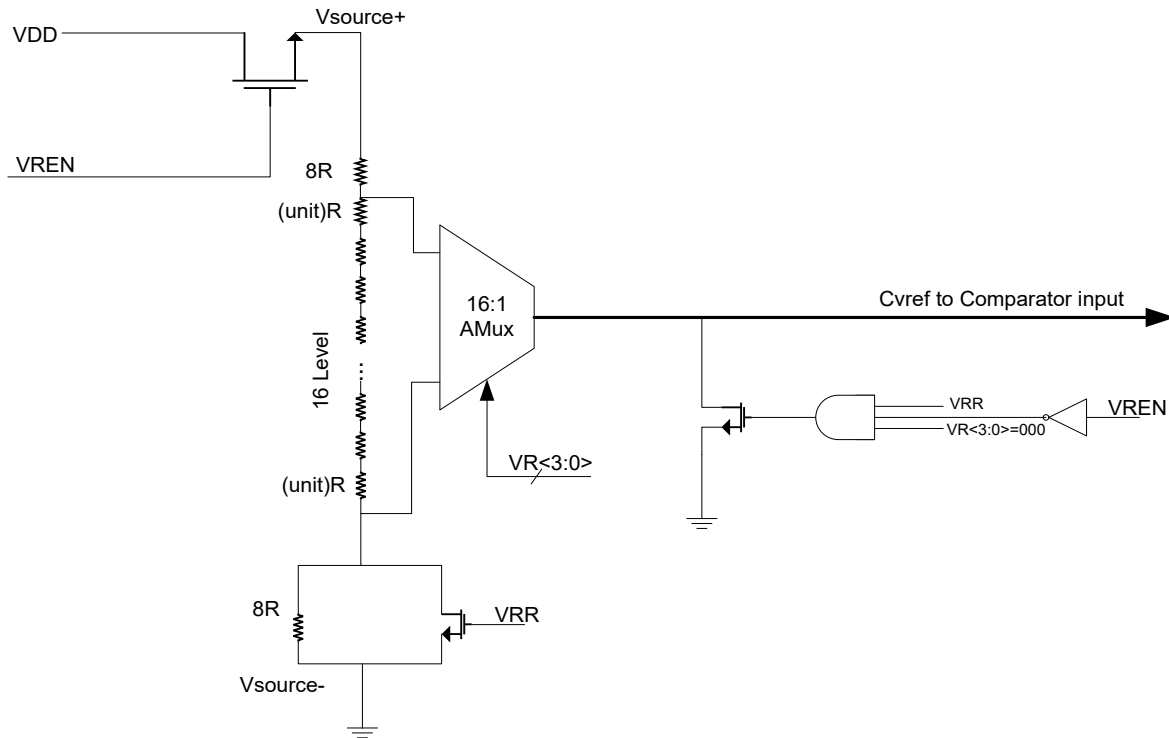


Figure 13-3 Block diagram of Comparator voltage reference

13.2.1 Comparator Interrupt

An Interrupt flag CxIF is set to 1 when the output of the Comparator 1/2 is changed, Software will need to maintain information about the status of the comparator output to determine the actual change that has occurred (Read CxOUT). Depends on the enable controls (GIE, PEIE, C1IE, C2IE) it may result in an AWAKE from SLEEP and/or Interrupt.

Note:

1. Any read or write of CMCON0. This will end the mismatch condition.
2. The CxIF interrupt flag must cleared by software. A persistent mismatch condition will preclude clearing the CxIF interrupt flag. Reading CMCON0 will end the mismatch condition and allow the CxIF bit to be cleared.
3. If CxOUT If a change in the CxOUT should occur when a CMCON0 read operation is being executed then the CxIF Interrupt flag may not get set.

13.2.2 Comparator 2 Gating Timer1

When the Timer1 gate source is software configurable to be the output of Comparator C2, this feature can be used to time the duration or interval of analog events See [Section 7.3.3](#) "Timer1 Gate".

14. VOLTAGE REGULATOR(VREG)

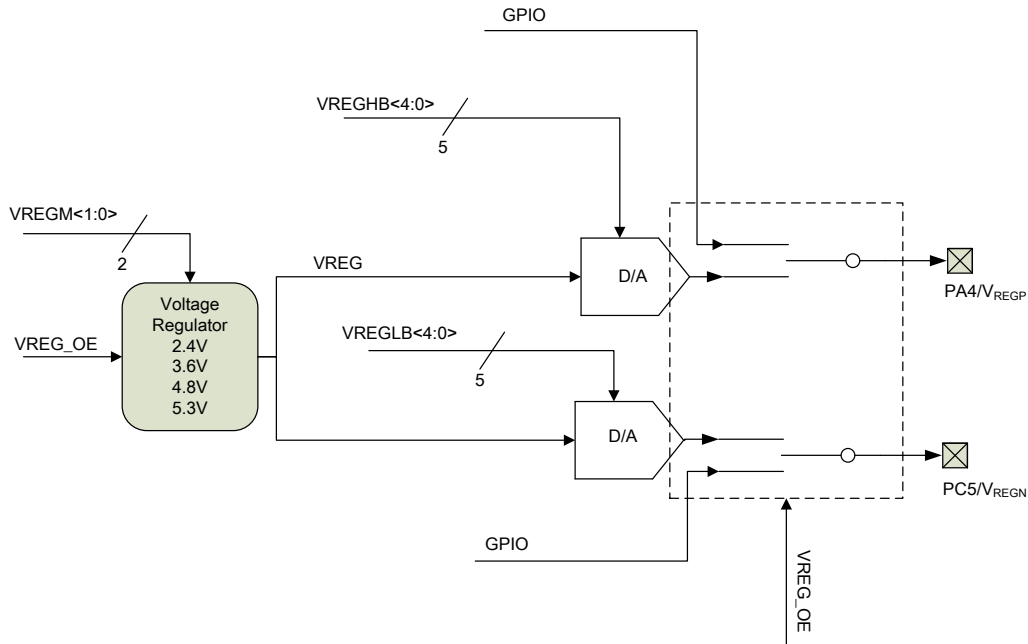


Figure 14-1 Voltage Regulator output diagram

FT61FC2X built-in 2 ways regulator output, each output up to 32 stalls voltage. Output voltage is determined by the following equations:

Equation 14-1 $V_{OUT} = V_{REG} * (VREGHB + 1) / 32$ (V_{REGP} , PA4 output)

Equation 14-2 $V_{OUT} = V_{REG} * (VREGLB + 1) / 32$ (V_{REGN} , PC5 output)

14.1 Summary of Voltage Regulator Related Registers

| Name | Status | Register | Addr. | Reset |
|---------|--|------------|-------|---------|
| VREG_OE | <u>VREG Output</u> 1 = Enables (PA4, PC5 output VREG) 0 = Disables (PA4, PC5 is GPIO) | MSCKCON[6] | 0x1B | RW-0 |
| VREGM | <u>VREG Select</u> 00 = 2.4V 10 = 4.8V 01 = 3.6V 11 = 5.3V | VCON1[6:5] | 0x108 | RW-00 |
| VREGHB | <u>High range (PA4) Output</u> $V_{OUT} = V_{REG} * (VREGHB + 1) / 32$ | VCON1[4:0] | | |
| VREGLB | <u>Low range (PC5) Output</u> $V_{OUT} = V_{REG} * (VREGLB + 1) / 32$ | VCON2[4:0] | 0x109 | RW-0000 |

Table 14-1 Instruction Level Voltage Regulator Related Control Registers

15. MEMORY READ / PROGRAM PROTECTON

The PROGRAM CODE(PROM) and DATA EEPROM(DROM) can be Array Read Protected. These protections selected at the IDE.

| Name | Functions | default |
|------|----------------------|----------|
| CPB | PROM Read Protection | disabled |

Table 15-1 BOOT Level Memory Read and/or Program Protection

16. INSTRUCTION SET

| Assembly Syntax | Function | Operation | Status |
|-----------------|--------------------------------|------------------------------------|----------|
| NOP | No operation | None | NONE |
| SLEEP | Enter SLEEP mode | 0 → WDT; Stop OSC | /PF, /TF |
| CLRWDT | Clear WDT | 0 → WDT | /PF, /TF |
| LJUMP N | Long JUMP Address | N → PC | NONE |
| LCALL N | Long CALL Subroutine | N → PC; PC + 1 → Stack | NONE |
| RETI | Return from Interrupt | Stack → PC; 1 → GIE | NONE |
| RET | Return from Subroutine | Stack → PC | NONE |
| BCR R, b | Bit Clear | 0 → R(b) | NONE |
| BSR R, b | Bit Set | 1 → R(b) | NONE |
| CLRR R | Clear Register | 0 → R | Z |
| LDR R, d (MOVF) | Load Register to d | R → d | Z |
| COMR R, d | Complement Register | /R → d | Z |
| INCR R, d | Increment Register | R + 1 → d | Z |
| INCRSZ R, d | Increment Register, Skip if 0 | R + 1 → d | NONE |
| DECR R, d | Decrement Register | R - 1 → d | Z |
| DECRSZ R, d | Decrement Register, Skip if 0 | R - 1 → d | NONE |
| SWAPR R, d | Swap Halves Register | R(0-3)R(4-7) → d | NONE |
| RRR R, d | Rotate Right Register | R(0) → C; R(n) → R(n-1); C → R(7); | C |
| RLR R, d | Rotate Left Register | R(7) → C; R(n) → R(n+1); C → R(0); | C |
| BTSC R, b | Bit Test, Skip if 0 | Skip if R(b)=0 | NONE |
| BTSS R, b | Bit Test, Skip if 1 | Skip if R(b)=1 | NONE |
| CLRW | Clear Working Register | 0 → W | Z |
| STTMD | Store W to OPTION | W → OPTION | NONE |
| CTLIO R | Control I/O Direction Register | W → TRISr | NONE |
| STR R (MOVWF) | Store W to Register | W → R | NONE |
| ADDWR R, d | Add W and Register | W + R → d | C, HC, Z |
| SUBWR R, d | Subtract W from Register | R - W → d | C, HC, Z |
| ANDWR R, d | AND W and Register | R & W → d | Z |
| IORWR R, d | OR W and Register | W R → d | Z |
| XORWR R, d | XOR W and register | W ^ R → d | Z |
| LDWI I (MOVLW) | Load Immediate to W | I → W | NONE |
| ANDWI I | AND W and imm | I & W → W | Z |
| IORWI I | OR W and imm | I W → W | Z |
| XORWI I | XOR W and imm | I ^ W → W | Z |
| ADDWI I | Add imm to W | I + W → W | C, HC, Z |
| SUBWI I | Subtract W from imm | I - W → W | C, HC, Z |
| RETW I | Return, Place imm to W | Stack → PC; I → W | NONE |

Table 16-1 37 RISC Instruction Commands

17. SPECIAL FUNCTION REGISTERS, SFR

There are two types of Special Function Registers (SFR).

- BOOT level registers are set at the Integrated Development Environment (IDE);
- Instruction level registers;

17.1 Boot Level Registers

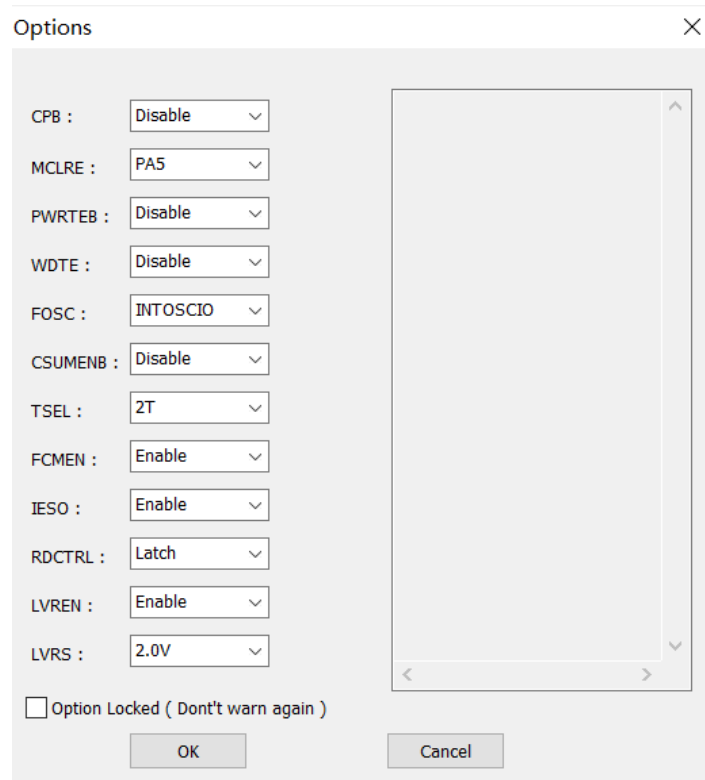


Figure 17-1 Boot Selectables in the IDE

| Name | Functions | default |
|---------|--|----------------|
| CPB | PROM Read Protection | disabled |
| MCLRE | Reset by External I/O | disabled |
| PWRTEB | Power-Up Timer (PWRT) | disabled |
| WDTE | <u>WDT</u> <ul style="list-style-type: none"> Enabled (overrides instructions disable) <u>Instruction controls (SWDTEN)</u> | SWDTEN control |
| FOSC | <ul style="list-style-type: none"> LP: external oscillator across PA7 (+) and PA6 (-) XT: external oscillator across PA7 (+) and PA6 (-) EC: external oscillator at PA7 (+), PA6 as I/O pin INTOSC: PA6 output "Instruction Clock", PA7 as I/O pin <u>INTOSCIO</u>: PA7 and PA6 as I/O pins | INTOSCIO |
| CSUMENB | Checksum | disabled |
| TSEL | <u># of SysClk per Instruction Cycle (2T or 4T)</u> <ul style="list-style-type: none"> 2 (Instruction Clock = SysClk/2) 4 (Instruction Clock = SysClk/4) | 2 |
| FCMEN | <u>Fail-Safe Clock Monitor</u> <ul style="list-style-type: none"> <u>Enabled</u> Disabled | Enabled |
| IESO | <u>Two-speed Startup for XT and LP</u> <ul style="list-style-type: none"> <u>Enabled</u> Disabled | Enabled |
| RDCTRL | <u>READ register when TRISx = 0 (Output enabled)</u> <ul style="list-style-type: none"> Input latch <u>Output latch</u> | Output |
| LVREN | <u>LVR</u> <ul style="list-style-type: none"> Enabled <u>Disabled</u> Enabled except in SLEEP Instruction controlled (SLVREN) | Enabled |
| LVRS | <u>7 V_{BOR} Voltage levels (V): 2.0 / 2.2 / 2.5 / 2.8 / 3.1 / 3.6 / 4.1</u> | 2.0 |

Table 17-1 Boot Level Registers (selected at IDE)

17.2 Instruction Set Registers

Instruction set Special Function Registers (SFR) are stored in four banks. The value of available addressing register is 384 because BANK3 is not use. The corresponding bank must be selected before the registers inside can be accessed.

Any instruction using the INDF register actually accesses data pointed to by the File Select Register{FSR_B8,FSR}. When FSR_B8 is 1 and using indirect addressing accesses SFR, {FSR_B8,FSR} will point the BANK2

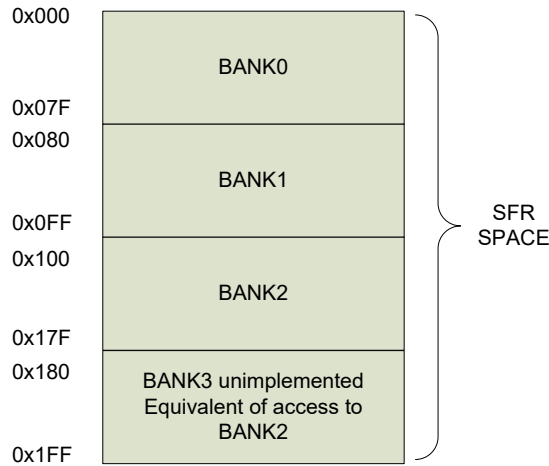


Figure 17-2 Indirect addressing

Since extra instructions are involved in switching BANK, some often-used SFR are stored in all 3 banks to minimize switching. Registers common to all four BANKS are synchronized.

| ADDR | Name | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Reset |
|---|------------------|--|-----------|-------|--|-------|-------|-------|-----------|-----------|
| 0, 80, 100 | INDF | Addressing this location uses contents of FSR to address data memory (not a physical register) | | | | | | | | xxxx xxxx |
| 2, 82, 102 | PCL | Program Counter's (PC) least Significant Byte | | | | | | | | 0000 0000 |
| 3, 83, 103 | STATUS | FSRB8 | PAGE[1:0] | /TF | /PF | Z | HC | C | | 0001 1xxx |
| 4, 84, 104 | FSR | Indirect Data Memory Address Pointer | | | | | | | | xxxx xxxx |
| A, 8A, 10A | PCLATH | - | - | - | Write Buffer for upper 5 bits of Program Counter | | | | | ---0 0000 |
| B, 8B, 10B | INTCON | GIE | PEIE | TOIE | INTE | PAIE | TOIF | INTF | PAIF | 0000 0000 |
| 0x70 – 0x7F 0xF0 – 0xFF 0x170 – 0x17F | COMMON BANK SRAM | | | | | | | | xxxx xxxx | |

Table 17-2 Registers common to all 3 banks

| ADDR | Name | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Reset | |
|-------|---|--|--------------|-----------|--|---------------|---------|--------------|--------|-----------|-----------|
| 0 | INDF | Addressing this location uses contents of FSR to address data memory (not a physical register) | | | | | | | | xxxx xxxx | |
| 1 | TMR0 | Timer0 counter | | | | | | | | xxxx xxxx | |
| 2 | PCL | Program Counter's (PC) least Significant Byte | | | | | | | | 0000 0000 | |
| 3 | STATUS | FSRB8 | PAGE[1:0] | | /TF | /PF | Z | HC | C | 0001 1xxx | |
| 4 | FSR | Indirect Data Memory Address Pointer | | | | | | | | xxxx xxxx | |
| 5 | PORTA | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 | xxxx xxxx | |
| 7 | PORTC | - | - | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 | --xx xxxx | |
| A | PCLATH | - | - | - | Write Buffer for upper 5 bits of Program Counter | | | | | ---0 0000 | |
| B | INTCON | GIE | PEIE | T0IE | INTE | PAIE | T0IF | INTF | PAIF | 0000 0000 | |
| C | PIR1 | EEIF | CKMEAIF | - | C2IF | C1IF | OSFIF | TMR2IF | TMR1IF | 0000 0000 | |
| D | PIR2 | - | - | - | - | - | - | ADIF | CCP1IF | ---- --00 | |
| E | TMR1L | Timer1[7:0] | | | | | | | | xxxx xxxx | |
| F | TMR1H | Timer1[15:8] | | | | | | | | xxxx xxxx | |
| 10 | T1CON | T1GINV | TMR1GE | T1CKPS1 | T1CKPS0 | T1OSCEN | T1SYNC | TMR1CS | TMR1ON | 0000 0000 | |
| 11 | TMR2 | TMR2 [7:0] | | | | | | | | 0000 0000 | |
| 12 | T2CON | - | TOUTPS [3:0] | | | | TMR2ON | T2CKPS [1:0] | | -000 0000 | |
| 13 | CCPR1L | Least significant byte of Capture, Compare, PWM1 Register | | | | | | | | xxxx xxxx | |
| 14 | CCPR1H | Most significant byte of Capture, Compare, PWM1 Register | | | | | | | | xxxx xxxx | |
| 15 | CCP1CON | P1M[1:0] | | DC1B[1:0] | | CCP1M[3:0] | | | | 0000 0000 | |
| 16 | PWM1CON | PRSEN | PDC[6:0] | | | | | | | | 0000 0000 |
| 17 | ECCPAS | ECCPASE | ECCPAS[2:0] | | | PSSAC[1:0] | | PSSBD[1:0] | | 0000 0000 | |
| 18 | WDTCON | - | - | - | WDTPS[3:0] | | | | SWDTEN | ---0 1000 | |
| 19 | CMCON0 | C2OUT | C1OUT | C2INV | C1INV | CIS | CM[2:0] | | | 0000 0000 | |
| 1A | CMCON1 | - | - | - | - | - | - | T1GSS | C2SYNC | ---- --10 | |
| 1B | MSCKCON | - | VREG_OE | T2CKSRC | SLVREN | - | CKMAVG | CKCNT1 | - | 0000 -00- | |
| 1C | SOSCPRL | SOSCPR [7:0] | | | | | | | | 1111 1111 | |
| 1D | SOSCPRH | - | - | - | - | SOSCPR [11:8] | | | | ---- 1111 | |
| 1E | ADRESH | Most Significant 2 bits of the right shifted A/D result or 8bits of left shifted result | | | | | | | | xxxx xxxx | |
| 1F | ADCON0 | ADFM | VCFG1 | VCFG0 | CHS[2:0] | | | GO/DONE | ADON | 0000 0000 | |
| 20-7F | SRAM BANK1 (96Bytes) , Physical address 0x00-0x5F | | | | | | | | | xxxx xxxx | |

Table 17-3 SFR, BANK 0

| ADDR | Name | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Reset | |
|-------|---|--|------------|-------------|--|---------|-------|--------|-----------|-----------|-----------|
| 80 | INDF | Addressing this location uses contents of FSR to address data memory (not a physical register) | | | | | | | | xxxx xxxx | |
| 81 | OPTION | /PAPU | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 | |
| 82 | PCL | Program Counter's (PC) least Significant Byte | | | | | | | | 0000 0000 | |
| 83 | STATUS | FSRB8 | PAGE[1:0] | | /TF | /PF | Z | HC | C | 0001 1xxx | |
| 84 | FSR | Indirect Data Memory Address Pointer | | | | | | | | xxxx xxxx | |
| 85 | TRISA | TRISA [7:0] | | | | | | | | 1111 1111 | |
| 87 | TRISC | - | - | TRISC [5:0] | | | | | - | --11 1111 | |
| 88 | WPUC | - | - | WPUC [5:0] | | | | | - | --00 0000 | |
| 89 | WPD | - | - | - | WPDA4 | WPDC1 | WPDC2 | WPDC3 | - | ---0 000- | |
| 8A | PCLATH | - | - | - | Write Buffer for upper 5 bits of Program Counter | | | | | - | ---0 0000 |
| 8B | INTCON | GIE | PEIE | T0IE | INTE | PAIE | T0IF | INTF | PAIF | 0000 0000 | |
| 8C | PIE1 | EEIE | CKMEAIE | - | C2IE | C1IE | OSFIE | TMR2IE | TMR1IE | 0000 0000 | |
| 8D | PIE2 | - | - | - | - | - | - | ADIE | CCP1IE | ---- --00 | |
| 8E | PCON | VREF_OE | LVDL [2:0] | | | LVDEN | LVDW | /POR | /BOR | 0000 0xqq | |
| 8F | OSCCON | LFMOD | IRCF[2:0] | | | OSTS | HTS | LTS | SCS | 0101 x000 | |
| 90 | PWM1AUX | AUX1EN | P1OS | P1FOE | P1EOE | P1DOE | P1COE | P1BOE | P1AOE | 0000 0000 | |
| 91 | ANSEL | ANSEL[7:0] | | | | | | | | 1111 1111 | |
| 92 | PR2 | PR2[7:0], Timer2 period register | | | | | | | | 1111 1111 | |
| 95 | WPUA | WPUA [7:0] | | | | | | | | 1111 1111 | |
| 96 | IOCA | IOCA [7:0] | | | | | | | | 0000 0000 | |
| 99 | VRCON | VREN | - | VRR | - | VR[3:0] | | | 0-0- 0000 | | |
| 9A | EEDAT | EEDAT [7:0] | | | | | | | | 0000 0000 | |
| 9B | EEADR | EEADR [7:0] | | | | | | | | 0000 0000 | |
| 9C | EECON1 | - | - | WREN3 | WREN2 | WRERR | WREN1 | - | RD | --00 x0-0 | |
| 9D | EECON2 | - | - | - | - | - | - | - | WR | ---- --0 | |
| 9E | ADRESL | Least Significant 2 bits of the left shifted A/D result or 8bits of right shifted result | | | | | | | | xxxx xxxx | |
| 9F | ADCON1 | DIVS | ADCS[2:0] | | | - | - | - | - | 0000 ---- | |
| A0-BF | SRAM BANK1 (32Bytes) , Physical address 0x00-0x1F | | | | | | | | | xxxx xxxx | |
| C0-EF | - | | | | | | | | | ---- ---- | |
| F0-FF | SRAM , address BANK0's 0x70-0x7F | | | | | | | | | xxxx xxxx | |

Table 17-4 SFR, BANK 1

| ADDR | Name | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Reset | |
|-----------|---------|--|------------|-------------|--|---|--------|--------|--------|-----------|-----------|
| 100 | INDF | Addressing this location uses contents of FSR to address data memory (not a physical register) | | | | | | | | xxxx xxxx | |
| 102 | PCL | Program Counter's (PC) least Significant Byte | | | | | | | | 0000 0000 | |
| 103 | STATUS | FSRB8 | PAGE[1:0] | /TF | /PF | Z | HC | C | | 0001 1xxx | |
| 104 | FSR | Indirect Data Memory Address Pointer | | | | | | | | xxxx xxxx | |
| 108 | VCON1 | - | VREGM[1:0] | VREGHB[4:0] | | | | | | -000 0000 | |
| 109 | VCON2 | - | - | - | VREGLB[4:0] | | | | | | ---0 0000 |
| 10A | PCLATH | - | - | - | Write Buffer for upper 5 bits of Program Counter | | | | | | ---0 0000 |
| 10B | INTCON | GIE | PEIE | T0IE | INTE | PAIE | T0IF | INTF | PAIF | 0000 0000 | |
| 10C | TMR3L | TMR3 [7:0], Least significant byte of TMR3 | | | | | | | | xxxx xxxx | |
| 10D | TMR3H | TMR3 [11:8], Most Significant 4 bits of TMR3 | | | | PR3[11:8] Most Significant 4 bits of Timer3 Period Register | | | | xxxx 1111 | |
| 10E | PR3L | PR3[7:0] Least significant byte of Timer3 Period Register | | | | | | | | 1111 1111 | |
| 10F | PWM3CR0 | P3INTS | P3PER[2:0] | | | P3CKSRC[2:0] | | | P3BZR | 0000 0000 | |
| 110 | PWM3CR1 | P3EN | P3POL | TMR3PS[2:0] | | | TMR3ON | TMR3IE | TMR3IF | 0000 0000 | |
| 111 | T3CKDIV | Timer3 Clock Divider Register | | | | | | | | 0000 0000 | |
| 112 | TMR4L | TMR4 [7:0], Least significant byte of TMR4 | | | | | | | | xxxx xxxx | |
| 113 | TMR4H | TMR4 [11:8], Most Significant 4 bits of TMR4 | | | | PR4[11:8] Most Significant 4 bits of Timer4 Period Register | | | | xxxx 1111 | |
| 114 | PR4L | PR4[7:0] Least significant byte of Timer4 Period Register | | | | | | | | 1111 1111 | |
| 115 | PWM4CR0 | P4INTS | P4PER[2:0] | | | P4CKSRC[2:0] | | | P4BZR | 0000 0000 | |
| 116 | PWM4CR1 | P4EN | P4POL | TMR4PS[2:0] | | | TMR4ON | TMR4IE | TMR4IF | 0000 0000 | |
| 117 | T4CKDIV | Timer 4 Clock Divider Register | | | | | | | | 0000 0000 | |
| 118 | TMR5L | TMR5 [7:0], Least significant byte of TMR5 | | | | | | | | xxxx xxxx | |
| 119 | TMR5H | TMR5 [11:8], Most Significant 4 bits of TMR5 | | | | PR5[11:8] Most Significant 4 bits of Timer5 Period Register | | | | xxxx 1111 | |
| 11A | PR5L | PR5[7:0] Least significant byte of Timer5 Period Register | | | | | | | | | |
| 11B | PWM5CR0 | P5INTS | P5PER[2:0] | | | P5CKSRC[2:0] | | | P5BZR | 0000 0000 | |
| 11C | PWM5CR1 | P5EN | P5POL | TMR5PS[2:0] | | | TMR5ON | TMR5IE | TMR5IF | 0000 0000 | |
| 11D | T5CKDIV | Timer 5 Clock Divider Register | | | | | | | | 0000 0000 | |
| 120 - 16F | | - | | | | | | | | ----- | |
| 170 - 17F | | SRAM , address BANK0's 0x70-0x7F | | | | | | | | xxxx xxxx | |

Table 17-5 SFR, BANK 2

Notes:

1. INDF is not a physical register;
2. Gray parts indicate not used;
3. Do not write the unused register bits;
4. ANSEL reset value os 0xFF, associated IO pin is analog pin, thus the return value of PORTA[3:0] and PORTC[2:0] are 0 when reading PORTA or PORTC after any reset, because they are analog pins at this time, which has noting to do with their data register.

17.3 STATUS Register

| Name | Status | Register | Addr. | Reset |
|-------|--|-------------|-----------------------|-------|
| FSRB8 | A 9-bit register comprises of the FSRB8 and FSR register. Refer to the Section 17.4 . | STATUS[7] | 0x03 0x83 0x103 | RW-0 |
| PAGE | <u>Register Bank Select</u> 00 = Bank 0 (0x00h – 0x7Fh) 01 = Bank 1 (0x80h – 0xFFh) 1x = Bank 2 (0x100 – 0x17F) | STATUS[6:5] | | RW-00 |
| /TF | <u>Time-out?</u> 1 = CLRWDT or SLEEP instruction after Power-up 0 = WDT time-out occurred | STATUS[4] | | RO-1 |
| /PF | <u>Power-down?</u> 1 = After power-up or by the CLRWDT instruction 0 = By execution of the SLEEP instruction | STATUS[3] | | RO-1 |
| Z | <u>Zero: Result of an arithmetic or logic operation is zero?</u> 1 = Yes 0 = No | STATUS[2] | | RW-x |
| HC | <u>Half Carry: Digit Carry-Over or Borrow from the 4th low-order bit of the result?</u> 1 = Carry-Over, Yes; Borrow, No 0 = Carry-Over, No; Borrow, Yes | STATUS[1] | | RW-x |
| C | <u>Carry: Digit Carry-Over or Borrow from MSB of the result?</u> 1 = Carry-Over, Yes; Borrow, No 0 = Carry-Over, No; Borrow, Yes | STATUS[0] | | RW-x |

Table 17-6 Status Register

Notes:

1. The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, HC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.
2. It is recommended, therefore, that only BCR, BSR, SWAPR and STR instructions are used to alter the STATUS register.

17.4 PCL and PCLATH

The program array have one Page (2kW). At the end of Page (0x7FF) it will roll over to the beginning of Page (0x000). The address width of a command is only 11 bits, and can address 2kW only. For LJUMP and LCALL, there is no need to set PCLATH.

The Program Counter (PC) is 11 bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high 3 bits PC[10:8] is not directly readable or writable and comes from PCLATH. On any Reset, PC clears. **Figure 17-3** shows the two situations for the loading of the PC.

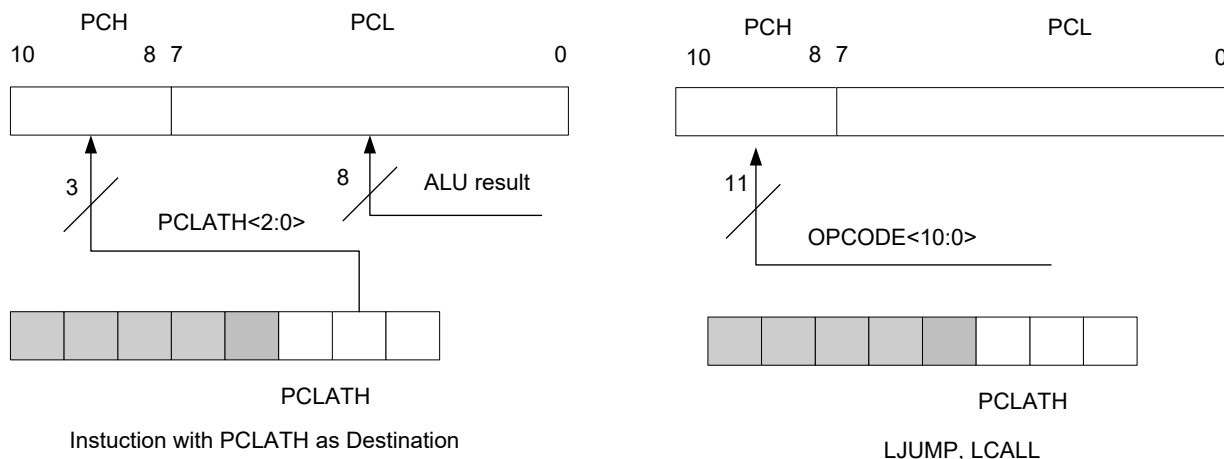


Figure 17-3 Loading of PC in different situations

Executing any instruction with the PCL register as the destination simultaneously causes the Program Counter PC[10:8] bits to be replaced by the contents of the PCLATH register. This allows the entire contents of the program counter to be changed by first writing the desired upper 3 bits to the PCLATH register

A computed JUMP is accomplished by adding an offset to the program counter (ADDWR PCL). Care should be exercised when jumping into a look-up table or program branch table (computed JUMP) by modifying the PCL register. Assuming that PCLATH is set to the table start address, if the table length is greater than 255 instructions or if the lower 8 bits of the memory address rolls over from 0xFF to 0x00 in the middle of the table, then PCLATH must be incremented for each address rollover that occurs between the table beginning and the target location within the table .

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

Any instruction using the INDF register actually accesses data pointed to by the File Select Register (FSRB8, FSR). Reading INDF itself indirectly will produce 0x000. Writing to the INDF register indirectly results in a no operation (although Status bits may be affected).

18. ELECTRICAL SPECIFICATIONS

18.1 Absolute Maximum Ratings

| | |
|------------------------------------|---|
| Operation temperature Grade 3..... | -40 – + 85°C |
| Operation temperature Grade 2..... | -40 – +105°C |
| Operation temperature Grade 1..... | -40 – +125°C |
| Storage temperature..... | -40 – +125°C |
| Power supply voltage..... | V _{SS} -0.3V – V _{SS} +6.0V |
| PAD input voltage..... | V _{SS} -0.3V – V _{DD} +0.3V |

Notes:

1. Stresses above “Absolute Maximum Ratings” may cause permanent damages to the device.
2. All characterizations are at 25°C, V_{DD} =2.0 – 5.5V unless otherwise stated.
3. Values and ranges indicated are from characterizations, and are not indicative of the final shipping criteria. Production test are at 25°C unless otherwise stated. Performance at temperature outside of above operation temperature are not guaranteed as high temperature screening is not part of normal production procedure.
4. Typical unstressed memory data retention @ 150°C > 10 years.

18.2 Operation Characteristics

| Parameters | | Min | Typical | Max | Units | Conditions |
|--|--------|---------------------------------------|---------|-----|-------|--|
| Fsys (SysClk) | 2T/4T | - | - | 8 | MHz | -40 – 85°C, V _{DD} = 2.0 – 5.5V |
| | | - | - | 16 | MHz | -40 – 85°C, V _{DD} = 2.7 – 5.5V |
| Instruction Period (T _{INSTRCLK}) | 2T | - | 125 | - | ns | SysClk = HIRC |
| | 4T | - | 250 | - | ns | |
| | 2T | - | 61 | - | µs | SysClk = LIRC |
| | 4T | - | 122 | - | µs | |
| T _{OCKI} High or Low Pulse Width | | 0.5 * T _{TOCK} + 20 | - | - | ns | no Prescaler |
| | | 10 | - | - | ns | with Prescaler |
| T _{OCKI} Input Period | | Max. 20 and (T _{TOCK} +40)/N | - | - | ns | N = 1, 2, 4, ..., 256 (with Prescaler) N = 1 (no Prescaler) |
| T _{OCKI} High or Low Pulse Width | Sync. | (T _{sysclk} + 20) / N | - | - | ns | N = 1, 2, 4, 8 (with Prescaler) |
| | Async. | Max(10 or 30 / N) | - | - | ns | |
| T _{OCKI} Input Period | Sync. | 2 * (T _{sysclk} + 20) / N | - | - | ns | |
| | Async. | Max(20 or 60 / N) | - | - | ns | |
| Power-On-Reset hold time (T _{DRH}) | | - | 4.2 | - | ms | 25°C, PWRT disable |
| Ext. Reset pulse width (T _{MCLRB}) | | 2000 | - | - | ns | 25°C |
| WDT period (T _{WDT}) | | - | 1 | - | ms | Prescaler = 1:1 |

Note: T_{TOCK} is the period dictated by T_{0CS}.

18.3 POR, LVR, LVD

Power-On-Reset (POR)

| Parameters | Min | Typical | Max | Units | Conditions |
|------------------------------------|-----|---------|-----|-------|------------------------------|
| I _{POR} Operating Current | – | 0.14 | – | μA | 25°C, V _{DD} = 3.3V |
| V _{POR} | – | 1.65 | – | V | 25°C |

Low Voltage Reset (LVR)

| Parameters | Min | Typical | Max | Units | Conditions |
|------------------------------------|------|---------|------|-------|------------------------------------|
| I _{LVR} Operating Current | – | 19.8 | – | μA | 25°C, V _{DD} = 3.3V |
| V _{LVR} , LVR threshold | 1.92 | 2.0 | 2.08 | V | 25°C |
| | 2.11 | 2.2 | 2.29 | | |
| | 2.40 | 2.5 | 2.60 | | |
| | 2.69 | 2.8 | 2.91 | | |
| | 2.98 | 3.1 | 3.22 | | |
| | 3.46 | 3.6 | 3.74 | | |
| LVR delay | – | 125 | 157 | μs | 25°C, V _{DD} = 2.0 – 5.5V |

Low Voltage Detect (LVD)

| Parameters | Min | Typical | Max | Units | Conditions |
|------------------------------------|------|---------|------|-------|------------------------------------|
| I _{LVD} Operating Current | – | 26.1 | – | μA | 25°C, V _{DD} = 3.3V |
| V _{LVD} , LVD threshold | 1.92 | 2.0 | 2.08 | V | 25°C |
| | 2.30 | 2.4 | 2.50 | | |
| | 2.69 | 2.8 | 2.91 | | |
| | 2.88 | 3.0 | 3.12 | | |
| | 3.46 | 3.6 | 3.74 | | |
| | 3.84 | 4.0 | 4.16 | | |
| LVD delay | – | 125 | 157 | μs | 25°C, V _{DD} = 2.0 – 5.5V |

18.4 I/O PORTS

| Parameters | Min | Typical | Max | Units | Conditions |
|-------------------------|--------------------|---------|--------------------|------------|---|
| V_{IL} | 0 | - | $0.3 \cdot V_{DD}$ | V | |
| V_{IH} | $0.7 \cdot V_{DD}$ | - | V_{DD} | V | |
| Leakage current | -1 | - | 1 | μA | $V_{DD} = 5V$ |
| Source current (Source) | - | -22 | - | mA | $25^{\circ}C, V_{DD} = 5.0V, V_{OH} = 4.5V$ |
| Sink Current (Sink) | - | 19 | - | mA | $25^{\circ}C, V_{DD} = 5.0V, V_{OL} = 0.5V$ |
| Pull-up resistance | - | 45 | - | k Ω | $25^{\circ}C, V_{DD} = 3.3V$ |
| | - | 28 | - | | $25^{\circ}C, V_{DD} = 5.0V$ |
| Pull-down resistance | - | 189 | - | k Ω | $25^{\circ}C, V_{DD} = 3.3V$ |
| | - | 97 | - | | $25^{\circ}C, V_{DD} = 5.0V$ |

18.5 Operation Current (I_{DD})

| Parameters | SysClk | Typical @ V_{DD} | | | Units |
|---|---------|--------------------|--------|--------|---------|
| | | 2.0V | 3.3V | 5.5V | |
| Normal mode (2T) - I_{DD} | 16MHz | — | 1.528 | 1.681 | mA |
| | 8 MHz | 0.694 | 1.196 | 1.291 | |
| | 4 MHz | 0.520 | 0.716 | 0.768 | |
| | 2 MHz | 0.327 | 0.447 | 0.469 | |
| | 1 MHz | 0.229 | 0.313 | 0.331 | |
| | 500 kHz | 0.187 | 0.262 | 0.268 | |
| | 250 kHz | 0.162 | 0.227 | 0.232 | |
| | 32 kHz | 0.036 | 0.071 | 0.083 | |
| Sleep Mode (WDT OFF, LVR OFF), I_{SB} | - | 0.464 | 0.728 | 0.878 | μA |
| Sleep Mode (WDT ON, LVR OFF) | 32 kHz | 1.468 | 2.937 | 3.215 | |
| Sleep Mode (WDT OFF, LVR ON) | - | 13.714 | 19.791 | 25.444 | |
| Sleep Mode (WDT ON, LVR ON) | 32 kHz | 14.529 | 22.070 | 27.816 | |
| Sleep Mode (WDT OFF, LVR OFF, LVD ON) | - | 22.032 | 26.193 | 30.792 | |

Note: Sleep mode I_{SB} is measured with all I/O in Pull-down input mode.

18.6 Internal Oscillators

Internal Low Frequency Oscillator (LIRC)

LIRC is set at 32 kHz during measurement (LFMOD=0).

| Parameters | Min | Typical | Max | Units | Conditions |
|-------------------------------------|-------|---------|------|-------|------------------------------------|
| Range | 30.4 | 32 | 33.6 | kHz | 25°C, V _{DD} = 2.5V |
| temperature dependence | -2.0% | - | 2.0% | - | -40 – 85°C, V _{DD} = 2.5V |
| supply voltage variation | -4.0% | - | 1.0% | - | 25°C, V _{DD} = 2.0 – 5.5V |
| I _{LIRC} Operating Current | - | 1.1 | - | µA | 25°C, V _{DD} = 3.0V |
| Start up Time | - | 4.6 | - | µs | 25°C, V _{DD} = 3.0V |

Internal High Frequency Oscillator (HIRC)

| Parameters | Min | Typical | Max | Units | Conditions |
|-------------------------------------|-------|---------|-------|-------|------------------------------------|
| Range | 15.84 | 16 | 16.16 | MHz | 25°C, V _{DD} = 2.5V |
| temperature dependence | -3.0% | - | 2.5% | - | -40 – 85°C, V _{DD} = 2.5V |
| supply voltage variation | -1.0% | - | 1.0% | - | 25°C, V _{DD} = 2.0 – 5.5V |
| I _{LIRC} Operating Current | - | 30 | - | µA | 25°C, V _{DD} = 3.0V |
| Start up Time | - | 2.5 | - | µs | 25°C, V _{DD} = 3.0V |

18.7 ADC (10 bit) and ADC VREF

ADC (10 bit)

| Parameters | Min | Typical | Max | Units | Conditions |
|--|-----------------|---------|------------------|-------|---|
| ADC operating V _{DD} | 2.7 | - | 5.5 | V | |
| ADC operating current I _{VDD} | - | 90 | - | µA | V _{REF} = V _{DD} = 5.5V |
| Analog input V _{AIN} | V _{SS} | - | V _{REF} | V | |
| External V _{REF} | 2.0 | - | V _{DD} | V | |
| Resolution | - | - | 10 | bit | |
| Integral error E _{IL} | - | ± 1.0 | - | LSB | V _{REF} = V _{DD} = 5.0V |
| Differential error E _{DL} | - | ± 0.5 | - | LSB | F _{ADCCLK} = 250KHZ |
| Offset error E _{OFF} | - | ± 5.0 | - | LSB | V _{REF} = V _{DD} = 5.0V |
| Gain error E _{GN} | - | ± 2.0 | - | LSB | F _{ADCCLK} = 250KHZ |
| Conversion clock period TAD | - | 2 | - | µs | V _{REF} > 3.0V, V _{DD} > 3.0V |
| Conversion clock amount | - | 14.5 | - | TAD | |
| Start-Up Time (T _{ST}) | - | 15 | - | µs | |
| Acquisition Time (T _{ACQ}) | - | ≥ 2 | - | µs | |
| Conversion clock period TAD | - | - | 10 | kΩ | (recommended) |

DNL Error

| typical DNL Error (LSB) @ $V_{DD} = 5\text{ V}$ | | | |
|---|-----------|-----------|-----------|
| V_{REF+} F_{ADCLK} | 2 | 3 | V_{DD} |
| $\leq 1\text{ MHz}$ | ± 0.5 | ± 0.5 | ± 0.5 |
| 2 MHz | ± 0.5 | ± 0.5 | ± 0.5 |
| 4 MHz | ± 2.0 | ± 1.5 | ± 1.0 |

INL Error

| typical INL Error (LSB) @ $V_{DD} = 5\text{ V}$ | | | |
|---|-----------|-----------|-----------|
| V_{REF+} F_{ADCLK} | 2 | 3 | V_{DD} |
| $\leq 1\text{ MHz}$ | ± 0.5 | ± 0.5 | ± 1.0 |
| 2 MHz | ± 1.0 | ± 1.0 | ± 1.0 |
| 4 MHz | ± 2.5 | ± 2.0 | ± 2.0 |

Internal ADC V_{REF}

| Parameters | | Min | Typical | Max | Units | Conditions |
|------------------------------|-----------------------------|-------|---------|-------|---------------|---|
| Internal $V_{ADC-REF}$ | $V_{ADC-REF} = 2.0\text{V}$ | 1.990 | 2 | 2.010 | V | 25°C , $V_{DD} = 5.0\text{V}$ |
| | $V_{ADC-REF} = 3.0\text{V}$ | 2.985 | 3 | 3.015 | V | 25°C , $V_{DD} = 5.0\text{V}$ |
| Supply voltage variation | $V_{ADC-REF} = 2.0\text{V}$ | -0.5% | - | 0.5% | V | 25°C , $V_{DD} = 2.7\sim 5.5\text{V}$ |
| | $V_{ADC-REF} = 3.0\text{V}$ | -0.5% | - | 0.5% | V | 25°C , $V_{DD} = 3.5\sim 5.5\text{V}$ |
| Temperature dependence | $V_{ADC-REF} = 2.0\text{V}$ | -2.0% | - | 2.0% | - | $-40 - 85^\circ\text{C}$, $V_{DD} = 5.0\text{V}$ |
| | $V_{ADC-REF} = 3.0\text{V}$ | -2.0% | - | 2.0% | - | $-40 - 85^\circ\text{C}$, $V_{DD} = 5.0\text{V}$ |
| Settling time T_{VRINT} | $V_{ADC-REF} = 2.0\text{V}$ | - | 450 | - | μs | |
| | $V_{ADC-REF} = 3.0\text{V}$ | - | 450 | - | μs | |

18.8 Comparator

| Parameters | Min | Typical | Max | Units | Conditions |
|-------------------------------|-----|---------|----------------------|-------|------------------------------------|
| Operation current Ivdd | — | 70 | — | uA | 3V, 25°C |
| Operating voltage | 2.0 | — | 5.5 | V | |
| Input common mode voltage | 0 | — | V _{DD} -1.5 | V | 2.0V~5.5V, -40°C~85°C |
| Offset | — | ±5 | ±10 | mV | 2.0V~5.5V, -40°C~85°C |
| CMRR | 55 | — | — | dB | 2.0V~5.5V, -40°C~85°C |
| Hysteresis | — | 0 | — | mV | 2.0V~5.5V, -40°C~85°C |
| Response Time | — | 200 | — | ns | Normal Mode: Output Low -> High |
| | — | 150 | — | ns | Normal Mode: Output High -> Low |
| Reference voltage stable time | | 10 | | us | |

18.9 4bit DAC (Reference voltage configuration)

| Parameters | Min | Typical | Max | Units | Conditions |
|-------------------|-----|---------------------|-------|-------|-----------------------|
| Relative Accuracy | — | V _{DD} /16 | — | V | 2.0V~5.5V, -40°C~85°C |
| Absolute Accuracy | — | — | ± 1/2 | LSB | 2.0V~5.5V, -40°C~85°C |
| Unit resistor | — | 5000 | — | Ω | 2.0V~5.5V, -40°C~85°C |
| Settle Time | — | — | 10 | us | 0000 -> 1111 |

18.10 Voltage Regulator Output Circuit

| Parameters | Min | Typical | Max | Units | Conditions |
|----------------|-----|---------|-----|-------|---|
| Ivdd | — | 70.68 | — | uA | 25°C, V _{DD} = 3.3V |
| Output voltage | — | 2.4 | — | V | VREGM = 00, 25°C, V _{DD} = 3.3~5.5V |
| | — | 3.6 | — | V | VREGM = 01, 25°C, V _{DD} = 3.8~5.5V |
| | — | 4.8 | — | V | VREGM = 10, 25°C, V _{DD} = 5.0~5.5V |
| | — | 5.24 | — | V | VREGM = 11, 25°C, V _{DD} = 5.5V |
| Output Current | — | 200 | — | uA | 25°C, V _{DD} = 3.3~5.5V |

18.11 Program and Data EEPROM

| Parameters | | Min | Typical | Max | Units | Conditions |
|-----------------------|-------------------------------|------------------|---------|-----|-------|--|
| V _{DD-READ} | Program/Data EE read voltage | V _{POR} | - | 5.5 | V | -40 – 85°C |
| V _{DD-WRITE} | Program EE write voltage | 2.7 | - | 5.5 | V | -40 – 85°C |
| | Data EE write voltage | 2.0 | - | 5.5 | | |
| N _{END} | Program EE erase/write cycles | 100 k | - | - | cycle | 25°C |
| | | 40 k | - | - | | 85°C |
| | Data EE erase/write cycles | 1,000 k | - | - | | 25 °C |
| | | 400 k | - | - | | 85 °C |
| T _{RET} | Program EE data retention | 20 | - | - | year | after 1k cycles @ 85 °C |
| | Data EE data retention | 20 | - | - | | after 10k cycles @ 85 °C |
| T _{WRITE} | Data EE write time | - | 4.0 | - | ms | Auto-Erase enabled |
| I _{PROG} | Data EE programming current | - | 500 | - | µA | 25 °C, V _{DD} = 3.3 V, 16MHz / 2T |

18.12 EMC characteristics
ESD

| Parameters | | Min | Typical | Max | Units | Conditions |
|------------------|-----|------|---------|-----|-------|----------------------------|
| V _{ESD} | HBM | 4000 | - | - | V | MIL-STD-883H Method 3015.8 |
| V _{ESD} | MM | 200 | - | - | V | JESD22-A115 |

Latch-up

| Parameters | | Min | Typical | Max | Units | Conditions |
|---------------------|--|-----|---------|-----|-------|-------------|
| LU, static latch-up | | 200 | - | - | mA | EIA/JESD 78 |

EFT

| Parameters | | Min | Typical | Max | Units | Conditions |
|------------------|--|-----|---------|-----|-------|---|
| V _{EFT} | | 5.5 | - | - | kV | 1µF Cap applied on V _{DD} (5V) |

19. Characterization Graphs

Note: The characterization graphs are for reference only, not guaranteed by production test.

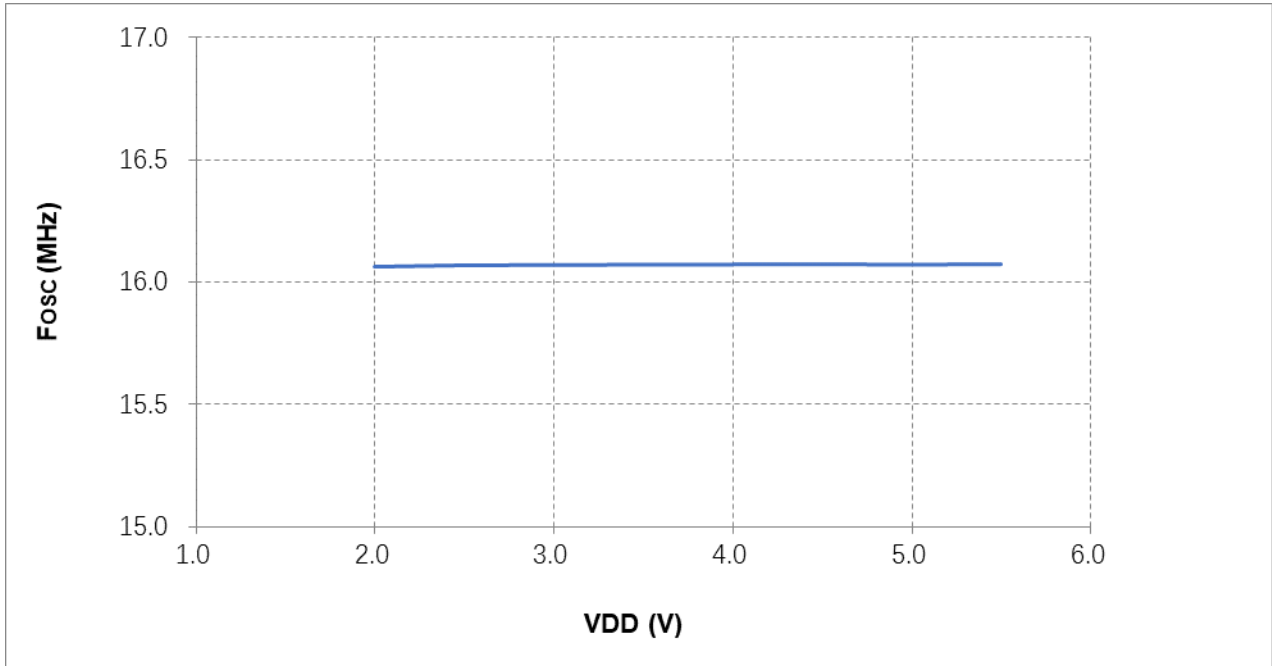


Figure 19-1 HIRC vs. V_{DD} ($T_A = 25^\circ\text{C}$)

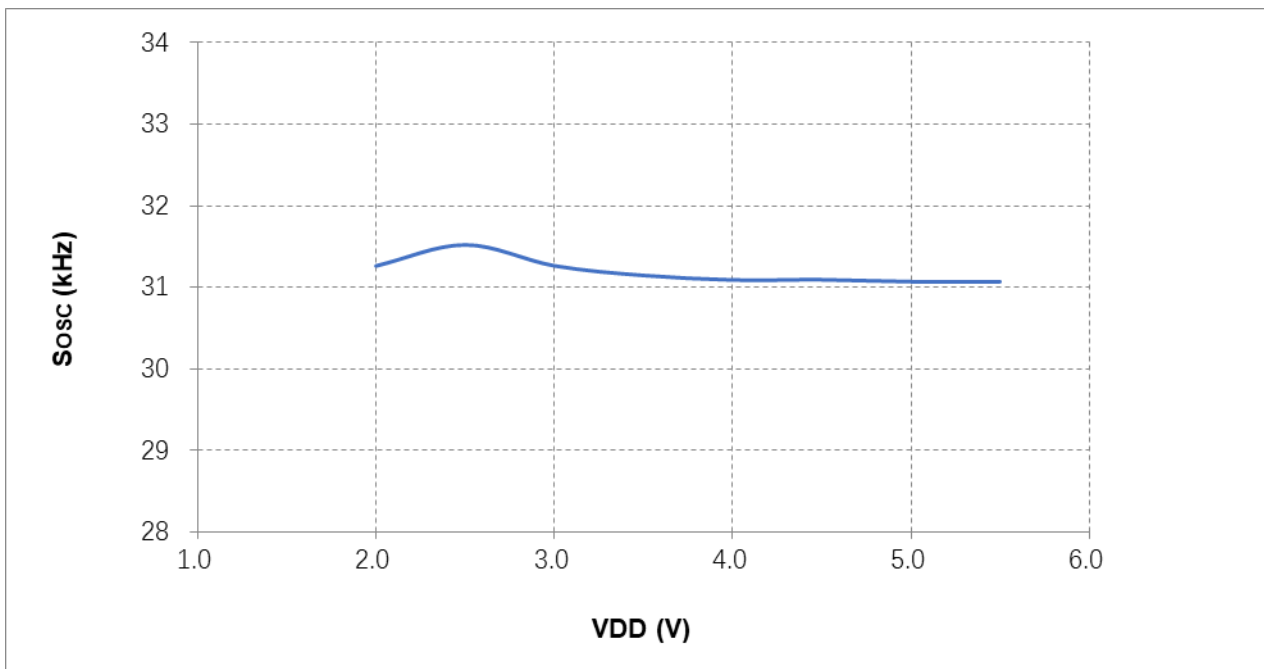


Figure 19-2 LIRC vs. V_{DD} ($T_A = 25^\circ\text{C}$)

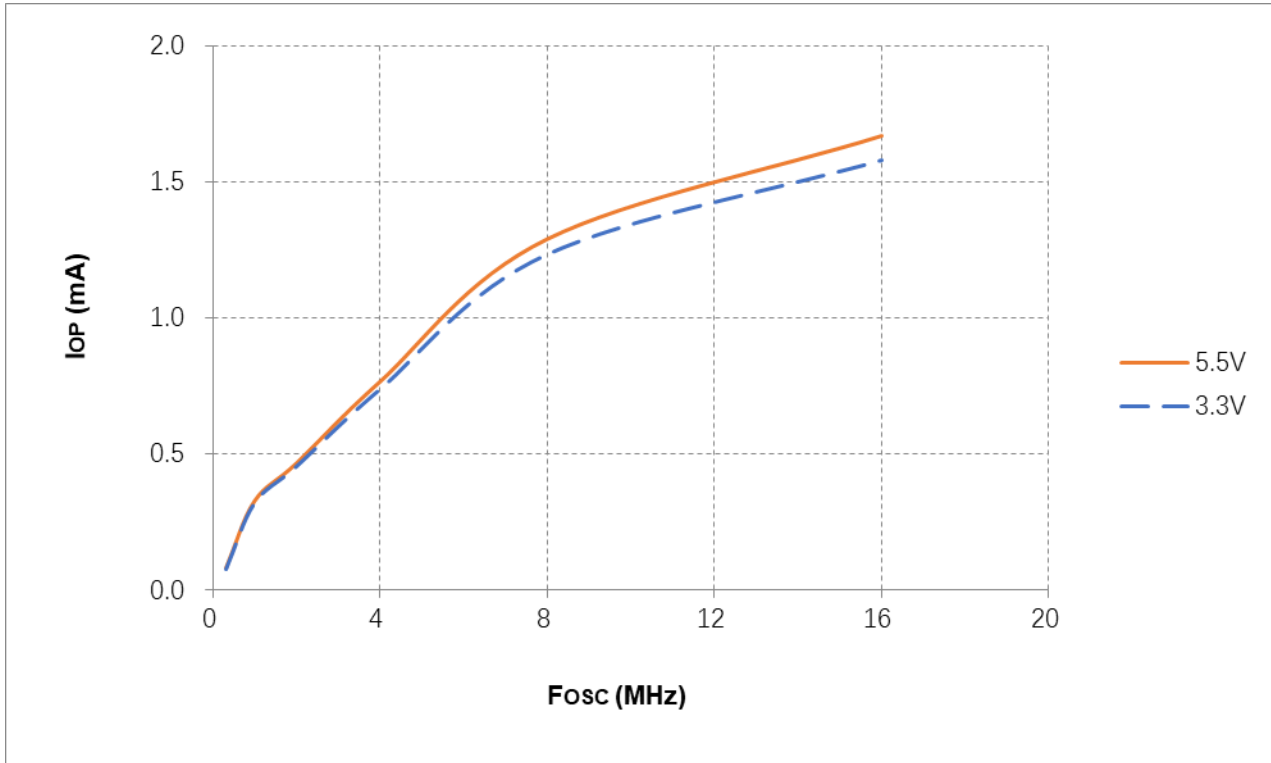


Figure 19-3 I_{DD} vs. Frequency (2T, $T_A = 25^\circ\text{C}$)

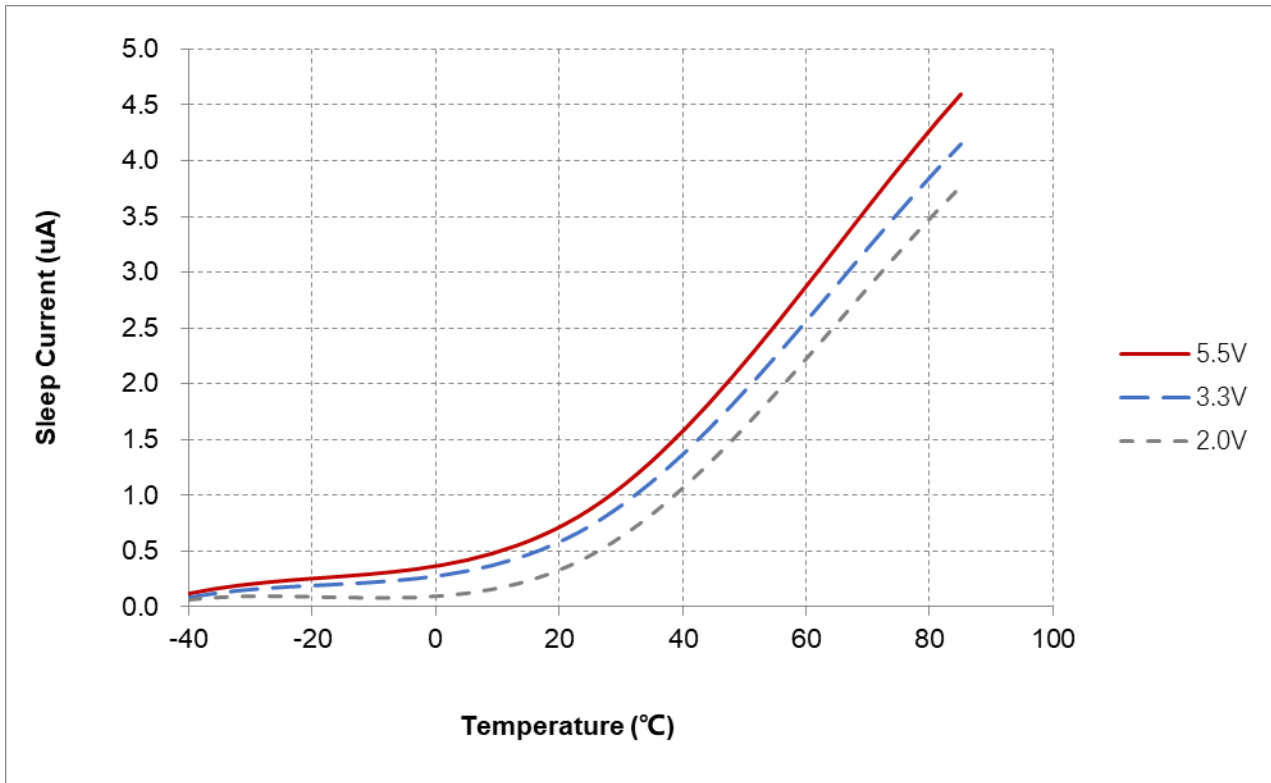


Figure 19-4 Sleep Current (I_{SB}) vs. Temperature

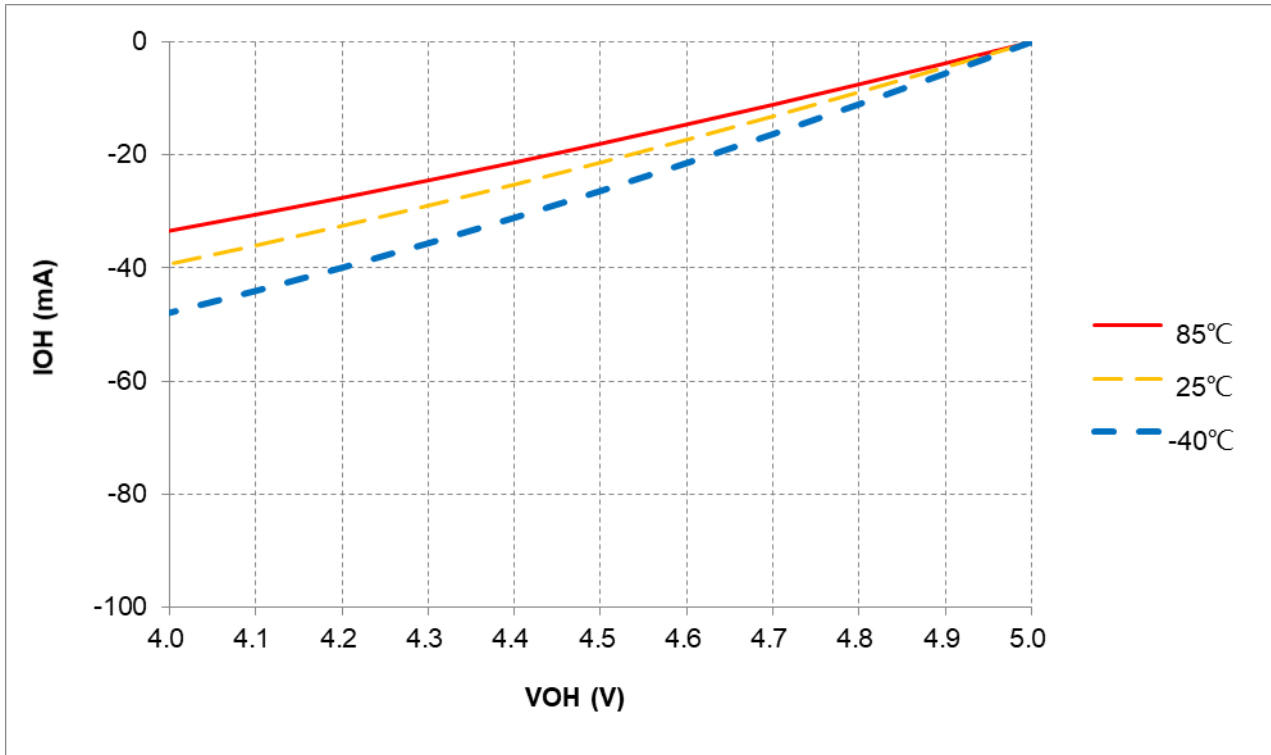


Figure 19-5 IOH vs. VDD, VOH @L = -22mA

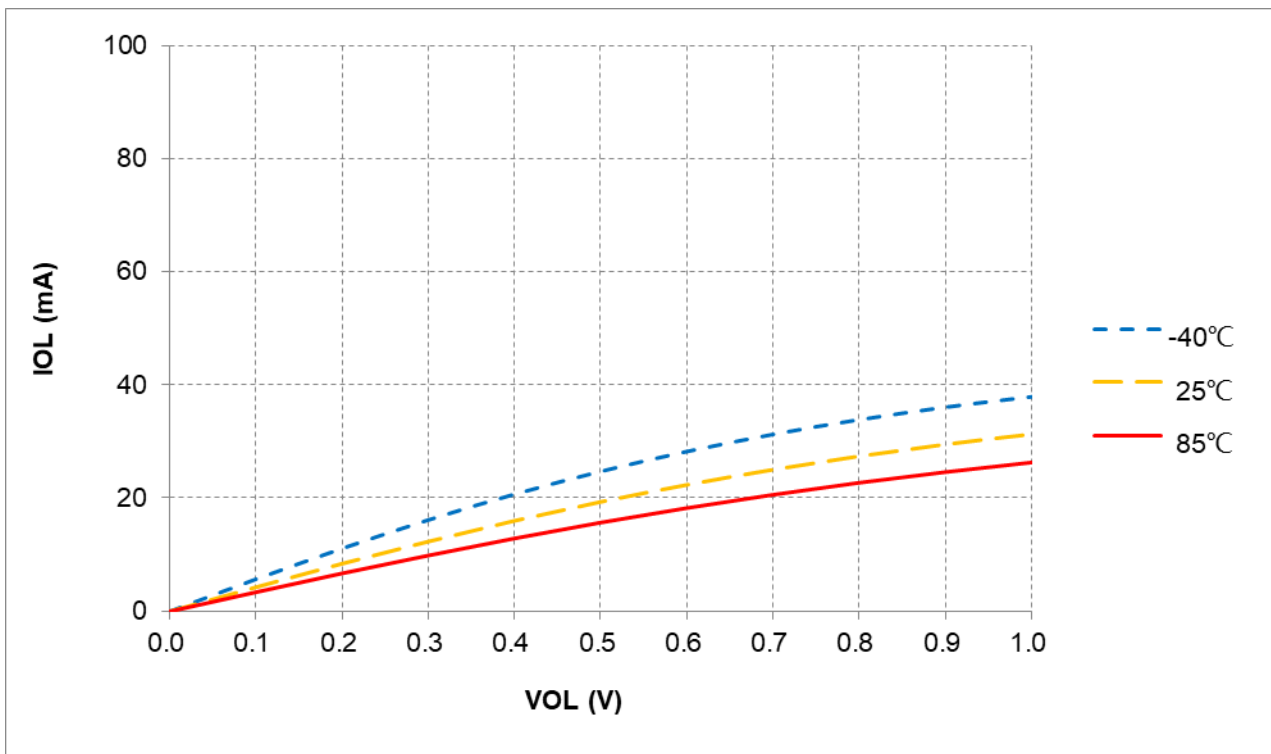
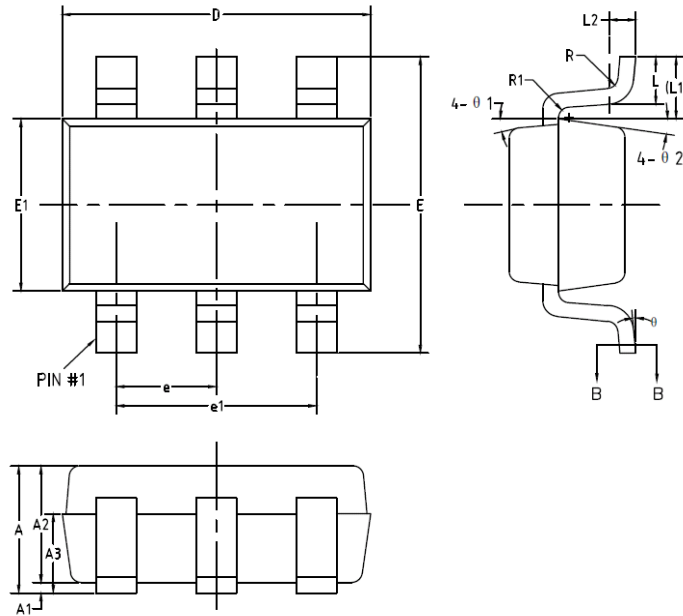


Figure 19-6 IOL vs. VDD, VOL @L = 19mA

20. PACKAGING INFORMATION

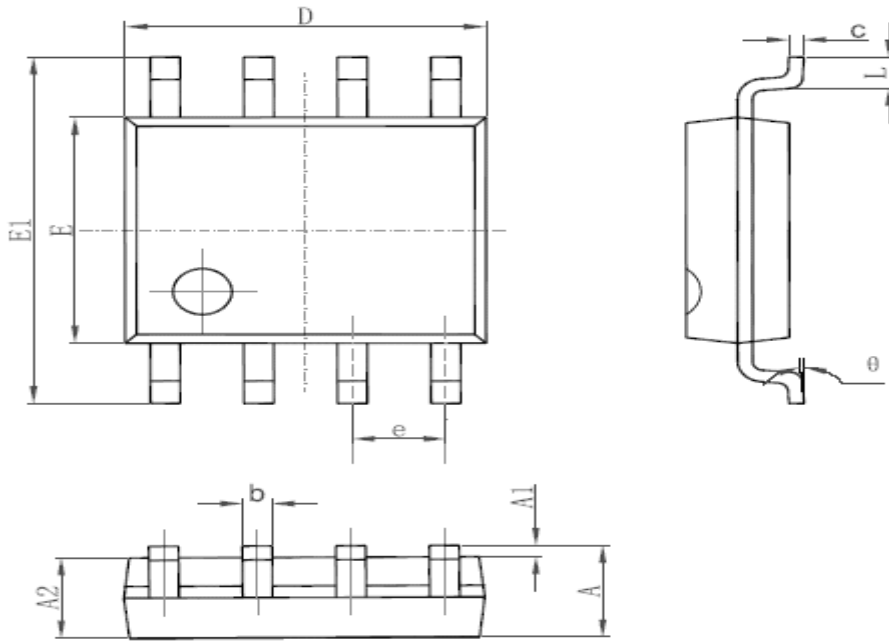
The device is available in SOT23-6, SOP8, MSOP10, SOP14 and SOP16 packages. The specific package size information is shown below:

SOT23-6



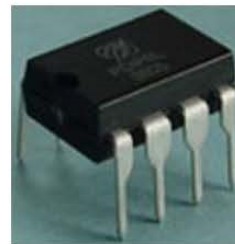
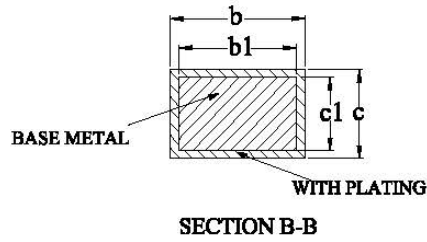
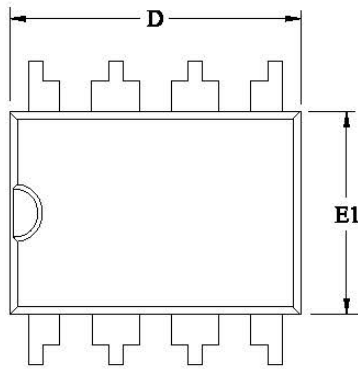
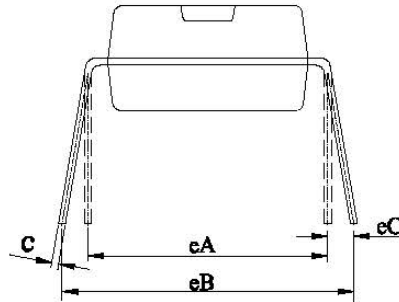
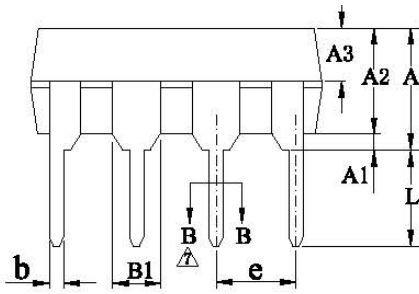
| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|-----------|---------------------------|------|----------------------|-------|
| | Min | Max | Min | Max |
| A | - | 1.45 | - | 0.057 |
| A1 | 0 | 0.15 | 0 | 0.006 |
| A2 | 0.90 | 1.30 | 0.035 | 0.051 |
| A3 | 0.60 | 0.70 | 0.024 | 0.028 |
| b | 0.39 | 0.49 | 0.015 | 0.019 |
| b1 | 0.35 | 0.45 | 0.014 | 0.018 |
| c | 0.08 | 0.22 | 0.003 | 0.009 |
| c1 | 0.08 | 0.20 | 0.003 | 0.008 |
| D | 2.80 | 3.00 | 0.110 | 0.118 |
| E | 2.60 | 3.00 | 0.102 | 0.118 |
| E1 | 1.50 | 1.70 | 0.059 | 0.067 |
| e | 0.85 | 1.05 | 0.033 | 0.041 |
| e1 | 1.80 | 2.00 | 0.071 | 0.079 |
| L | 0.35 | 0.60 | 0.014 | 0.024 |
| L1 | 0.60REF | | 0.024REF | |
| L2 | 0.25BSC | | 0.010BSC | |
| R | 0.10 | - | 0.004 | - |
| R1 | 0.10 | 0.25 | 0.004 | 0.010 |
| θ | 0° | 8° | 0° | 8° |
| $\theta1$ | 7° | 11° | 7° | 11° |
| $\theta2$ | 8° | 12° | 8° | 12° |

SOP8



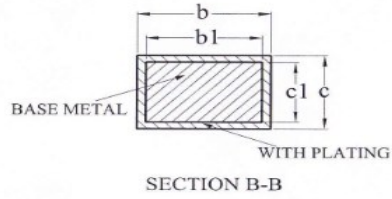
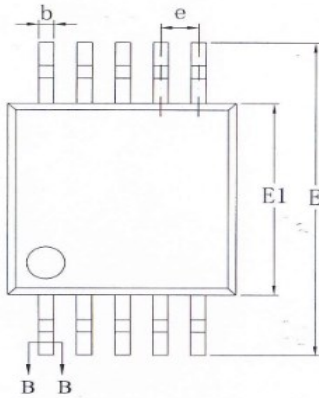
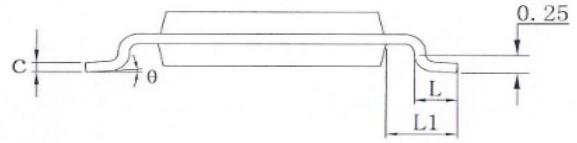
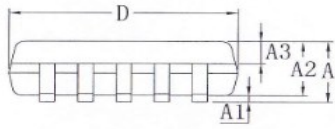
| Symbol | Dimensions (mm) | | Dimensions (inches) | |
|--------|-----------------|-------|---------------------|-------|
| | Min | Max | Min | Max |
| A | 1.350 | 1.750 | 0.053 | 0.069 |
| A1 | 0.100 | 0.250 | 0.004 | 0.010 |
| A2 | 1.350 | 1.550 | 0.053 | 0.061 |
| b | 0.330 | 0.510 | 0.013 | 0.020 |
| c | 0.170 | 0.250 | 0.006 | 0.010 |
| D | 4.700 | 5.100 | 0.185 | 0.200 |
| E | 3.800 | 4.000 | 0.150 | 0.157 |
| E1 | 5.800 | 6.200 | 0.228 | 0.244 |
| e | 1.270 (BSC) | | 0.050 (BSC) | |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| theta | 0° | 8° | 0° | 8° |

DIP8



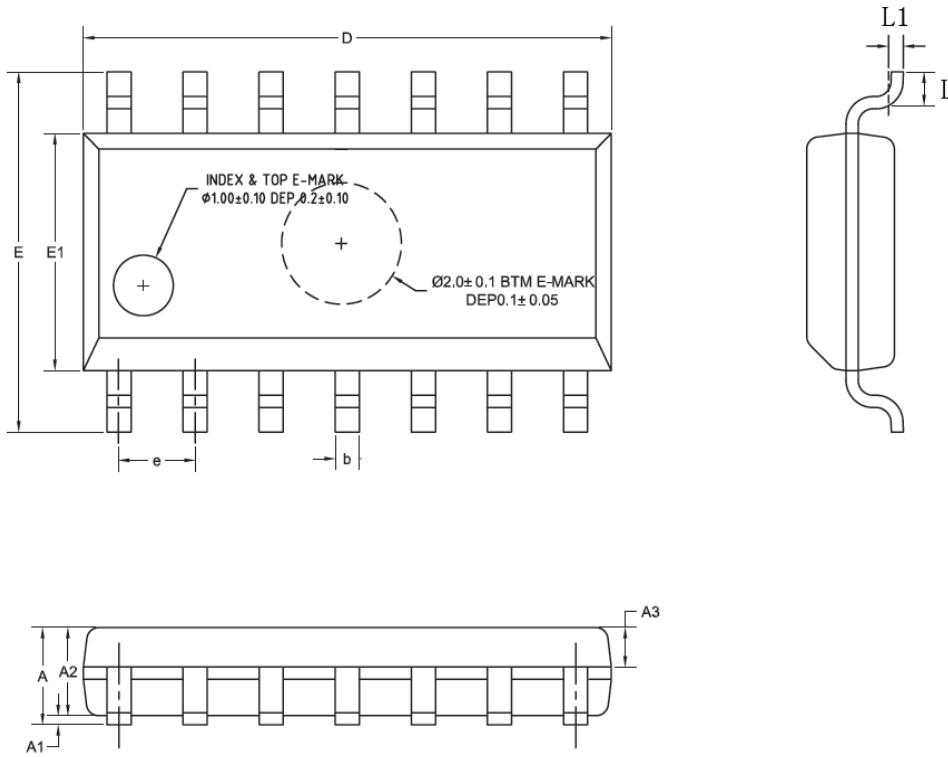
| Symbol | Dimensions (mm) | | Dimensions (inches) | |
|--------|-----------------|-------|---------------------|-------|
| | Min | Max | Min | Max |
| A | 3.600 | 4.000 | 0.142 | 0.157 |
| A1 | 0.510 | - | 0.020 | - |
| A2 | 3.200 | 3.400 | 0.126 | 0.134 |
| A3 | 1.550 | 1.650 | 0.061 | 0.065 |
| b | 0.440 | 0.520 | 0.017 | 0.020 |
| b1 | 0.430 | 0.490 | 0.017 | 0.019 |
| B1 | 1.520 (REF) | | 0.060 (REF) | |
| c | 0.250 | 0.290 | 0.010 | 0.011 |
| c1 | 0.240 | 0.260 | 0.009 | 0.010 |
| D | 9.150 | 9.350 | 0.360 | 0.368 |
| E1 | 6.250 | 6.450 | 0.246 | 0.254 |
| e | 2.540 (BSC) | | 0.100 (BSC) | |
| eA | 7.620 (REF) | | 0.300 (REF) | |
| eB | 7.620 | 9.300 | 0.300 | 0.366 |
| eC | 0 | 0.840 | 0 | 0.033 |
| L | 3.000 | - | 0.118 | - |

MSOP10



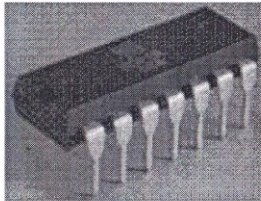
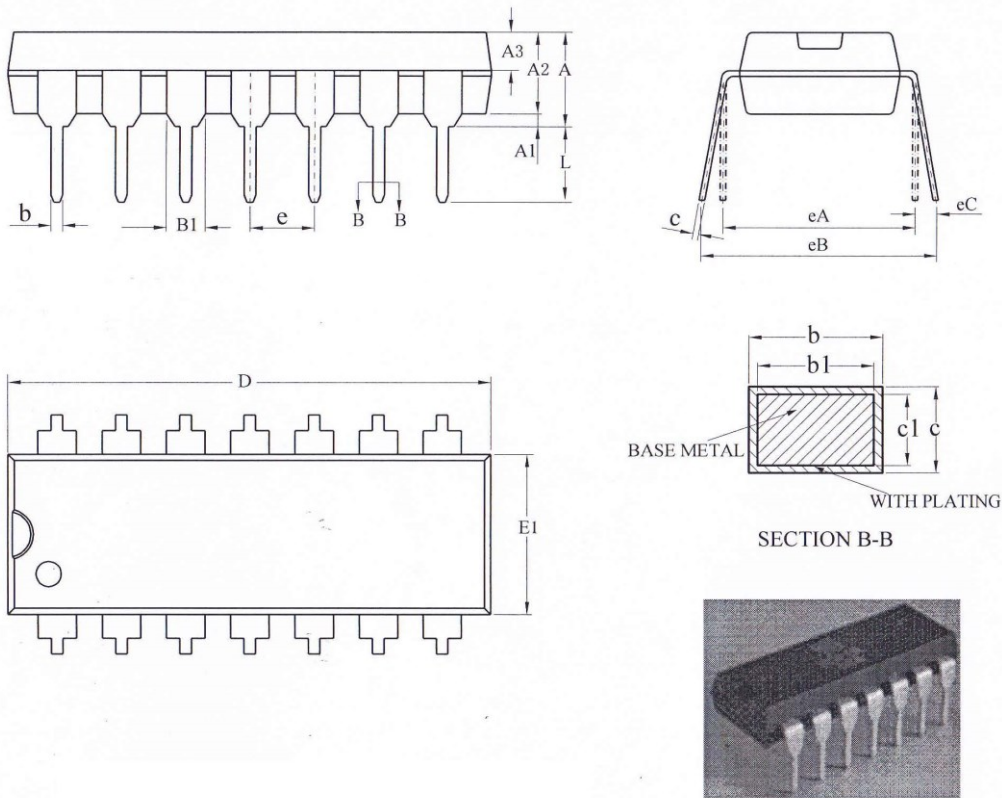
| Symbol | Dimensions (mm) | | Dimensions (inches) | |
|--------|-----------------|-------|---------------------|-------|
| | Min | Max | Min | Max |
| A | - | 1.100 | - | 0.043 |
| A1 | 0.050 | 0.150 | 0.002 | 0.006 |
| A2 | 0.750 | 0.950 | 0.030 | 0.037 |
| A3 | 0.300 | 0.400 | 0.012 | 0.016 |
| b | 0.180 | 0.260 | 0.007 | 0.010 |
| b1 | 0.170 | 0.230 | 0.007 | 0.009 |
| c | 0.150 | 0.190 | 0.006 | 0.007 |
| c1 | 0.140 | 0.160 | 0.006 | 0.006 |
| D | 2.900 | 3.100 | 0.114 | 0.122 |
| E | 4.700 | 5.100 | 0.185 | 0.201 |
| E1 | 2.900 | 3.100 | 0.114 | 0.122 |
| e | 0.500 (BSC) | | 0.020 (BSC) | |
| L | 0.400 | 0.700 | 0.016 | 0.028 |
| L1 | 0.950 (REF) | | 0.037 (REF) | |
| theta | 0 | 8° | 0 | 8° |

SOP14



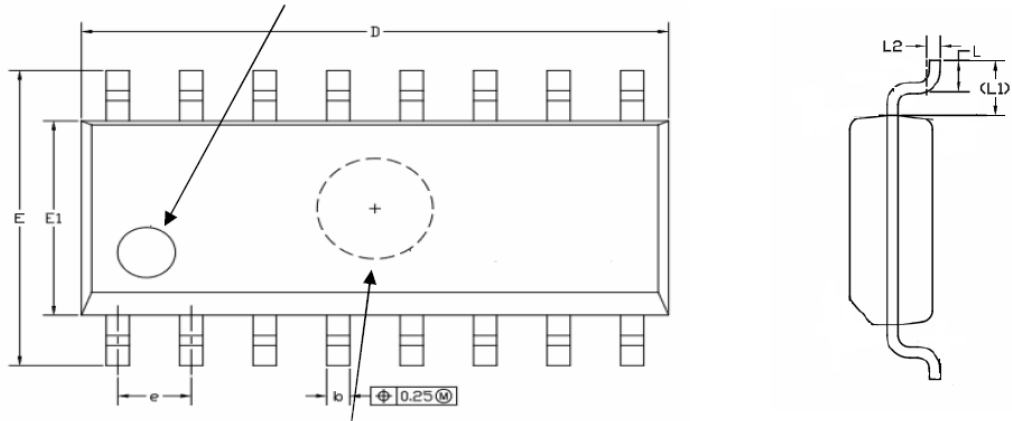
| Symbol | Dimensions (mm) | | Dimensions (inches) | |
|--------|-----------------|-------|---------------------|-------|
| | Min | Max | Min | Max |
| A | - | 1.700 | - | 0.066 |
| A1 | 0.100 | 0.200 | 0.004 | 0.008 |
| A2 | 1.400 | 1.500 | 0.055 | 0.059 |
| A3 | 0.620 | 0.680 | 0.024 | 0.027 |
| b | 0.370 | 0.420 | 0.015 | 0.016 |
| D | 8.710 | 8.910 | 0.343 | 0.347 |
| E | 5.900 | 6.100 | 0.232 | 0.238 |
| E1 | 3.800 | 3.950 | 0.150 | 0.156 |
| e | 1.270 (BSC) | | 0.050 (BSC) | |
| L | 0.500 | 0.700 | 0.020 | 0.027 |
| L1 | 0.250 (BSC) | | 0.010 (BSC) | |

DIP14

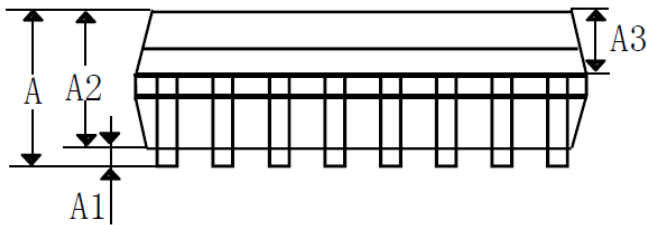


| Symbol | Dimensions (mm) | | Dimensions (inches) | |
|--------|-----------------|--------|---------------------|-------|
| | Min | Max | Min | Max |
| A | 3.600 | 4.000 | 0.142 | 0.157 |
| A1 | 0.510 | - | 0.020 | - |
| A2 | 3.200 | 3.400 | 0.126 | 0.134 |
| A3 | 1.470 | 1.570 | 0.058 | 0.062 |
| b | 0.440 | 0.520 | 0.017 | 0.020 |
| b1 | 0.430 | 0.490 | 0.017 | 0.019 |
| B1 | 1.520 (REF) | | 0.060 (REF) | |
| c | 0.250 | 0.290 | 0.010 | 0.011 |
| c1 | 0.240 | 0.260 | 0.009 | 0.010 |
| D | 19.000 | 19.200 | 0.748 | 0.756 |
| E1 | 6.250 | 6.450 | 0.246 | 0.254 |
| e | 2.540 (BSC) | | 0.100 (BSC) | |
| eA | 7.620 (REF) | | 0.300 (REF) | |
| eB | 7.620 | 9.300 | 0.300 | 0.365 |
| eC | 0 | 0.840 | 0 | 0.033 |
| L | 3.000 | - | 0.118 | - |

SOP16

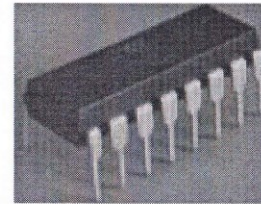
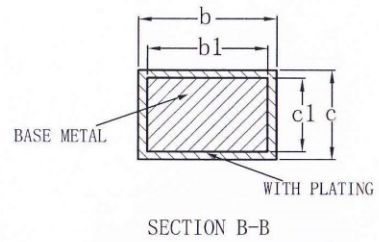
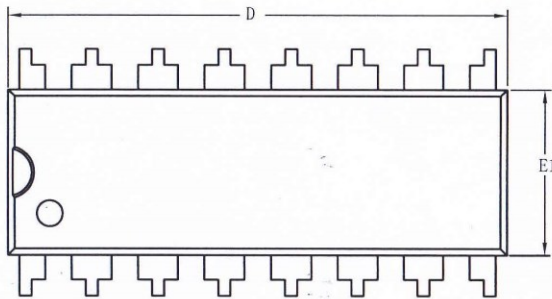
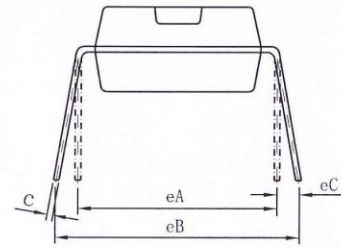
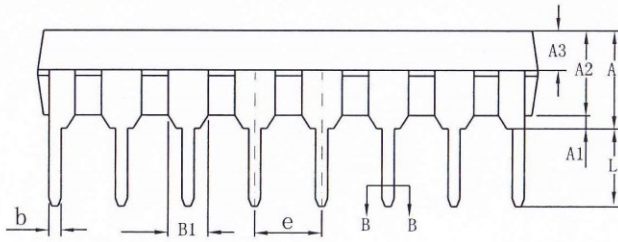


$\Phi 2.0 \pm 0.05$ DEP $0.1 + 0.03 / -0.05$



| Symbol | Dimensions (mm) | | Dimensions (inches) | |
|--------|-----------------|--------|---------------------|-------|
| | Min | Max | Min | Max |
| A | - | 1.700 | - | 0.066 |
| A1 | 0.100 | 0.200 | 0.004 | 0.008 |
| A2 | 1.420 | 1.480 | 0.056 | 0.058 |
| A3 | 0.620 | 0.680 | 0.024 | 0.027 |
| D | 9.960 | 10.160 | 0.392 | 0.396 |
| E | 5.900 | 6.100 | 0.232 | 0.238 |
| E1 | 3.870 | 3.930 | 0.152 | 0.153 |
| b | 0.370 | 0.430 | 0.015 | 0.017 |
| e | 1.240 | 1.300 | 0.048 | 0.051 |
| L | 0.500 | 0.700 | 0.020 | 0.027 |
| L1 | 1.050 (REF) | | 0.041 (REF) | |
| L2 | 0.250 (BSC) | | 0.010 (BSC) | |

DIP16



| Symbol | Dimensions (mm) | | Dimensions (inches) | |
|--------|-----------------|--------|---------------------|-------|
| | Min | Max | Min | Max |
| A | 3.600 | 4.000 | 0.142 | 0.157 |
| A1 | 0.510 | - | 0.020 | - |
| A2 | 3.200 | 3.400 | 0.126 | 0.134 |
| A3 | 1.470 | 1.570 | 0.058 | 0.062 |
| b | 0.440 | 0.520 | 0.017 | 0.020 |
| b1 | 0.430 | 0.490 | 0.017 | 0.019 |
| B1 | 1.520 (REF) | | 0.060 (REF) | |
| c | 0.250 | 0.290 | 0.010 | 0.011 |
| c1 | 0.240 | 0.260 | 0.009 | 0.010 |
| D | 19.000 | 19.200 | 0.748 | 0.756 |
| E1 | 6.250 | 6.450 | 0.246 | 0.254 |
| e | 2.540 (BSC) | | 0.100 (BSC) | |
| eA | 7.620 (REF) | | 0.300 (REF) | |
| eB | 7.620 | 9.300 | 0.300 | 0.365 |
| eC | 0 | 0.840 | 0 | 0.033 |
| L | 3.000 | - | 0.118 | - |

Contact Information**Fremont Micro Devices Corporation**

#5-8, 10/F, Changhong Building
Ke-Ji Nan 12 Road, Nanshan District,
Shenzhen, Guangdong, PRC 518057

Tel: (+86 755) 8611 7811

Fax: (+86 755) 8611 7810

Fremont Micro Devices (HK) Limited

#16, 16/F, Block B, Veristrong Industrial Centre,
34-36 Au Pui Wan Street, Fotan, Shatin, Hong Kong SAR

Tel: (+852) 2781 1186

Fax: (+852) 2781 1144

<http://www.fremontmicro.com>

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