

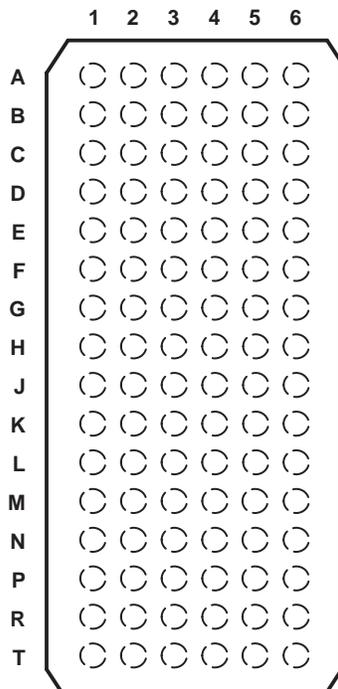
SN74LVTH32245

3.3-V ABT 32-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCBS750A – OCTOBER 2000 – REVISED SEPTEMBER 2003

- Member of the Texas Instruments Widebus+™ Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} and Power-Up 3-State Support Hot Insertion
- Supports Unregulated Battery Operation Down to 2.7 V
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

GKE OR ZKE PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	1B2	1B1	1DIR	1 \overline{OE}	1A1	1A2
B	1B4	1B3	GND	GND	1A3	1A4
C	1B6	1B5	1V $_{CC}$	1V $_{CC}$	1A5	1A6
D	1B8	1B7	GND	GND	1A7	1A8
E	2B2	2B1	GND	GND	2A1	2A2
F	2B4	2B3	1V $_{CC}$	1V $_{CC}$	2A3	2A4
G	2B6	2B5	GND	GND	2A5	2A6
H	2B7	2B8	2DIR	2 \overline{OE}	2A8	2A7
J	3B2	3B1	3DIR	3 \overline{OE}	3A1	3A2
K	3B4	3B3	GND	GND	3A3	3A4
L	3B6	3B5	2V $_{CC}$	2V $_{CC}$	3A5	3A6
M	3B8	3B7	GND	GND	3A7	3A8
N	4B2	4B1	GND	GND	4A1	4A2
P	4B4	4B3	2V $_{CC}$	2V $_{CC}$	4A3	4A4
R	4B6	4B5	GND	GND	4A5	4A6
T	4B7	4B8	4DIR	4 \overline{OE}	4A8	4A7

description/ordering information

ORDERING INFORMATION

T _A	PACKAGE†	Tape and reel	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	LFBGA – GKE	Tape and reel	SN74LVTH32245GKER	HV245
	LFBGA – ZKE (Pb-free)		SN74LVTH32245ZKER	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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description/ordering information (continued)

The SN74LVTH32245 is a 32-bit noninverting 3-state transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

This device can be used as four 8-bit transceivers, two 16-bit transceivers, or one 32-bit transceiver. The device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the devices so that the buses are effectively isolated.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

FUNCTION TABLE
(each 8-bit transceiver)

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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recommended operating conditions (see Note 4)

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	2.7	3.6	V	
V _{IH}	High-level input voltage	2		V	
V _{IL}	Low-level input voltage		0.8	V	
V _I	Input voltage		5.5	V	
I _{OH}	High-level output current		-32	mA	
I _{OL}	Low-level output current		64	mA	
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate	200			μs/V
T _A	Operating free-air temperature	-40	85		°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT		
V _{IK}		V _{CC} = 2.7 V, I _I = -18 mA				-1.2	V		
V _{OH}		V _{CC} = 2.7 V to 3.6 V, I _{OH} = -100 μA		V _{CC} -0.2			V		
		V _{CC} = 2.7 V, I _{OH} = -8 mA		2.4					
		V _{CC} = 3 V, I _{OH} = -32 mA		2					
V _{OL}		V _{CC} = 2.7 V		I _{OL} = 100 μA		0.2	V		
				I _{OL} = 24 mA		0.5			
		V _{CC} = 3 V		I _{OL} = 16 mA		0.4			
				I _{OL} = 32 mA		0.5			
				I _{OL} = 64 mA		0.55			
I _I		V _{CC} = 3.6 V, V _I = V _{CC} or GND				±1	μA		
				V _{CC} = 0 or 3.6 V, V _I = 5.5 V				10	
		V _{CC} = 3.6 V		V _I = 5.5 V				20	
				V _I = V _{CC}				1	
				V _I = 0				-5	
I _{off}		V _{CC} = 0, V _I or V _O = 0 to 4.5 V				±100	μA		
I _{I(hold)}		V _{CC} = 3 V		V _I = 0.8 V		75	μA		
				V _I = 2 V		-75			
		V _{CC} = 3.6 V, §		V _I = 0 to 3.6 V				±500	
I _{OZPU}		V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, \overline{OE} = don't care				±100	μA		
I _{OZPD}		V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, \overline{OE} = don't care				±100	μA		
I _{CC}		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND		Outputs high		0.38	mA		
				Outputs low		10			
				Outputs disabled		0.38			
ΔI _{CC} ¶		V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				0.2	mA		
C _i		V _I = 3 V or 0				4	pF		
C _{io}		V _O = 3 V or 0				10	pF		

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ Unused pins at V_{CC} or GND

§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT
			MIN	TYP†	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	1.5	2.3	3.3	3.7		ns
t _{PHL}			1.3	2.1	3.3	3.5		
t _{PZH}	\overline{OE}	A or B	1.5	2.8	4.5	5.3		ns
t _{PZL}			1.6	2.9	4.6	5.2		
t _{PHZ}	\overline{OE}	A or B	2.3	3.7	5.1	5.5		ns
t _{PLZ}			2.2	3.5	5.1	5.4		
t _{sk(o)}						0.5		ns

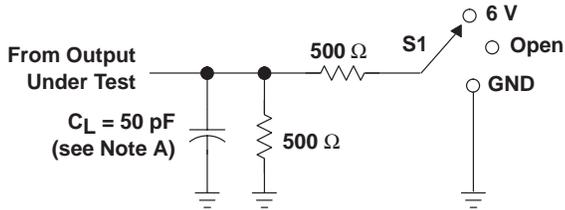
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.



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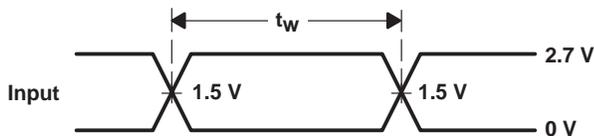
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PARAMETER MEASUREMENT INFORMATION

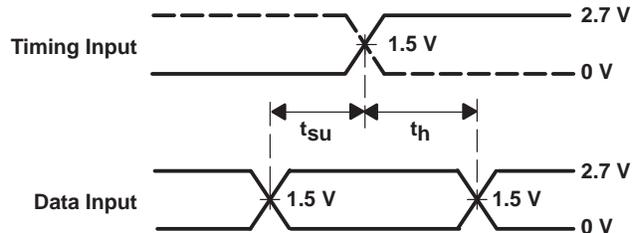


LOAD CIRCUIT

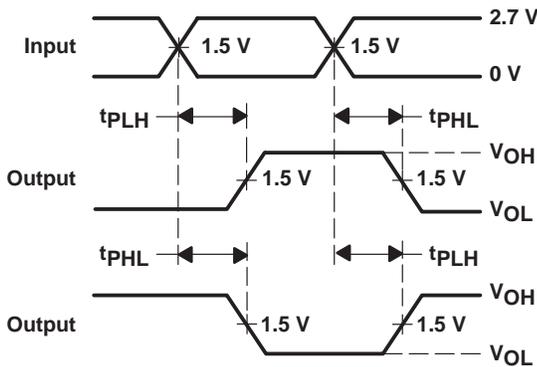
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



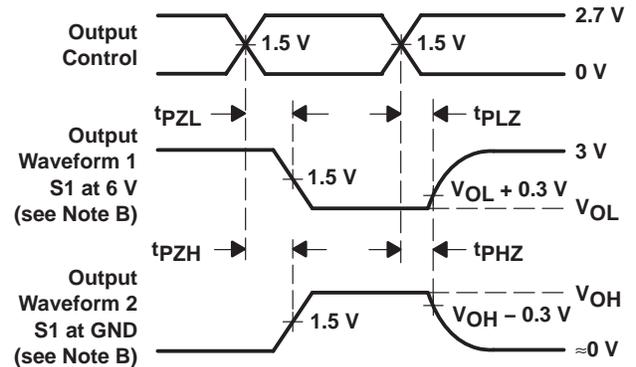
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LVTH32245GKER	ACTIVE	LFBGA	GKE	96	1000	TBD	SNPB	Level-3-220C-168 HR
SN74LVTH32245ZKER	ACTIVE	LFBGA	ZKE	96	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-250C-168 HR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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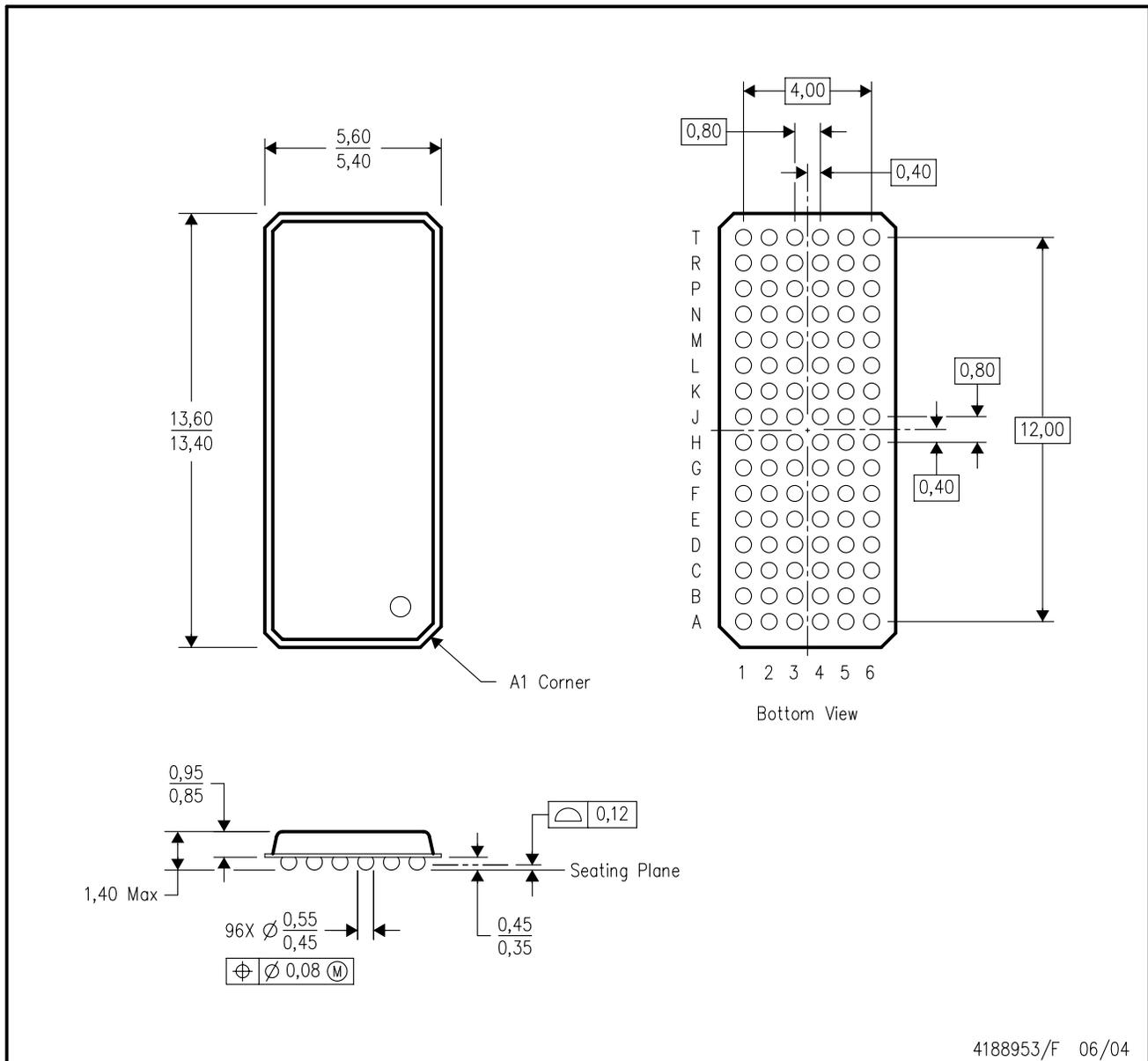
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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GKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY

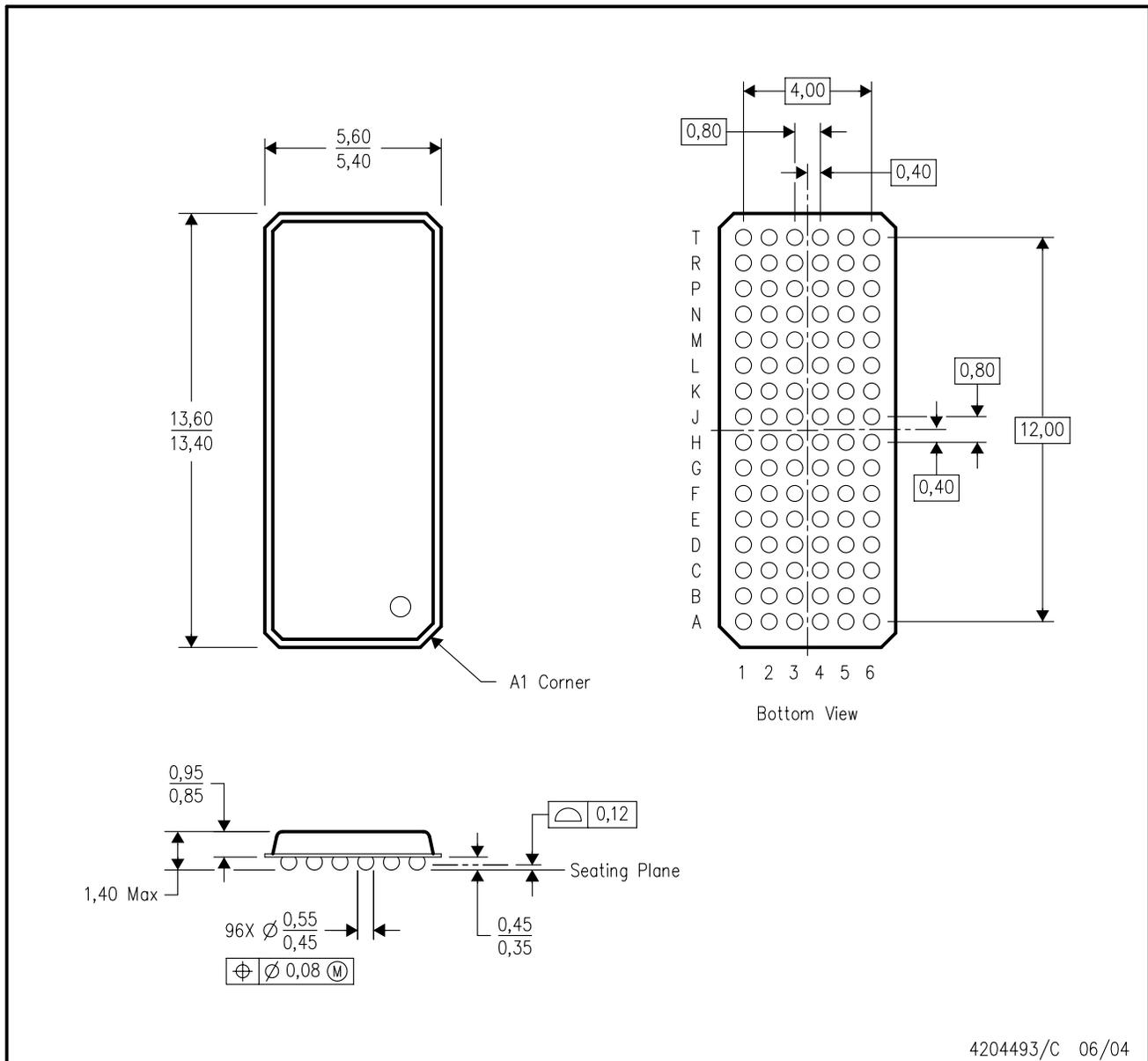


4188953/F 06/04

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-205 variation CC.
 - D. This package is tin-lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead-free.

ZKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-205 variation CC.
 - D. This package is lead-free. Refer to the 96 GKE package (drawing 4188953) for tin-lead (SnPb).

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