AMC1351 Precision, 5-V Input, Reinforced Isolated Amplifier

1 Features

- Linear input voltage range: –0.25 V to 5 V
- High input impedance: 1.25 MΩ (typ)
- Fixed gain: 0.4 V/V
- Low DC errors:
  - Offset error ±1.5 mV (max)
  - Offset drift: ±15 µV/°C (max)
  - Gain error: ±0.2% (max)
  - Gain drift: ±35 ppm/°C (max)
  - Nonlinearity ±0.02% (max)
- Operation on high-side and low-side: 3.3 V or 5 V
- High CMTI: 100 kV/µs (min)
- Fail-safe output
- Safety-related certifications:
  - 7070-V_{PK} reinforced isolation per DIN VDE V 0884-11: 2017-01
  - 5000-V_{RMS} isolation for 1 minute per UL1577
- Fully specified over the extended industrial temperature range: –40°C to +125°C

2 Applications

- Isolated DC voltage sensing in:
  - Motor drives
  - Frequency inverters
  - Solar inverters
  - Power supplies

3 Description

The AMC1351 is a precision, isolated amplifier with an output separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced galvanic isolation of up to 5 kV_{RMS} according to VDE V 0884-11 and UL1577, and supports a working voltage of up to 1.5 kV_{RMS}.

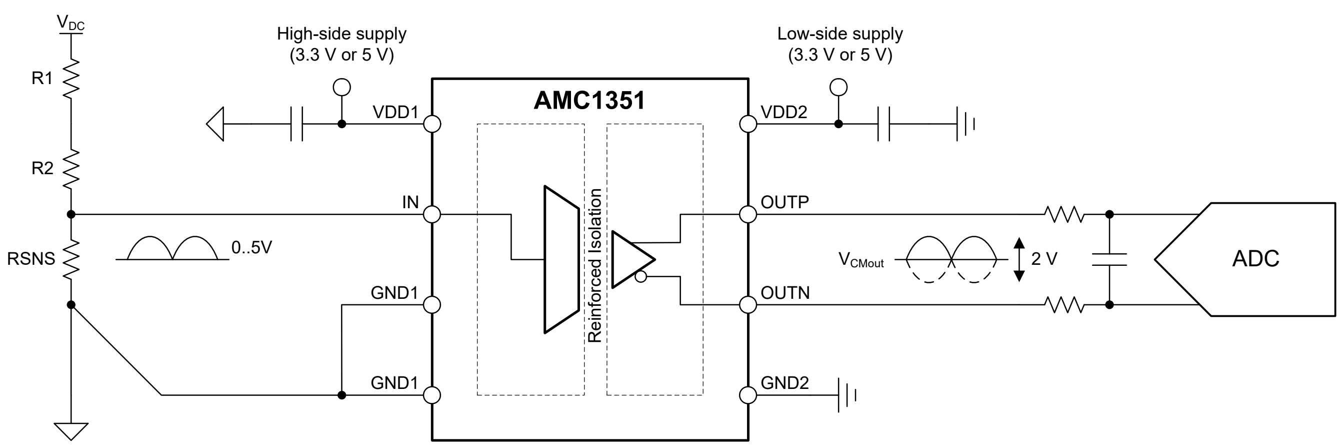
The isolation barrier separates parts of the system that operate on different common-mode voltage levels and protects the low-voltage side from potentially harmful voltages and damage.

The high-impedance input of the AMC1351 is optimized for connection to high-impedance resistive dividers or other voltage signal sources with high output resistance. The excellent accuracy and low temperature drift supports accurate DC voltage sensing in DC/DC converters, frequency inverters, motor-drive, or other applications over the extended industrial temperature range from –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AMC1351	SOIC (8)	5.85 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2021	*	Initial Release

5 Pin Configuration and Functions

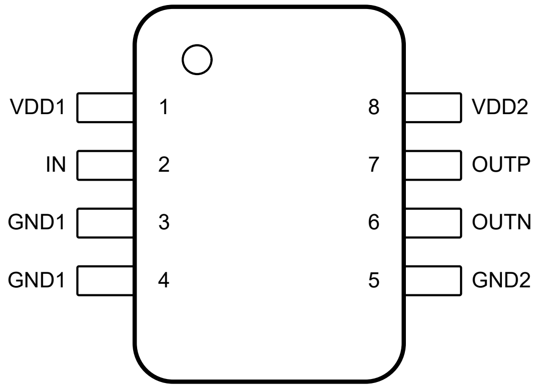


Figure 5-1. DWV Package, 8-Pin SOIC (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VDD1	High-side power	High-side power supply(1)
2	IN	Analog input	Analog input
3	GND1	High-side ground	High-side analog ground reference for input amplifier. Connect to pin 4. Do not leave unconnected.
4	GND1	High-side ground	High-side analog ground
5	GND2	Low-side ground	Low-side analog ground
6	OUTN	Analog output	Inverting analog output
7	OUTP	Analog output	Noninverting analog output
8	VDD2	Low-side power	Low-side power supply(1)

(1) See the *Power Supply Recommendations* section for power-supply decoupling recommendations.

6 Specifications

6.1 Absolute Maximum Ratings

see[(1)]

		MIN	MAX	UNIT
Power-supply voltage	High-side VDD1 to GND1	–0.3	6.5	V
	Low-side VDD2 to GND2	–0.3	6.5	
Analog input voltage	IN	–1	15	V
Analog output voltage	OUTP, OUTN	GND2 – 0.5	VDD2 + 0.5	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged-device model (CDM), per per ANSI/ESDA/JEDEC JS-002[(2)]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
VDD1	High-side power-supply	VDD1 to GND1	3	5	5.5	V
VDD2	Low-side power-supply	VDD2 to GND2	3	3.3	5.5	V
ANALOG INPUT						
$V_{Clipping}$	Input voltage before clipping output			6.25		V
V_{FSR}	Specified linear full-scale voltage		–0.25		5	V
ANALOG OUTPUT						
C_{LOAD}	Capacitive load	On OUTP or OUTN to GND2			500	pF
		OUTP to OUTN			250	
R_{LOAD}	Resistive load	On OUTP or OUTN to GND2		10	1	kΩ
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–55		125	°C
	Specified ambient temperature		–40		125	

6.4 Thermal Information

THERMAL METRIC[(1)]		AMC1351 DWV (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	39.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation (both sides)	VDD1 = VDD2 = 5.5 V	96	mW
P_{D1}	Maximum power dissipation (high-side)	VDD1 = 3.6 V	29	mW
		VDD1 = 5.5 V	51	
P_{D2}	Maximum power dissipation (low-side)	VDD2 = 3.6 V	26	mW
		VDD2 = 5.5 V	45	

6.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest pin-to-pin distance through air	≥ 8.5	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	≥ 8.5	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation	≥ 0.021	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN VDE V 0884-11 (VDE V 0884-11): 2017-01				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	2120	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave)	1500	V_{RMS}
		At DC voltage	2120	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification test)	7070	V_{PK}
		$V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production test)	8480	
V_{IOSM}	Maximum surge isolation voltage(2)	Test method per IEC 60065, 1.2/50-µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 12800\ V_{PK}$ (qualification)	8000	V_{PK}
q_{pd}	Apparent charge(3)	Method a, after input/output safety test subgroups 2 and 3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤ 5	
		Method b1, at routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s, $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(4)	$V_{IO} = 0.5\ V_{PP}$ at 1 MHz	~1.5	pF
R_{IO}	Insulation resistance, input to output(4)	V_{IO} = 500 V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^{9}	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 5000\ V_{RMS}$ or 7071 V_{DC}, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO} = 6000\ V_{RMS}$, t = 1 s (100% production test)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(3) Apparent charge is electrical discharge caused by a partial discharge (pd).
(4) All pins on each side of the barrier are tied together, creating a two-pin device.

6.7 Safety-Related Certifications

VDE	UL
Certified according to DIN VDE V 0884-11 (VDE V 0884-11): 2017-01, DIN EN 60950-1 (VDE 0805 Teil 1): 2014-08, and DIN EN 60065 (VDE 0860): 2005-11	Recognized under 1577 component recognition
Reinforced insulation	Single protection
Certificate number: pending	File number: E181974

6.8 Safety Limiting Values

Safety limiting[(1)] intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 84.6°C/W, VDDx = 5.5 V, T_J = 150°C, T_A = 25°C			270	mA
		$R_{\theta JA}$ = 84.6°C/W, VDDx = 3.6 V, T_J = 150°C, T_A = 25°C			410	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 84.6°C/W, T_J = 150°C, T_A = 25°C			1480	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times VDD_{max}$, where VDD_{max} is the maximum supply voltage for high-side and low-side.

6.9 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD1 = 3.0 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, IN = –0.25 V to +5 V (unless otherwise noted); typical specifications are at T_A = 25°C, VDD1 = 5 V, and VDD2 = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
V_{OS}	Offset voltage[2]	T_A = 25°C, IN = GND1, 4.5 V ≤ VDD1 ≤ 5.5 V[1]	–1.5	±0.3	1.5	mV
		T_A = 25°C, IN = GND1, 3.0 V ≤ VDD1 ≤ 5.5 V[3]	–2.5	–0.8	2.5	
ΔV_{OS}	Offset voltage long-term stability	10 years at T_A = 55°C		0[7]		mV
TCV_{OS}	Offset voltage thermal drift[5]	IN = GND1	–15	±3	15	µV/°C
ΔTCV_{OS}	Offset voltage thermal drift long-term stability	10 years at T_A = 55°C, IN = GND1		0[7]		mV/°C
R_{IN}	Input resistance		1	1.25	1.5	MΩ
ΔR_{IN}	Input resistance long-term stability	10 years at T_A = 55°C		0[7]		ppm
TCR_{IN}	Input resistance thermal drift	–40°C ≤ T_A ≤ 85°C		5		ppm/°C
C_{IN}	Input capacitance	f_{IN} = 275 kHz		4		pF
ANALOG OUTPUT						
	Nominal gain			0.40		V/V
E_G	Gain error[1]	T_A = 25°C	–0.2%	±0.05%	0.2%	
ΔE_G	Gain error long-term stability	10 years at T_A = 55°C		0[7]		
TCE_G	Gain error thermal drift[1] [6]		–35	±10	35	ppm/°C
ΔTCE_G	Gain error thermal drift long-term stability	10 years at T_A = 55°C		0[7]		ppm/°C
	Nonlineartity[1]		–0.02%	±0.003%	0.02%	
	Nonlinearity thermal drift			0.2		ppm/°C
THD	Total harmonic distortion[4]	V_{IN} = 5 V_{PP}, f_{IN} = 10 kHz, BW = 100 kHz		–82		dB
SNR	Signal-to-noise ratio	V_{IN} = 5 V_{PP}, f_{IN} = 1 kHz, BW = 10 kHz	75	79		dB
		V_{IN} = 5 V_{PP}, f_{IN} = 10 kHz, BW = 100 kHz		69		
	Output noise	IN = GND1, BW = 100 kHz		250		µVrms
PSRR	Power-supply rejection ratio[2]	PSRR vs VDD1, DC		–67		dB
		PSRR vs VDD2, DC		–80		
		PSRR vs VDD1 with 10-kHz, 100-mV ripple		–65		
		PSRR vs VDD2 with 10-kHz, 100-mV ripple		–64		
V_{CMout}	Output common-mode voltage		1.39	1.44	1.49	V
$V_{CLIPout}$	Clipping differential output voltage	V_{OUT} = (V_{OUTP} – V_{OUTN}), V_{IN} > $V_{Clipping}$		2.49		V
$V_{Fail\text{-}safe}$	Fail-safe differential output voltage	VDD1 undervoltage or VDD1 missing		–2.57	–2.5	V
BW	Output bandwidth		275	300		kHz
R_{OUT}	Output resistance	On OUTP or OUTN		< 0.2		Ω
	Output short-circuit current	On OUTP or OUTN, sourcing or sinking, IN = GND1, outputs shorted to either GND or VDD2		14		mA
CMTI	Common-mode transient immunity		100	150		kV/µs
POWER SUPPLY						

6.9 Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD1 = 3.0 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, IN = –0.25 V to +5 V (unless otherwise noted); typical specifications are at T_A = 25°C, VDD1 = 5 V, and VDD2 = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$VDD1_{UV}$	VDD1 undervoltage detection threshold	VDD1 rising	2.5	2.7	2.9	V
		VDD1 falling	2.4	2.6	2.8	
$VDD2_{UV}$	VDD2 undervoltage detection threshold	VDD2 rising	2.2	2.45	2.65	V
		VDD2 falling	1.85	2.0	2.2	
I_{DD1}	High-side supply current	3.0 V < VDD1 < 3.6 V		6.0	8.1	mA
		4.5 V < VDD1 < 5.5 V		7.0	9.3	
I_{DD2}	Low-side supply current	3.0 V < VDD2 < 3.6 V		5.3	7.2	mA
		4.5 V < VDD2 < 5.5 V		5.9	8.1	

(1) The typical value includes one standard deviation (*sigma*) at nominal operating conditions.
(2) This parameter is input referred.
(3) The typical value is at VDD1 = 3.3 V.
(4) THD is the ratio of the rms sum of the amplitues of first five higher harmonics to the amplitude of the fundamental.
(5) Offset error temperature drift is calculated using the box method, as described by the following equation: $TCV_{OS} = (V_{OS,MAX} - V_{OS,MIN}) / TempRange$ where $V_{OS,MAX}$ and $V_{OS,MIN}$ refer to the maximum and minimum V_{OS} values measured within the temperature range (–40 to 125℃).
(6) Gain error temperature drift is calculated using the box method, as described by the following equation: $TCE_G (ppm) = ((E_{G,MAX} - E_{G,MIN}) / TempRange) \times 10^4$ where $E_{G,MAX}$ and $E_{G,MIN}$ refer to the maximum and minimum E_G values (in %) measured within the temperature range (–40 to 125℃).
(7) Value is below measurement capability.

6.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output signal rise time			1.3		µs
t_f	Output signal fall time			1.3		µs
	IN to OUTx signal delay (50% – 10%)	Unfiltered output		1	1.5	µs
	IN to OUTx signal delay (50% – 50%)	Unfiltered output		1.6	2.1	µs
	IN to OUTx signal delay (50% – 90%)	Unfiltered output		2.5	3	µs
t_{AS}	Analog settling time	VDD1 step to 3.0 V with VDD2 ≥ 3.0 V, to V_{OUTP} and V_{OUTN} valid, 0.1% settling		500	800	µs

6.11 Timing Diagram

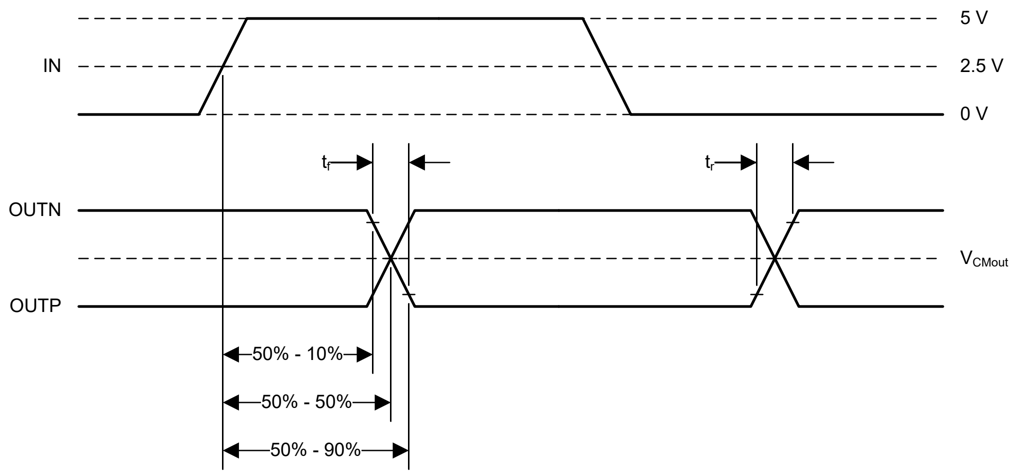


Figure 6-1. Rise, Fall, and Delay Time Definition

6.12 Insulation Characteristics Curves

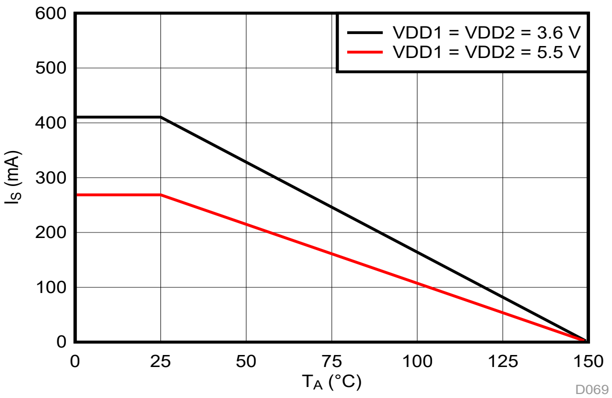


Figure 6-2. Thermal Derating Curve for Safety-Limiting Current per VDE

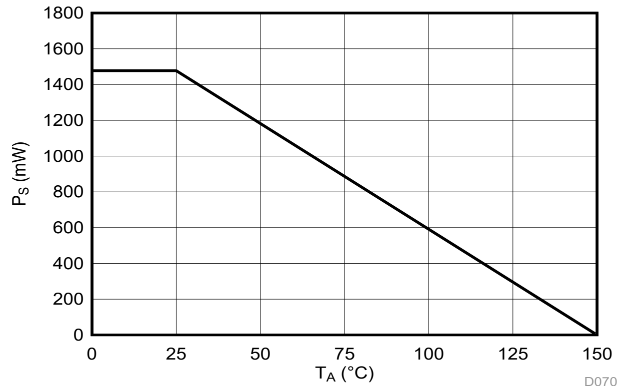
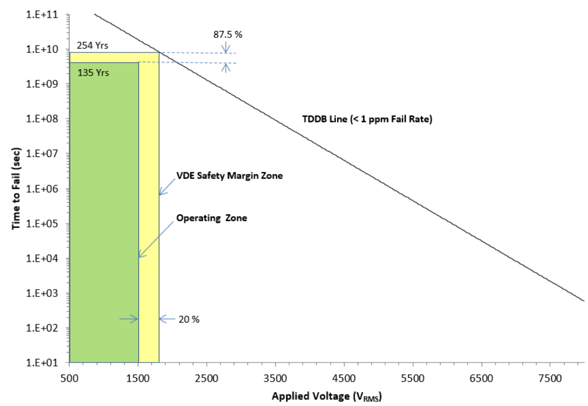


Figure 6-3. Thermal Derating Curve for Safety-Limiting Power per VDE



T_A up to 150°C, stress-voltage frequency = 60 Hz, isolation working voltage = 1500 V_{RMS}, operating lifetime = 135 years

Figure 6-4. Reinforced Isolation Capacitor Lifetime Projection

6.13 Typical Characteristics

at VDD1 = 5 V, VDD2 = 3.3 V, IN = 0 V to 5 V, and f_{IN} = 10 kHz (unless otherwise noted)

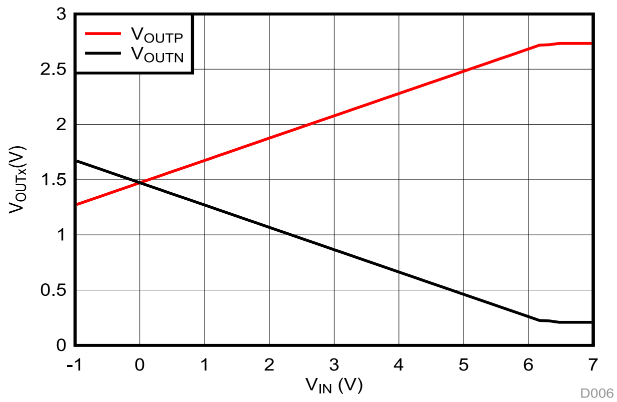
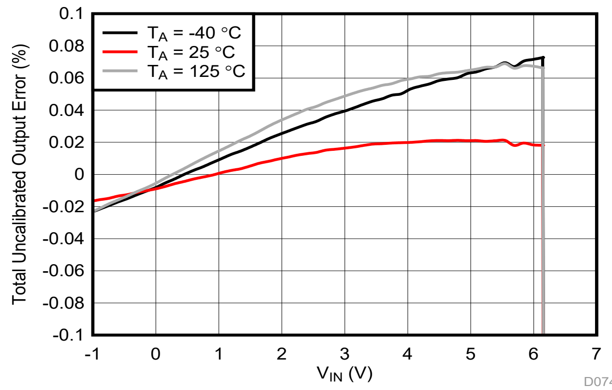


Figure 6-5. Output Voltage vs Input Voltage



Total uncalibrated output error is defined as: $(V_{OUT} – V_{IN} × G) / (V_{Clipping} × G)$, where G is the nominal gain of the device (0.4 V/V) and $V_{Clipping}$ is 6.25 V

Figure 6-6. Total Uncalibrated Output Error vs Input Voltage

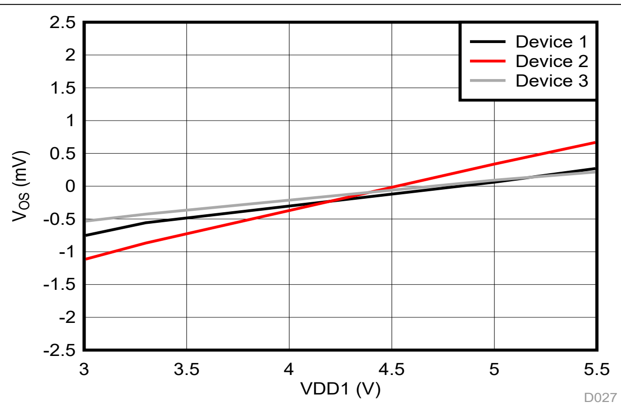


Figure 6-7. Input Offset Voltage vs High-Side Supply Voltage

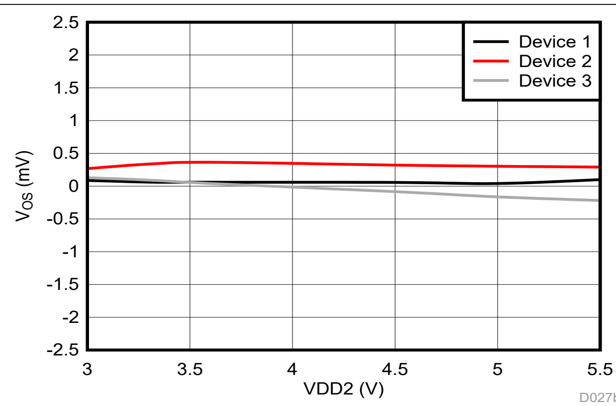


Figure 6-8. Input Offset Voltage vs Low-Side Supply Voltage

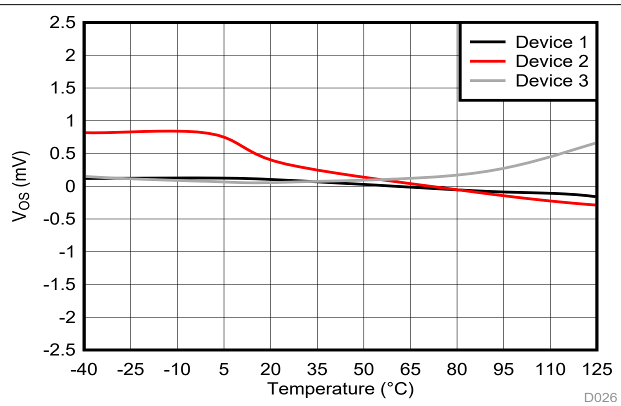


Figure 6-9. Input Offset Voltage vs Temperature

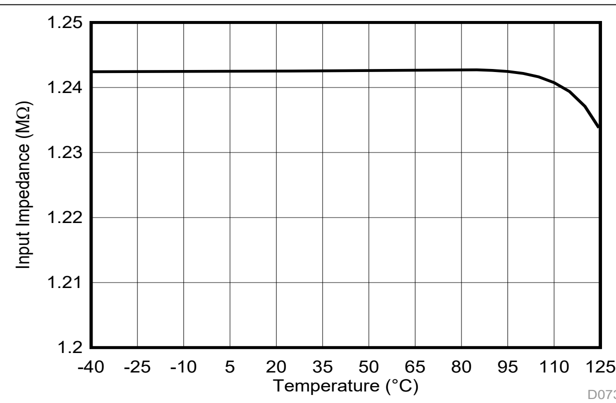


Figure 6-10. Input Impedance vs Temperature

6.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, IN = 0 V to 5 V, and f_{IN} = 10 kHz (unless otherwise noted)

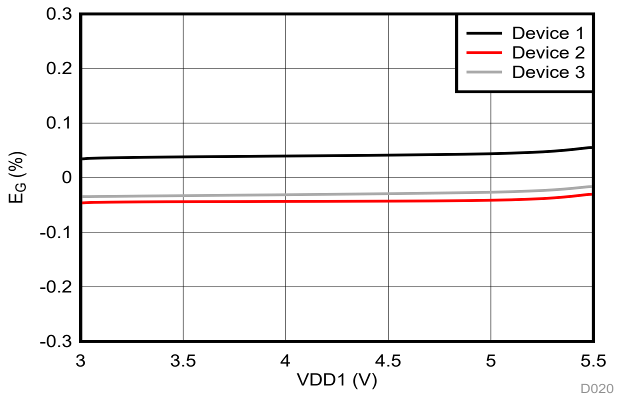


Figure 6-11. Gain Error vs High-Side Supply Voltage

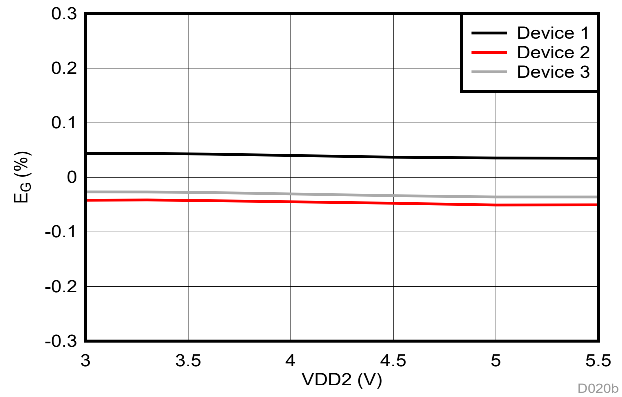


Figure 6-12. Gain Error vs Low-Side Supply Voltage

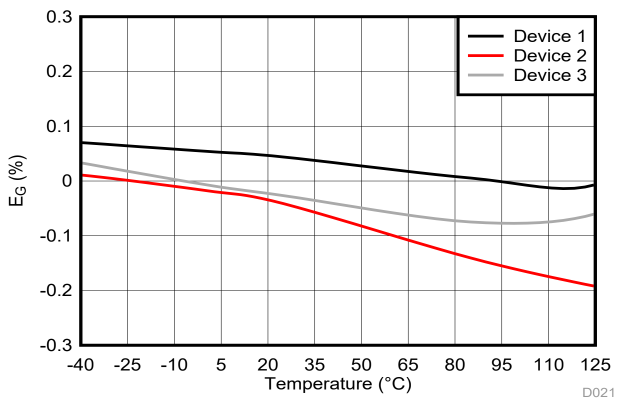


Figure 6-13. Gain Error vs Temperature

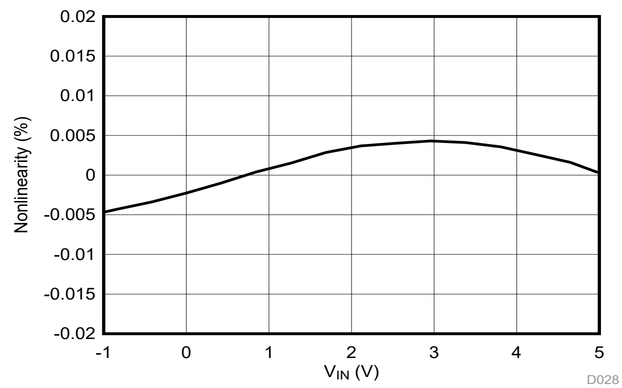


Figure 6-14. Nonlinearity vs Input Voltage

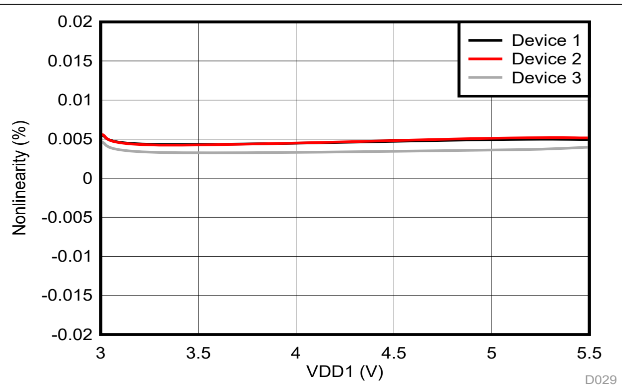


Figure 6-15. Nonlinearity vs High-Side Supply Voltage

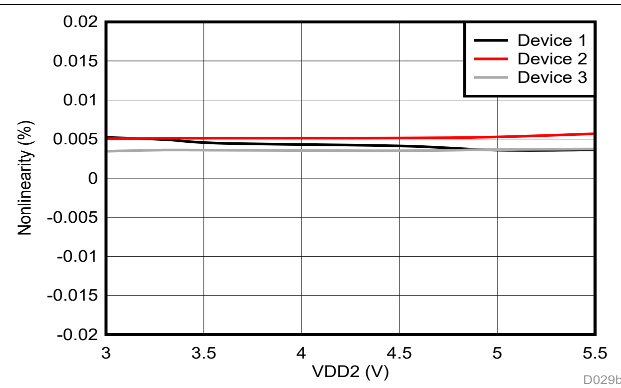


Figure 6-16. Nonlinearity vs Low-Side Supply Voltage

6.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, IN = 0 V to 5 V, and f_{IN} = 10 kHz (unless otherwise noted)

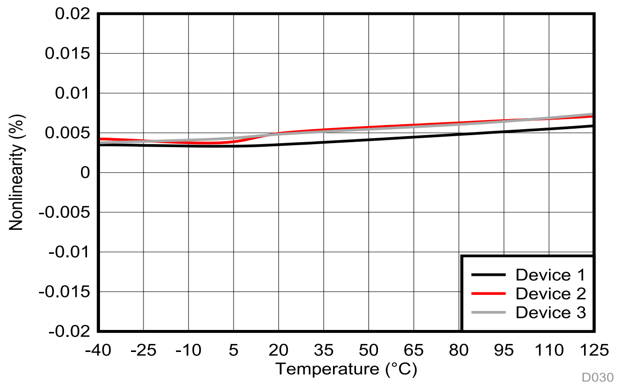


Figure 6-17. Nonlinearity vs Temperature

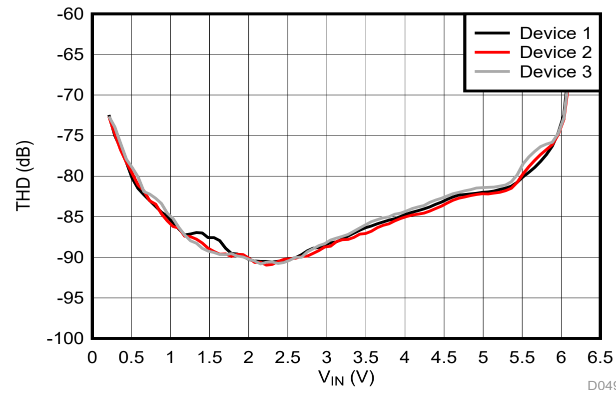


Figure 6-18. Total Harmonic Distortion vs Input Voltage

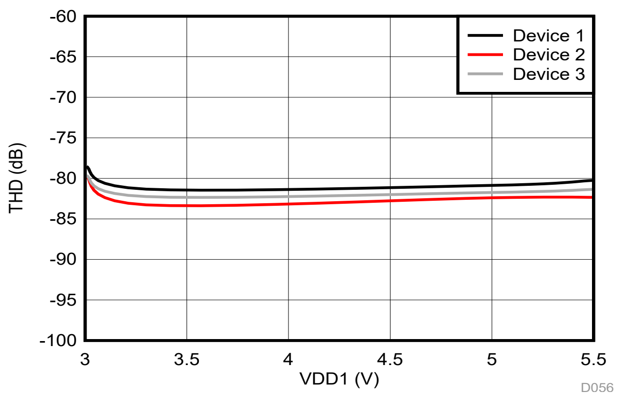


Figure 6-19. Total Harmonic Distortion vs High-Side Supply Voltage

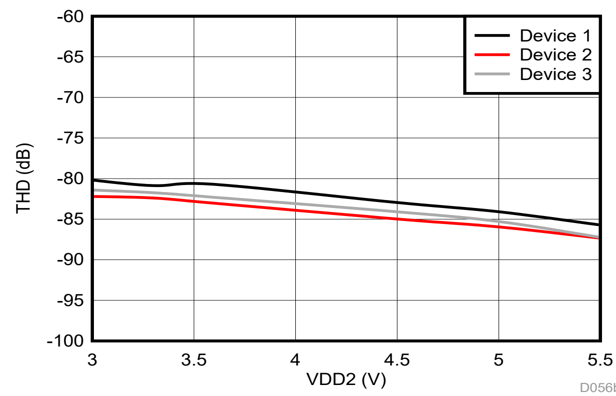


Figure 6-20. Total Harmonic Distortion vs Low-Side Supply Voltage

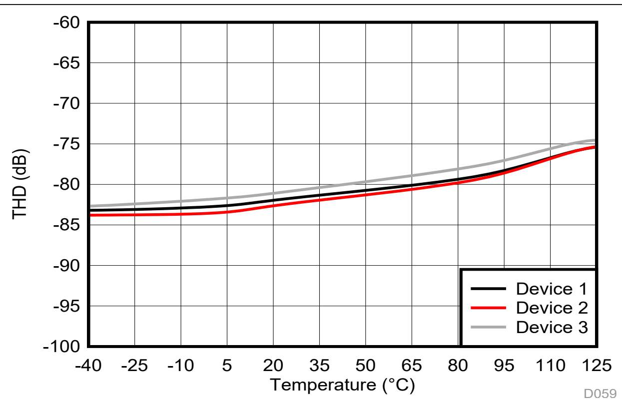


Figure 6-21. Total Harmonic Distortion vs Temperature

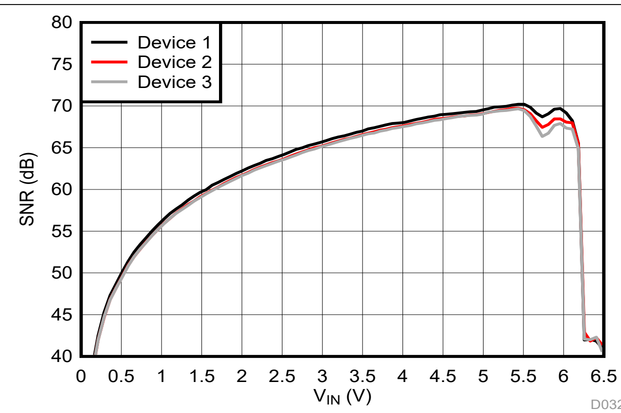


Figure 6-22. Signal-to-Noise Ratio vs Input Voltage

6.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, IN = 0 V to 5 V, and f_{IN} = 10 kHz (unless otherwise noted)

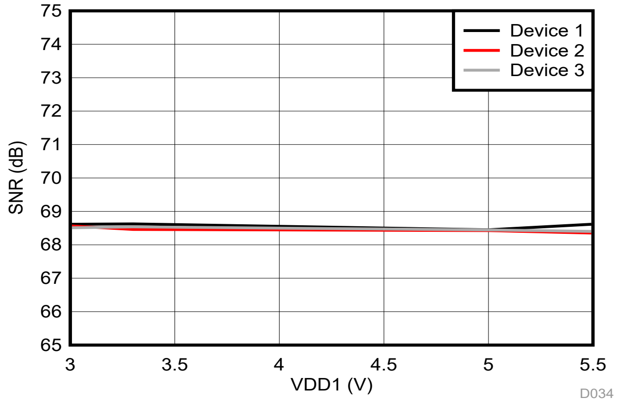


Figure 6-23. Signal-to-Noise Ratio vs High-Side Supply Voltage

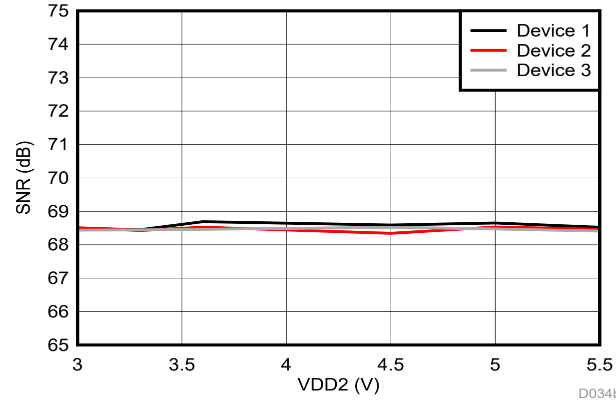


Figure 6-24. Signal-to-Noise Ratio vs Low-Side Supply Voltage

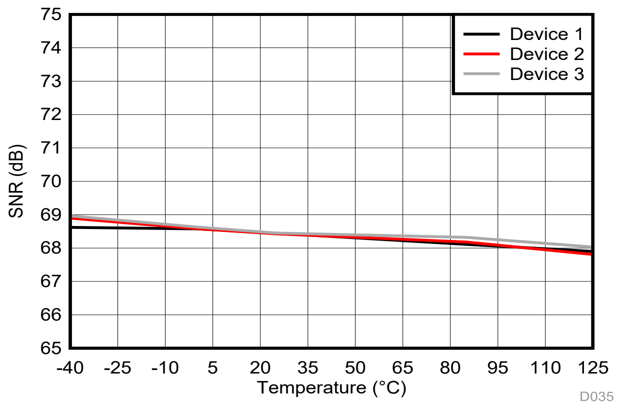


Figure 6-25. Signal-to-Noise Ratio vs Temperature

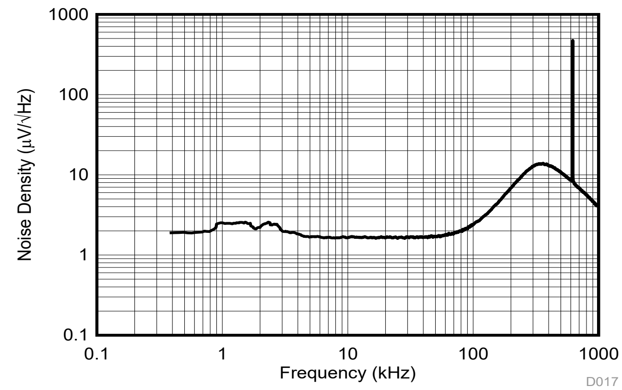


Figure 6-26. Input-Referred Noise Density vs Frequency

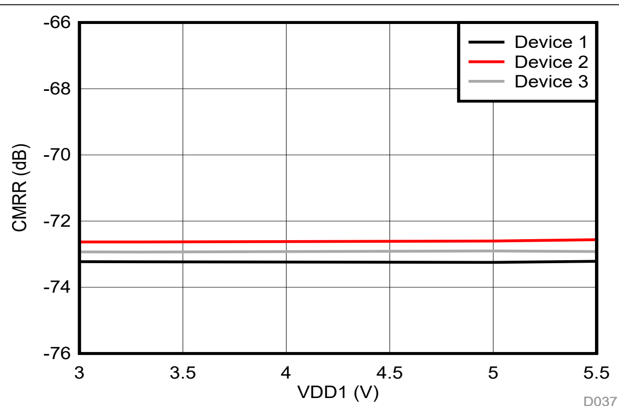


Figure 6-27. Common-Mode Rejection Ratio vs Supply Voltage

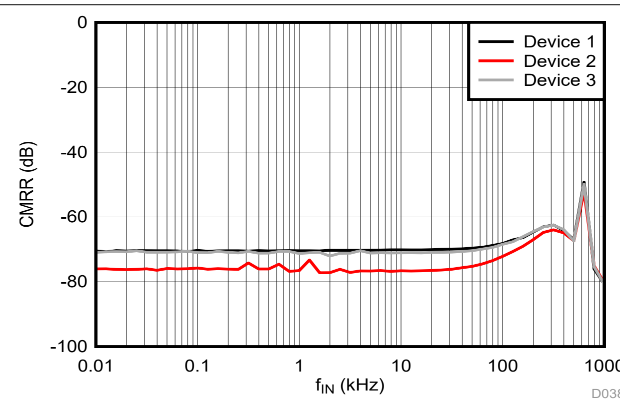
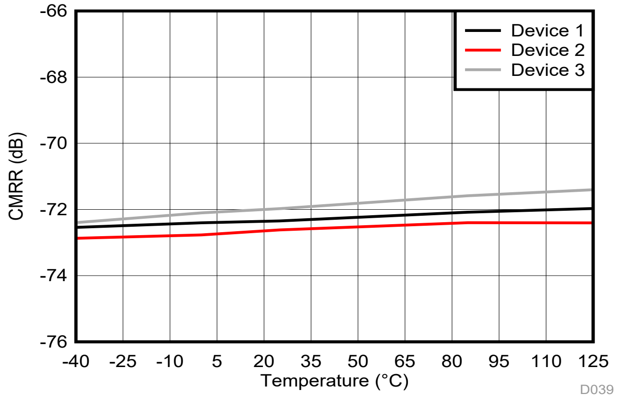


Figure 6-28. Common-Mode Rejection Ratio vs Input Frequency

6.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, IN = 0 V to 5 V, and f_{IN} = 10 kHz (unless otherwise noted)



f_{IN} = 10 kHz

Figure 6-29. Common-Mode Rejection Ratio vs Temperature

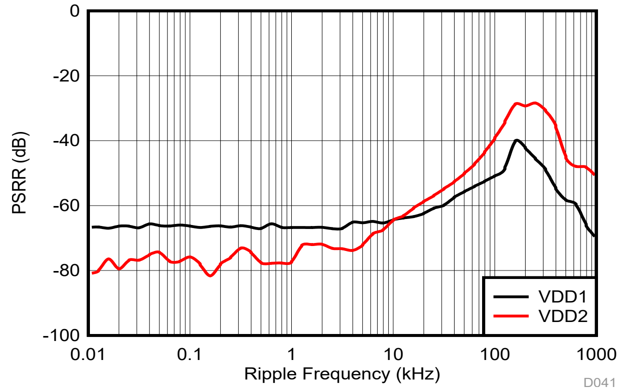
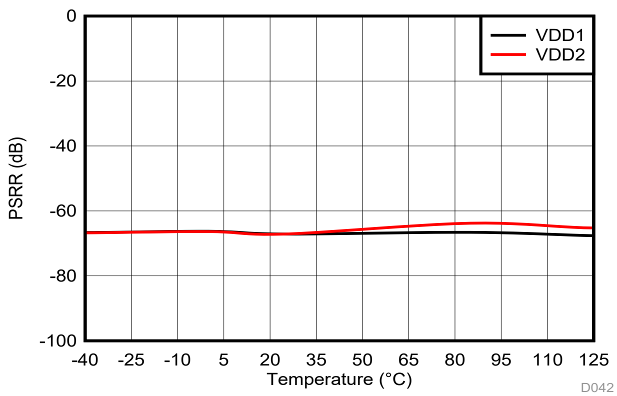


Figure 6-30. Power-Supply Rejection Ratio vs Ripple Frequency



f_{Ripple} = 10 kHz

Figure 6-31. Power-Supply Rejection Ratio vs Temperature

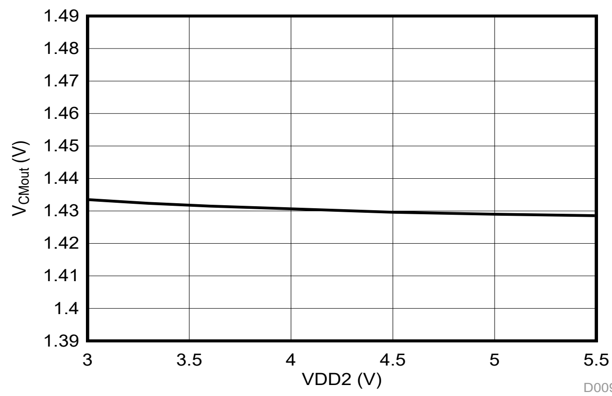


Figure 6-32. Common-Mode Output Voltage vs Supply Voltage

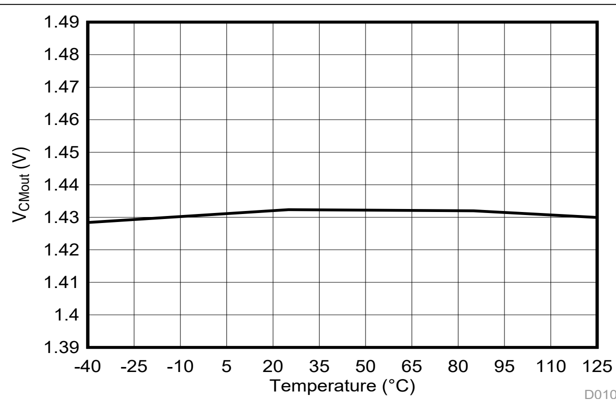


Figure 6-33. Common-Mode Output Voltage vs Temperature

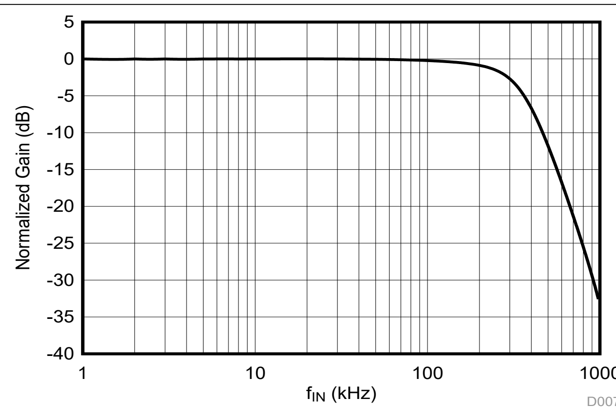


Figure 6-34. Normalized Gain vs Input Frequency

6.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, IN = 0 V to 5 V, and f_{IN} = 10 kHz (unless otherwise noted)

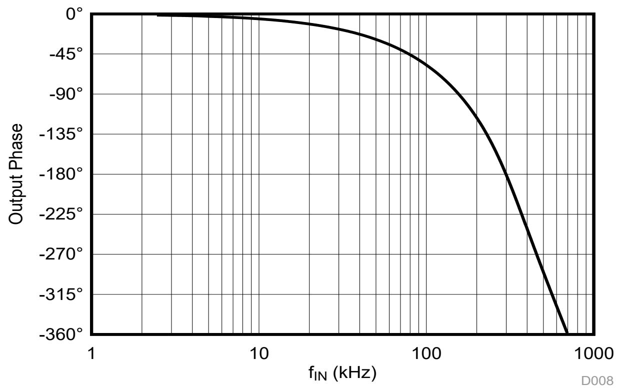


Figure 6-35. Output Phase vs Input Frequency

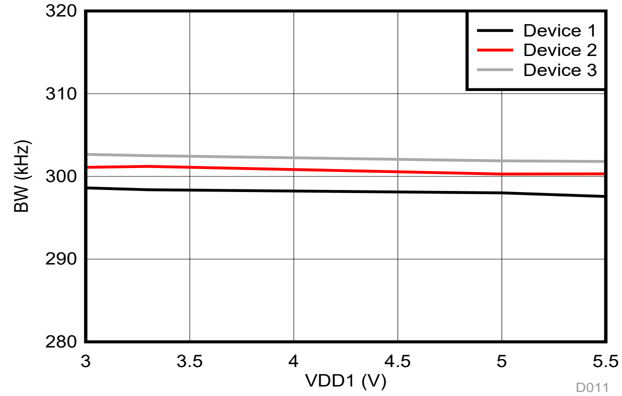


Figure 6-36. Bandwidth vs Supply Voltage

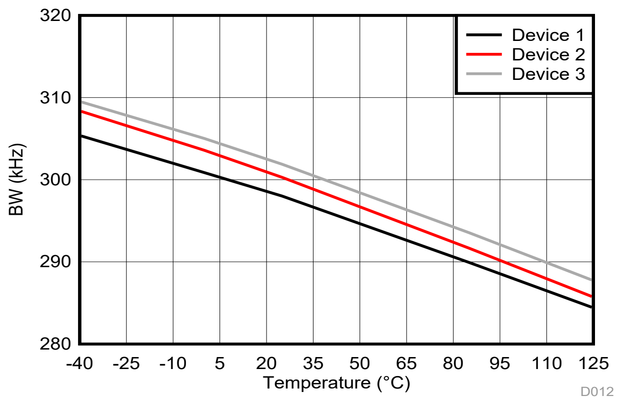


Figure 6-37. Bandwidth vs Temperature

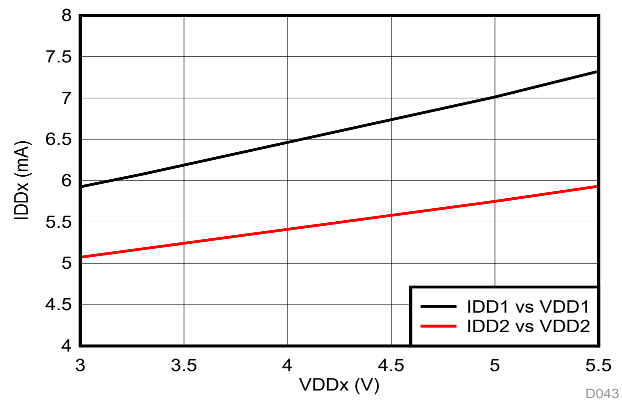


Figure 6-38. Supply Current vs Supply Voltage

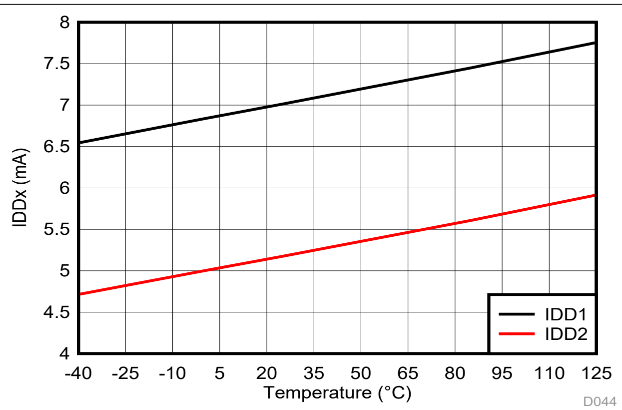


Figure 6-39. Supply Current vs Temperature

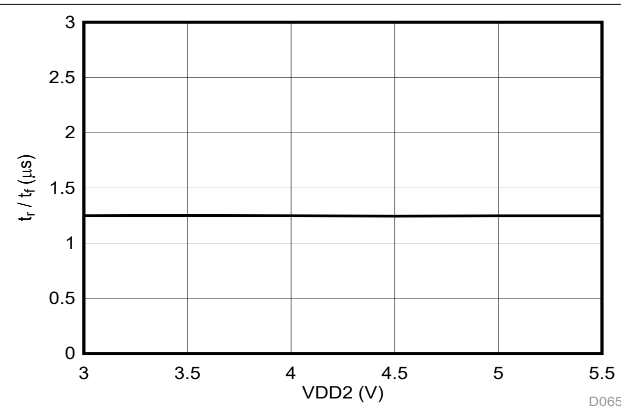


Figure 6-40. Output Rise and Fall Time vs Supply Voltage

6.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, IN = 0 V to 5 V, and f_{IN} = 10 kHz (unless otherwise noted)

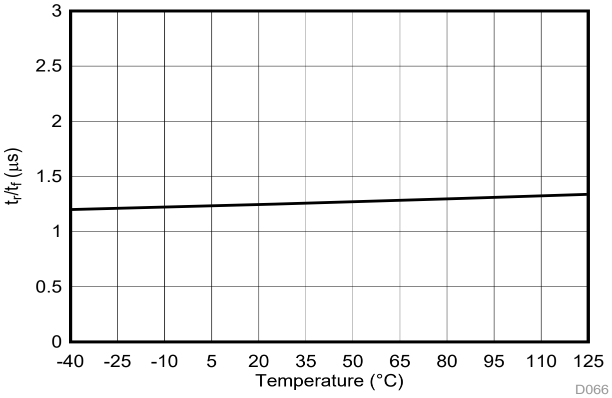


Figure 6-41. Output Rise and Fall Time vs Temperature

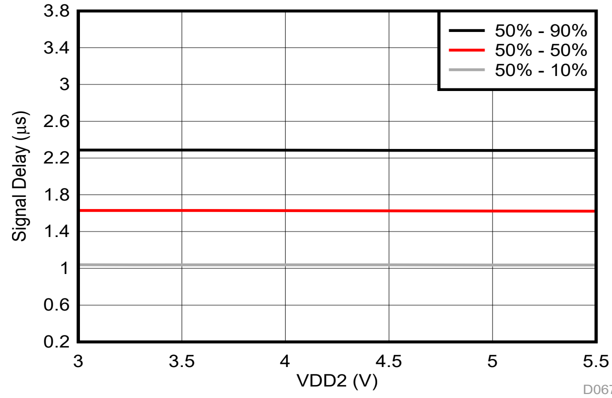


Figure 6-42. Input to Output Signal Delay vs Supply Voltage

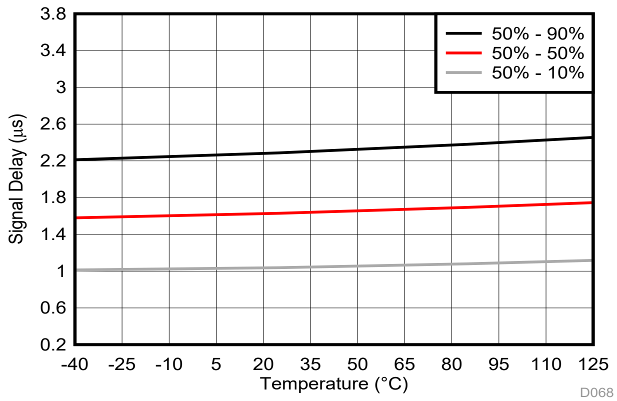


Figure 6-43. Input to Output Signal Delay vs Temperature

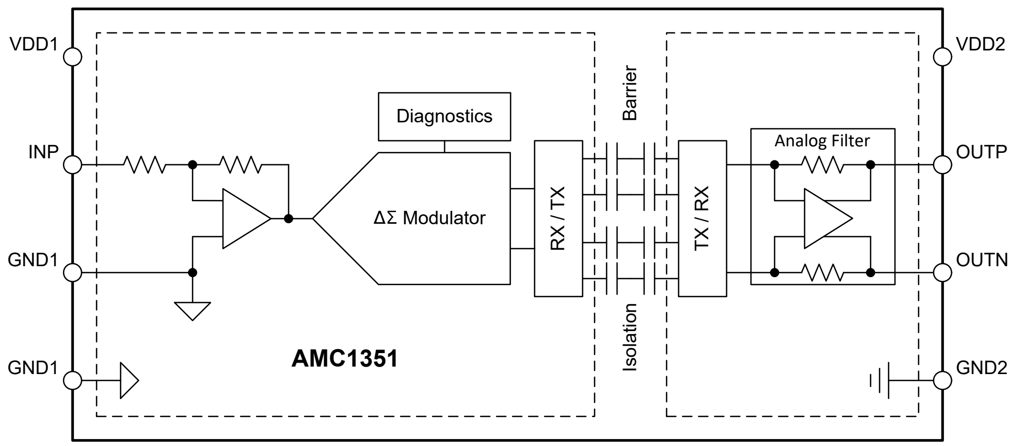
7 Detailed Description

7.1 Overview

The AMC1351 is a single-ended input, precision, isolated amplifier with a high input-impedance and wide input-voltage range. The input stage of the device drives a second-order, delta-sigma (ΔΣ) modulator. The modulator converts the analog input signal into a digital bitstream that is transferred across the isolation barrier that separates the high-side from the low-side. On the low-side, the received bitstream is processed by a fourth-order analog filter that outputs a differential signal at the OUTP and OUTN pins proportional to the input signal.

The SiO_2-based, capacitive isolation barrier supports a high level of magnetic field immunity, as described in the *ISO72x Digital Isolator Magnetic-Field Immunity* application report. The digital modulation used in the AMC1351 to transmit data across the isolation barrier, and the isolation barrier characteristics itself, result in high reliability and common-mode transient immunity.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Input

The single-ended, high-impedance input stage of the AMC1351 feeds a second-order, switched-capacitor, feed-forward ΔΣ modulator. The modulator converts the analog signal into a bitstream that is transferred across the isolation barrier, as described in the *Isolation Channel Signal Transmission* section.

There are two restrictions on the analog input signal IN. First, if the input voltage V_{IN} exceeds the range specified in the *Absolute Maximum Ratings* table, the input current must be limited to the absolute maximum value because the electrostatic discharge (ESD) protection turns on. In addition, the linearity and parametric performance of the device is ensured only when the analog input voltage remains within the linear full-scale range (V_{FSR}) as specified in the *Recommended Operating Conditions* table.

7.3.2 Isolation Channel Signal Transmission

The AMC1351 uses an on-off keying (OOK) modulation scheme, as shown in Figure 7-1, to transmit the modulator output bitstream across the SiO_2-based isolation barrier. The transmit driver (TX) shown in the *Functional Block Diagram* transmits an internally-generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC1351 is 480 MHz.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and provides the input to the fourth-order analog filter. The AMC1351 transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and lowest level of radiated emissions caused by the high-frequency carrier and RX, TX buffer switching.

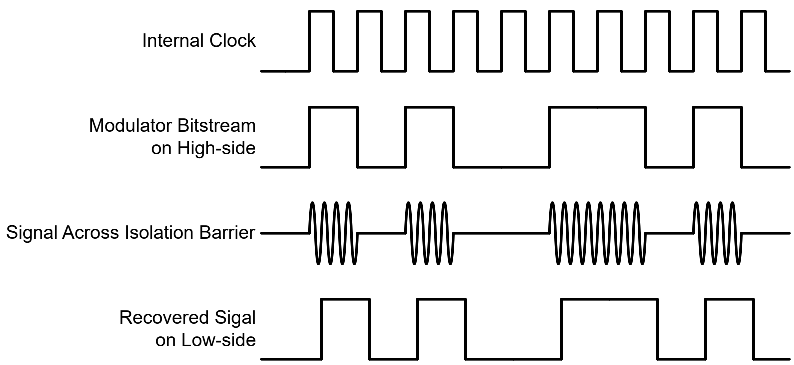


Figure 7-1. OOK-Based Modulation Scheme

7.3.3 Analog Output

The AMC1351 provides a differential analog output on the OUTP and OUTN pins. For input voltages (V_{IN}) in the range from –0.25 V to 5 V, the device provides a linear response with a nominal gain of 0.4 V/V. For example, for an input voltage of 5 V, the differential output voltage (V_{OUTP} – V_{OUTN}) is 2 V. At zero input (IN shorted to GND1), both pins output the same common-mode output voltage V_{CMout}, as specified in the *Electrical Characteristics* table. For input voltages greater than 5 V but less than approximately 6.25 V, the differential output voltage continues to increase but with reduced linearity performance. The outputs saturate at a differential output voltage of $V_{CLIPout}$, as shown in Figure 7-2, if the input voltage exceeds the $V_{Clipping}$ value.

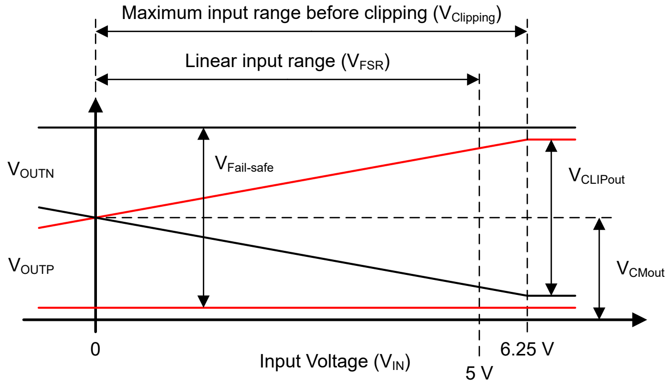


Figure 7-2. Output Behavior of the AMC1351

The AMC1351 output offers a fail-safe feature that simplifies diagnostics on a system level. Figure 7-2 shows the behavior in fail-safe mode, in which the AMC1351 outputs a negative differential output voltage that does not occur under normal operating conditions. The fail-safe output is active:

- When the high-side supply VDD1 of the AMC1351 device is missing
- When the high-side supply VDD1 falls below the undervoltage threshold $VDD1_{UV}$

Use the maximum $V_{Fail-safe}$ voltage specified in the *Electrical Characteristics* table as a reference value for fail-safe detection on a system level.

7.4 Device Functional Modes

The AMC1351 is operational when the power supplies VDD1 and VDD2 are applied as specified in the *Recommended Operating Conditions* table.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The high input impedance, low input bias current, excellent accuracy, and low temperature drift make the AMC1351 a high-performance solution for industrial applications where voltage sensing in the presence of high common-mode voltage levels is required.

8.2 Typical Application

Isolated amplifiers are widely used for voltage measurements in high-voltage applications that must be isolated from a low-voltage domain. A typical application is the sensing of the DC bus voltage in a frequency inverter.

With its wide, 5-V input voltage range, the AMC1351 is designed for isolated DC voltage-sensing applications where accurate voltage monitoring is required in high-noise environments.

Figure 8-1 shows a simplified schematic of the AMC1351 in a typical motor drive application. The DC bus voltage is divided down to an approximate 5-V level across the bottom resistor (RSNS) of a high-impedance resistor divider that is sensed by the AMC1351. The AMC1351 digitizes the analog input signal on the high-side, transfers the data across the isolation barrier to the low-side, and reconstructs an analog signal that is presented as a differential voltage on the output pins.

The high-impedance input and the high common-mode transient immunity (CMTI) of the AMC1351 ensure reliable and accurate operation even in high-noise environments.

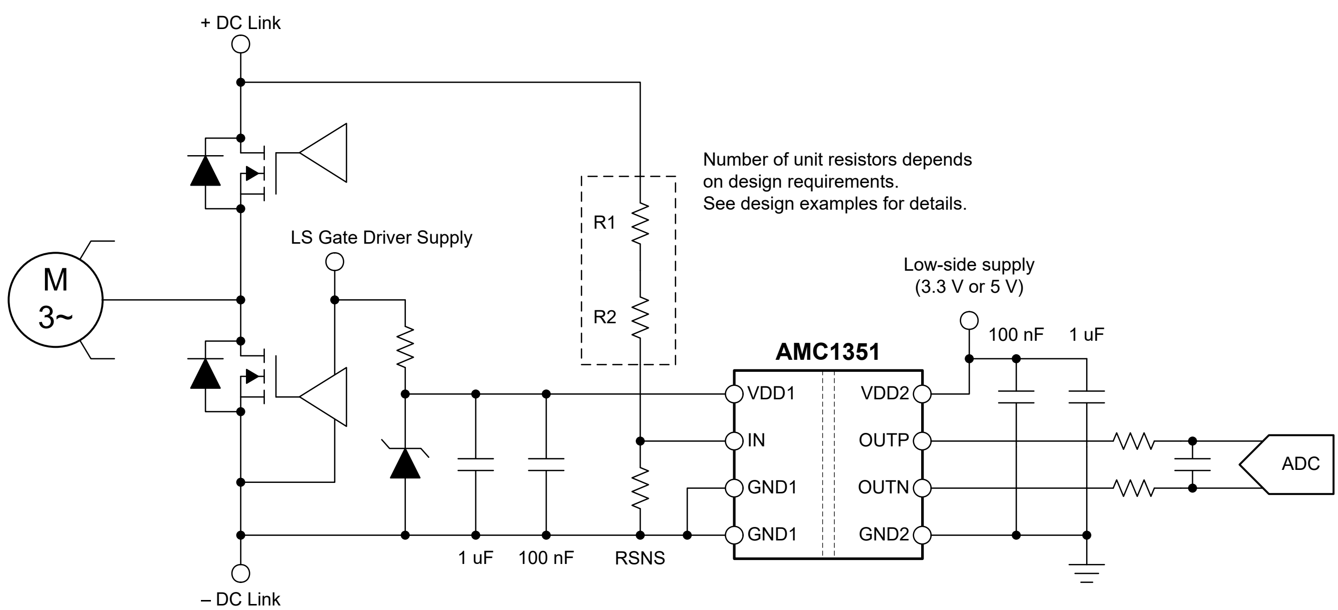


Figure 8-1. Using the AMC1351 for DC Link Voltage Sensing in Frequency Inverters

8.2.1 Design Requirements

Table 8-1 lists the parameters for this typical application.

Table 8-1. Design Requirements

PARAMETER	190-V_{DC} LINE VOLTAGE	360-V_{DC} LINE VOLTAGE
System input voltage	120 V_{RMS} ±10%, 60 Hz	230 V_{RMS} ±10%, 50 Hz
DC bus voltage (max)	190 V	360 V
High-side supply voltage	3.3 V or 5 V	3.3 V or 5 V
Low-side supply voltage	3.3 V or 5 V	3.3 V or 5 V
Maximum resistor operating voltage	75 V	75 V
Voltage drop across the sense resistor (RSNS) for a linear response	5 V (maximum)	5 V (maximum)
Current through the resistive divider (I_{CROSS})	100 µA	100 µA

8.2.2 Detailed Design Procedure

This discussion covers the 360-V_{DC} example. The procedure for calculating the resistive divider for the 190-V_{DC} use case is identical.

The 100-µA, cross-current requirement at peak input voltage (360 V) determines that the total impedance of the resistive divider is 3.6 MΩ. The impedance of the resistive divider is dominated by the top resistors (shown exemplary as R1 and R2 in Figure 8-1) and the voltage drop across RSNS can be neglected for a short time. The maximum allowed voltage drop per unit resistor is specified as 75 V; therefore, the total minimum number of unit resistors in the top portion of the resistive divider is 360 V / 75 V = 5. The calculated unit value is 3.6 MΩ / 5 = 720 kΩ and the next closest value from the E96 series is 715 kΩ.

The *effective* sense resistor value $RSNS_{EFF}$ is the parallel combination of the external resistor RSNS and the input impedance of the AMC1351, R_{IN}. $RSNS_{EFF}$ is sized such that the voltage drop across the impedance at maximum input voltage (360 V) equals the linear full-scale input voltage (V_{FSR}) of the AMC1351 (that is, 5 V). $RSNS_{EFF}$ is calculated as $RSNS_{EFF} = V_{FSR} / (V_{Peak} – V_{FSR}) \times R_{TOP}$, where R_{TOP} is the total value of top resistor string (5 × 715 kΩ = 3575 kΩ). The resulting value for $RSNS_{EFF}$ is 9.96 kΩ. In a final step, RSNS is calculated as $RSNS = R_{IN} \times RSNS_{EFF} / (R_{IN} – RSNS_{EFF})$. With R_{IN} = 1.25 MΩ (typical), RSNS equals 52.47 kΩ and the next closest value from the E96 series is 52.3 kΩ.

Table 8-2 summarizes the design of the resistive divider.

Table 8-2. Resistor Value Examples

PARAMETER	190-V_{DC} LINE VOLTAGE	360-V_{DC} LINE VOLTAGE
Unit resistor value (R_{TOP})	634 kΩ	715 kΩ
Number of unit resistors in R_{TOP}	3	5
Sense resistor value (RSNS)	51.1 kΩ	49.9 kΩ
Total resistance value (R_{TOP} + RSNS)	1953.1 kΩ	3624.9 kΩ
Resulting current through resistive divider (I_{CROSS})	97.3 µA	99.3 µA
Resulting full-scale voltage drop across sense resistor RSNS	4.971 V	4.956 V
Peak power dissipated in R_{TOP} unit resistors	6 mW	7.1 mW
Total peak power dissipated in resistive divider	18.5 mW	35.8 mW

8.2.2.1 Input Filter Design

Placing an RC filter in front of the isolated amplifier improves signal-to-noise performance of the signal path. In practice, however, the impedance of the resistor divider is so high that adding a filter capacitor on the IN pin limits the signal bandwidth to an unacceptable low limit, such that the filter capacitor is omitted. When used, design the input filter such that:

- The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency (20 MHz) of the internal ΔΣ modulator
- The input bias current does not generate significant voltage drop across the DC impedance of the input filter

Most voltage-sensing applications use high-impedance resistor dividers in front of the isolated amplifier to scale down the input voltage. In that case, no additional resistor is needed and a single capacitor (as shown in Figure 8-2) is sufficient to filter the input signal.

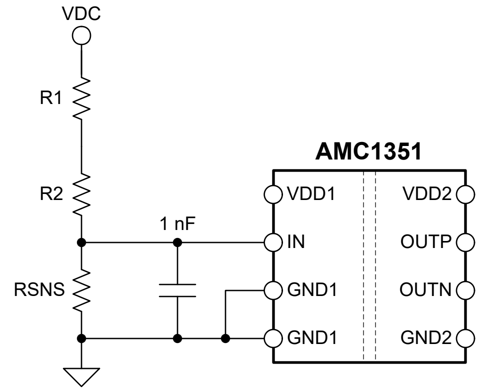


Figure 8-2. Input Filter

8.2.2.2 Differential to Single-Ended Output Conversion

Figure 8-3 shows an example of a TLV6001-based signal conversion and filter circuit for systems using single-ended input ADCs to convert the analog output voltage into digital. With R1 = R2 = R3 = R4, the output voltage equals (V_{OUTP} – V_{OUTN}) + V_{REF}. Tailor the bandwidth of this filter stage to the bandwidth requirement of the system and use NP0-type capacitors for best performance. For most applications, R1 = R2 = R3 = R4 = 3.3 kΩ and C1 = C2 = 330 pF yields good performance.

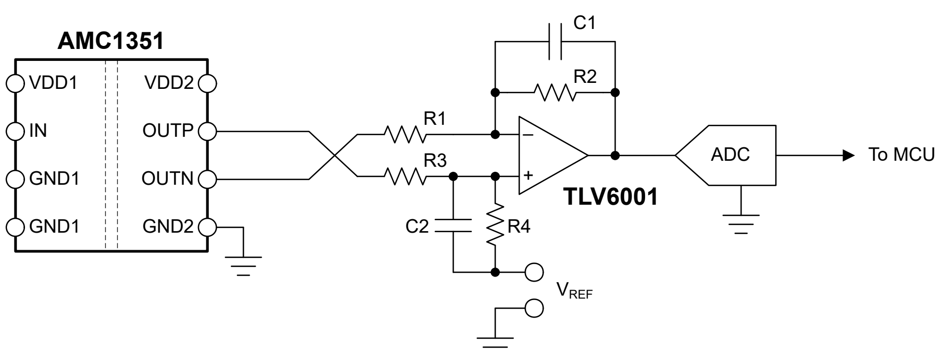


Figure 8-3. Connecting the AMC1351 Output to a Single-Ended Input ADC

For more information on the general procedure to design the filtering and driving stages of SAR ADCs, see the *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* and *18-Bit Data Acquisition Block (DAQ) Optimized for Lowest Power* reference guides, available for download at www.ti.com.

8.2.3 Application Curve

One important aspect of system design is the effective detection of an overvoltage condition to protect switching devices and passive components from damage. To power off the system quickly in the event of an overvoltage condition, a low delay caused by the isolated amplifier is required. Figure 8-4 shows the typical full-scale step response of the AMC1351.

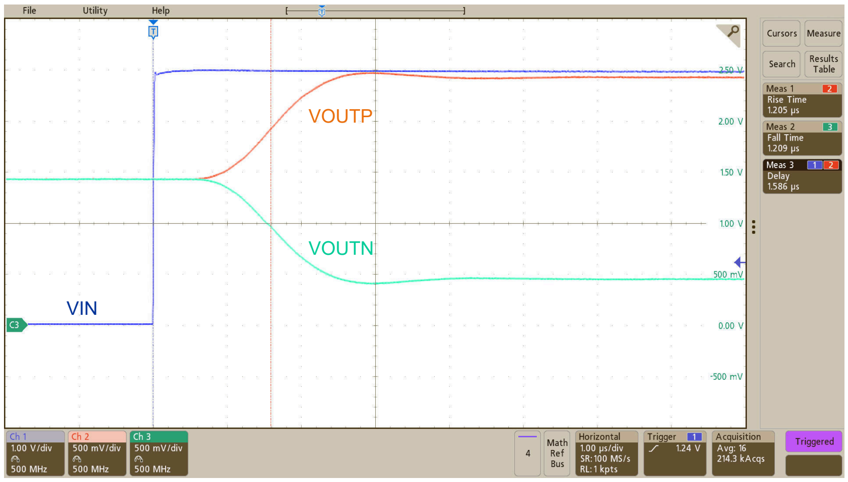


Figure 8-4. Step Response of the AMC1351

8.3 What To Do and What Not To Do

Do not leave the analog input (IN) of the AMC1351 unconnected (floating) when the device is powered up on the high-side. If the device input is left floating, the bias current may generate a positive or negative input voltage and the output of the device is undetermined.

Do not connect protection diodes to the input (IN) of the AMC1351. Diode leakage current can introduce significant measurement error especially at high temperatures. The input pin is protected against high voltages by its ESD protection circuit and the high impedance of the external restive divider

Connect both GND1 pins to the high-side ground potential. Do not leave one of the GND1 pins unconnected.

9 Power Supply Recommendations

In a typical application, the high-side power supply (VDD1) for the AMC1351 is generated either from a gate-driver supply on the high-side (as shown in Figure 8-1), or from the low-side supply (VDD2) by an isolated DC/DC converter. A low-cost solution is based on the push-pull driver SN6501 and a transformer that supports the desired isolation voltage ratings.

The AMC1351 does not require any specific power-up sequencing. The high-side power supply (VDD1) is decoupled with a low-ESR, 100-nF capacitor (C1) parallel to a low-ESR, 1-µF capacitor (C2). The low-side power supply (VDD2) is equally decoupled with a low-ESR, 100-nF capacitor (C3) parallel to a low-ESR, 1-µF capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible.

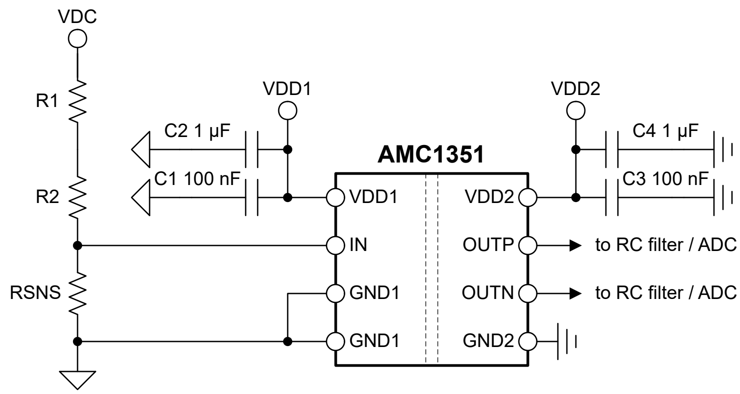


Figure 9-1. Decoupling of the AMC1351

Capacitors must provide adequate effective capacitance under the applicable DC bias conditions they experience in the application. Multilayer ceramic capacitors (MLCC) typically exhibit only a fraction of their nominal capacitance under real-world conditions and this factor must be taken into consideration when selecting these capacitors. This problem is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

10 Layout

10.1 Layout Guidelines

Figure 10-1 shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC1351 supply pins) and placement of the other components required by the device. For best performance, place the sense resistor close to the device input pin (IN).

10.2 Layout Example

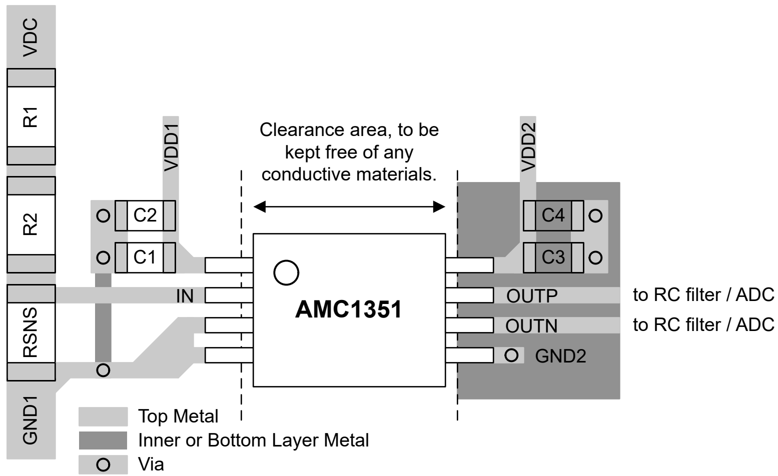


Figure 10-1. Recommended Layout of the AMC1351

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Isolation Glossary* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application report
- Texas Instruments, *TLV600x Low-Power, Rail-to-Rail In/Out, 1-MHz Operational Amplifier for Cost-Sensitive Systems* data sheet
- Texas Instruments, *18-Bit, 1-MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* reference guide
- Texas Instruments, *18-Bit, 1-MSPS Data Acquisition Block (DAQ) Optimized for Lowest Power* reference guide
- Texas Instruments, *Isolated Amplifier Voltage Sensing Excel Calculator* design tool
- Texas Instruments, *Best in Class Radiated Emissions EMI Performance with the AMC1300B-Q1 Isolated Amplifier* technical white paper

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC1351DWV	ACTIVE	SOIC	DWV	8	64	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1351	Samples
AMC1351DWVR	ACTIVE	SOIC	DWV	8	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1351	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

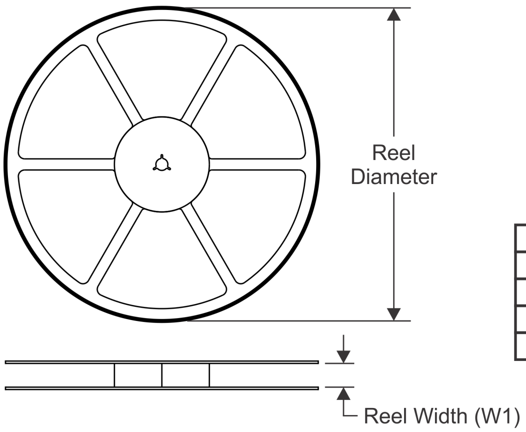
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

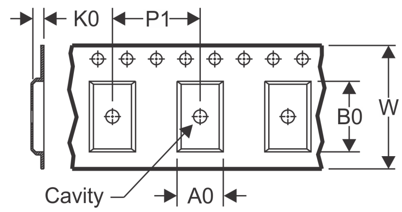
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

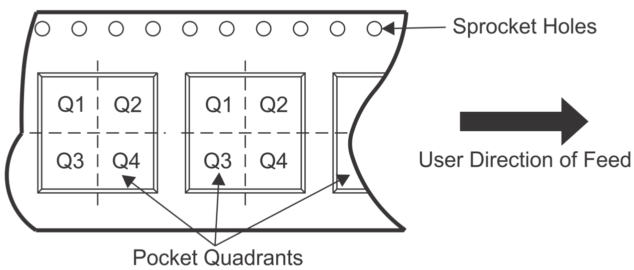


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

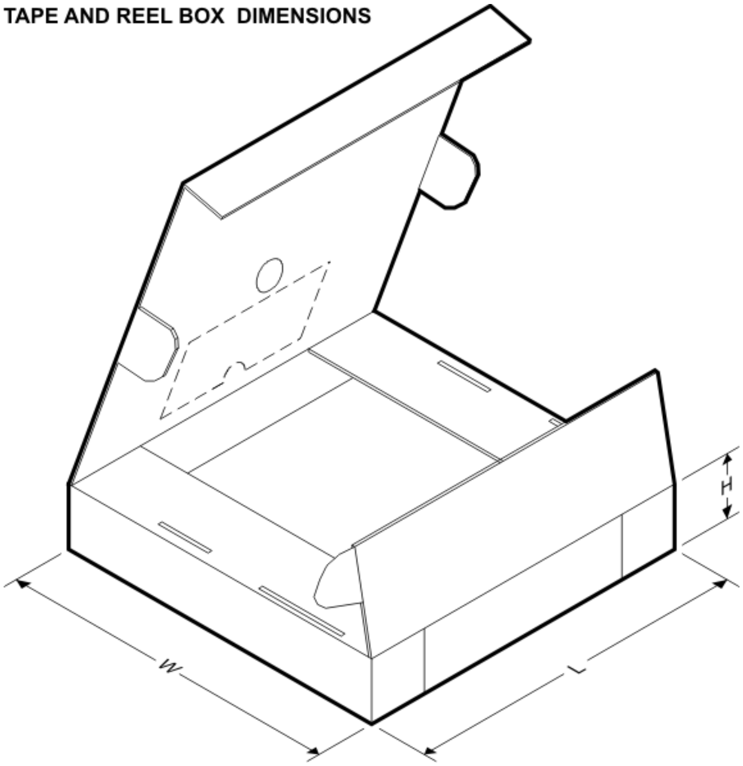
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

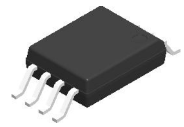
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1351DWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

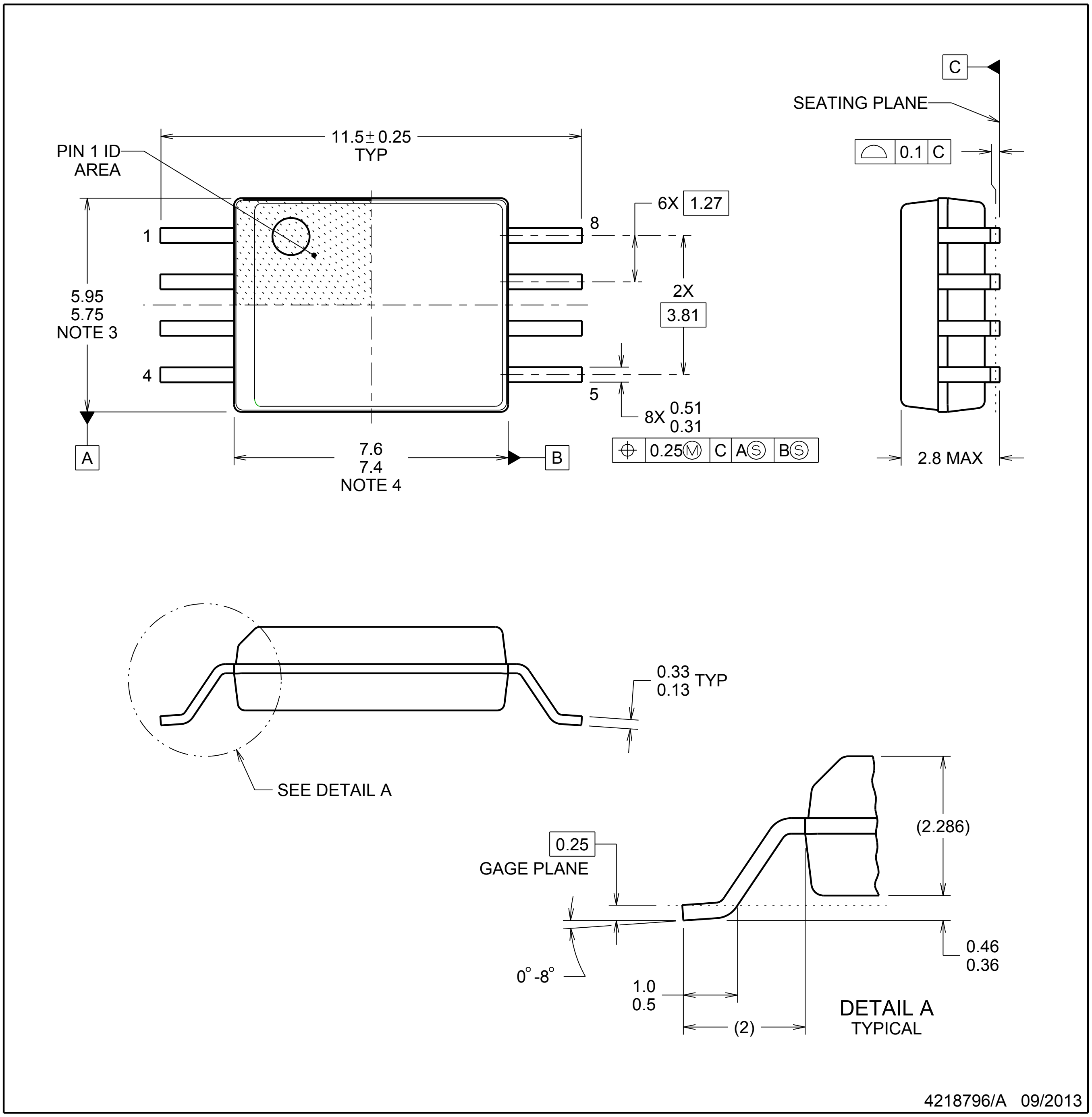
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1351DWVR	SOIC	DWV	8	1000	350.0	350.0	43.0



DWV0008A

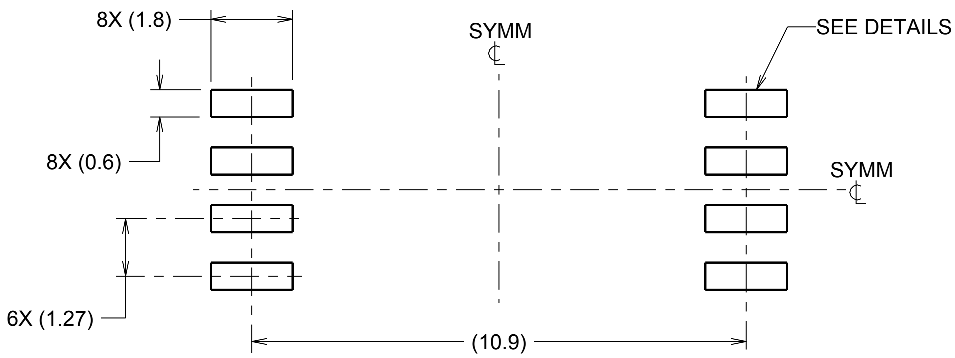
SOIC - 2.8 mm max height

SOIC

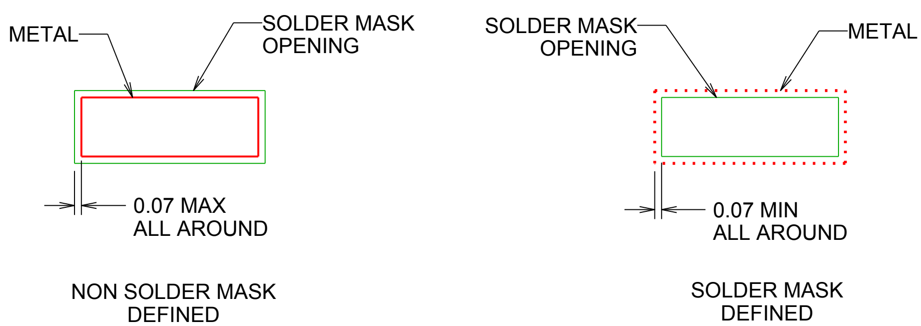


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



SOLDER MASK DETAILS

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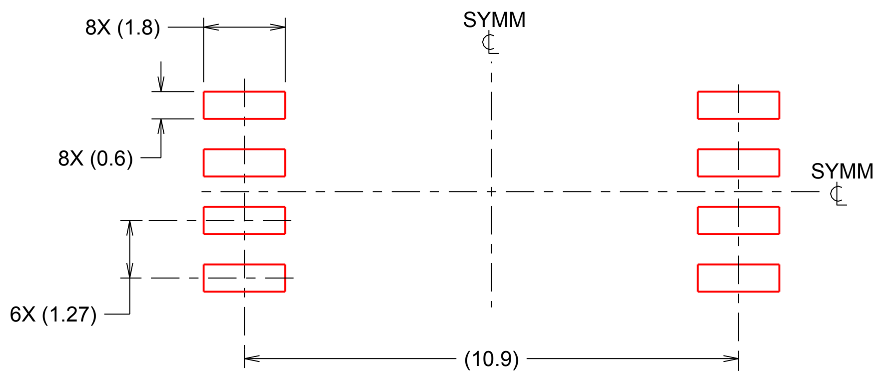
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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