

## Octal channel high side driver

### Features

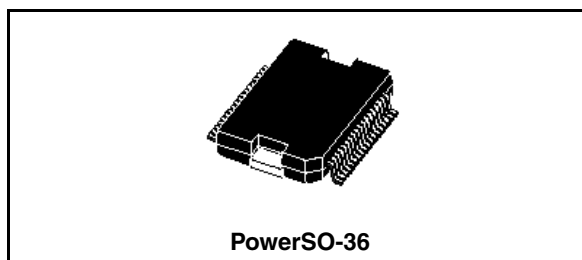
Type	$R_{DS(on)}^{(1)}$	$I_{out}^{(1)}$	$V_{CC}$
VN808-E	150 mΩ	0.7 A	45 V

1. Per channel

- $V_{CC}/2$  compatible input
- Junction over-temperature protection
- Case over-temperature protection for thermal independence of the channels
- Current limitation
- Shorted load protection
- Undervoltage shut-down
- Protection against loss of ground
- Very low stand-by current
- Compliance to 61000-4-4 IEC test up to 4 kV

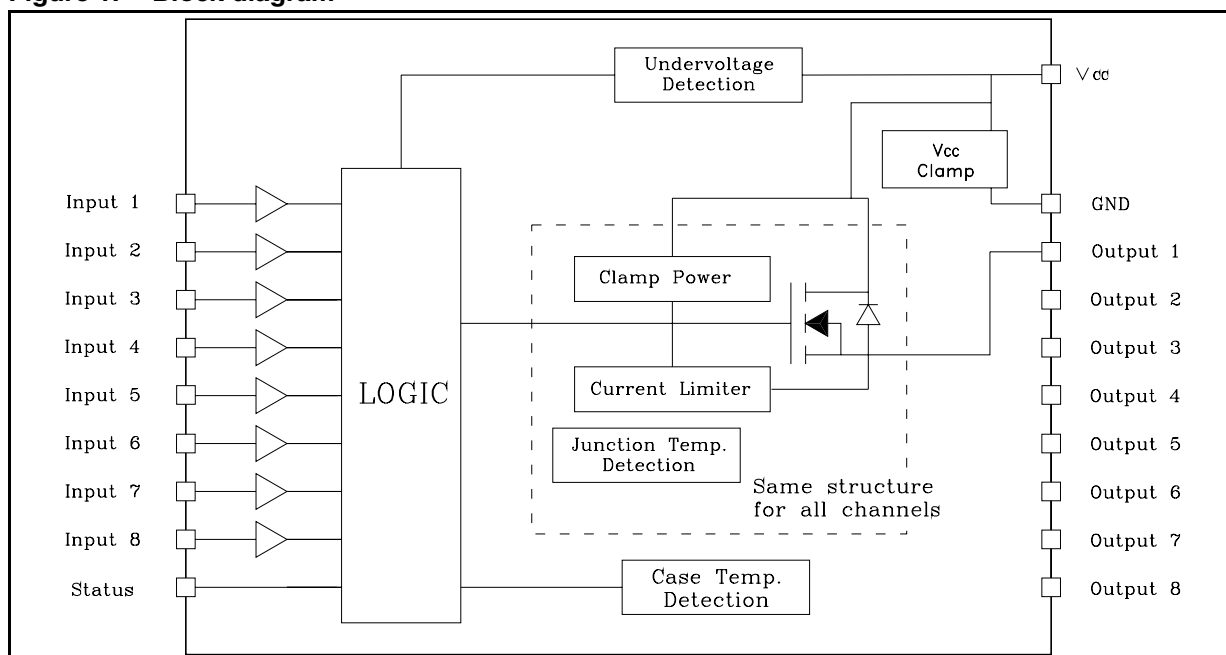
### Description

The VN808-E is a monolithic device designed in STMicroelectronics VIPower M0-3 technology, intended for driving any kind of load with one side connected to ground.



Active current limitation combined with thermal shutdown and automatic restart, protect the device against overload. In overload condition, channel turns OFF and back ON automatically so as to maintain junction temperature between  $T_{TSD}$  and  $T_R$ . If this condition makes case temperature reach  $T_{CSD}$ , overloaded channel is turned OFF and will restart only when case temperature has decreased down to  $T_{CR}$  (see waveform 3 [Figure 8 on page 11](#)). Non overloaded channels continue to operate normally. Device automatically turns OFF in case of ground pin disconnection. This device is especially suitable for industrial applications conform to IEC 61131

**Figure 1. Block diagram**



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# 1 Maximum ratings

**Table 1. Absolute maximum rating**

Symbol	Parameter	Value	Unit
$V_{CC}$	DC supply voltage	45	V
$-I_{GND}$	DC ground pin reverse current TRAN ground pin reverse current (pulse duration < 1ms)	-250 -6	mA A
$I_{OUT}$	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	-2	A
$I_{IN}$	DC input current	$\pm 10$	mA
$V_{IN}$	Input voltage range	$-3/+V_{CC}$	V
$V_{ESD}$	Electrostatic discharge (R = 1.5 k $\Omega$ ; C = 100 pF)	2000	V
$P_{TOT}$	Power dissipation at $T_C = 25\text{ }^\circ\text{C}$	96	W
$L_{MAX}$	Max inductive load ( $V_{CC} = 24\text{ V}$ , $R_{LOAD} = 48\text{ }\Omega$ , $T_A = 100\text{ }^\circ\text{C}$ )	2	H
$T_J$	Junction operating temperature	Internally limited	$^\circ\text{C}$
$T_C$	Case operating temperature	Internally limited	$^\circ\text{C}$
$T_{STG}$	Storage temperature	-40 to 150	$^\circ\text{C}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance junction-case	Max 1.3	$^\circ\text{C}/\text{W}$
$R_{thJA}$	Thermal resistance junction-ambient <sup>(1)</sup>	Max 50	$^\circ\text{C}/\text{W}$

1. When mounted on FR4 printed circuit board with 0.5 cm<sup>2</sup> of copper area (at least 35  $\mu\text{m}$  thick) connected to all TAB pins.

## 2 Electrical characteristics

(10.5 V < V<sub>CC</sub> < 32 V; -40 °C < T<sub>J</sub> < 125 °C; unless otherwise specified)

**Table 3. Power section**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	Operating supply voltage		10.5		45	V
V <sub>USD</sub>	Undervoltage shutdown		7		10.5	V
R <sub>ON</sub>	On state resistance	I <sub>OUT</sub> = 0.5 A; T <sub>J</sub> = 25 °C I <sub>OUT</sub> = 0.5 A;		150	185 280	mΩ mΩ
I <sub>S</sub>	Supply current	OFF state; V <sub>CC</sub> = 24 V; T <sub>CASE</sub> = 25 °C ON state (all channels ON); V <sub>CC</sub> = 24 V, T <sub>CASE</sub> = 100 °C			150 12	μA mA
I <sub>LGND</sub>	Output current at turn-off	V <sub>CC</sub> = V <sub>STAT</sub> = V <sub>IN</sub> = V <sub>GND</sub> = 24 V V <sub>OUT</sub> = 0 V			1	mA
I <sub>L(off)</sub>	OFF state output current	V <sub>IN</sub> = V <sub>OUT</sub> = 0 V;	0		5	μA
V <sub>OUT(off)</sub>	OFF state output voltage	V <sub>IN</sub> = 0 V, I <sub>OUT</sub> = 0 A			3	V
t <sub>d(Vccon)</sub>	Power-on delay time from V <sub>CC</sub> rising edge	<i>Figure 7 on page 10</i>		1		ms

**Table 4. Switching (V<sub>CC</sub> = 24 V)**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t <sub>ON</sub>	Turn-on time	R <sub>L</sub> = 48 Ω from 80 % V <sub>OUT</sub> <i>Figure 6.</i>		50	100	μs
t <sub>OFF</sub>	Turn-off time	R <sub>L</sub> = 48 Ω to 10 % V <sub>OUT</sub> <i>Figure 6.</i>		75	150	μs
dV <sub>OUT</sub> /dt <sub>(on)</sub>	Turn-on voltage slope	R <sub>L</sub> = 48 Ω from V <sub>OUT</sub> = 2.4 V to V <sub>OUT</sub> = 19.2 V <i>Figure 6.</i>		0.7		V/μs
dV <sub>OUT</sub> /dt <sub>(off)</sub>	Turn-off voltage slope	R <sub>L</sub> = 48 Ω from V <sub>OUT</sub> = 21.6 V to V <sub>OUT</sub> = 2.4 V <i>Figure 6.</i>		1.5		V/μs

Table 5. Input pin

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{INL}$	Input low level				$V_{CC}/2-1$	V
$I_{INL}$	Low level input current	$V_{IN} = V_{CC}/2 - 1$ V	80			$\mu$ A
$V_{INH}$	Input high level		$V_{CC}/2+1$			V
$I_{INH}$	High level input current	$V_{IN} = V_{CC}/2 + 1$ V		150	260	$\mu$ A
$V_{I(HYST)}$	Input hysteresis voltage			0.6		V
$I_{IN}$	Input current	$V_{IN} = V_{CC} = 32$ V			300	$\mu$ A

Table 6. Protections

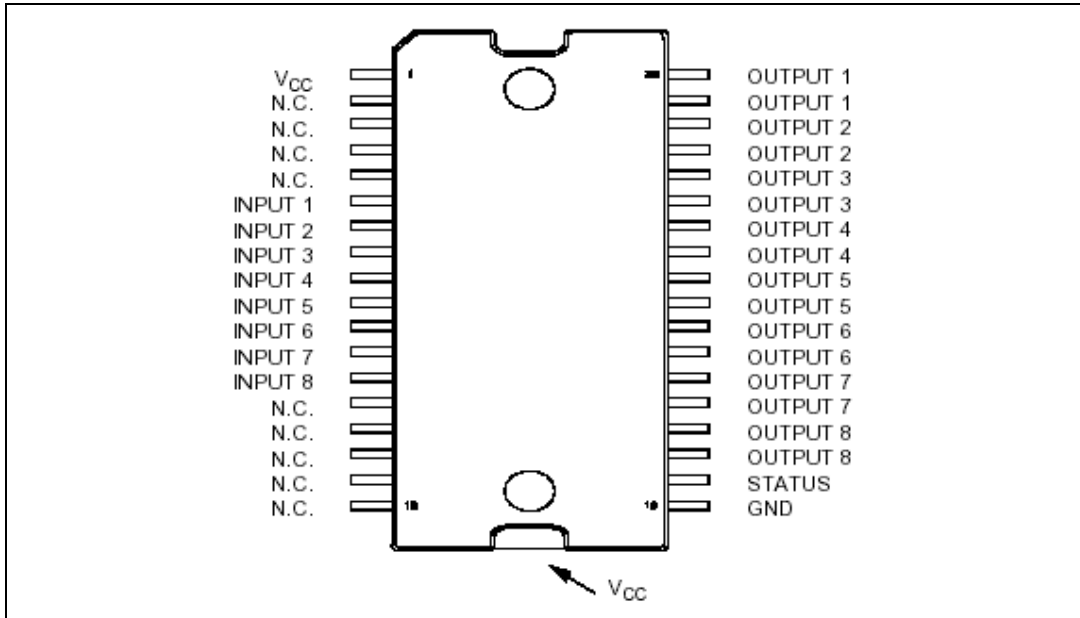
Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$T_{CSD}$	Case shut-down temperature		125	130	135	$^{\circ}$ C
$T_{CR}$	Case reset temperature		110			$^{\circ}$ C
$T_{CHYST}$	Case thermal hysteresis		7	15		$^{\circ}$ C
$T_{TSD}$	Junction shutdown temperature		150	175	200	$^{\circ}$ C
$T_R$	Junction reset temperature		135			$^{\circ}$ C
$T_{HYST}$	Junction thermal hysteresis		7	15		$^{\circ}$ C
$I_{lim}$	DC short circuit current per channel	$V_{CC} = 24$ V; $R_{LOAD} = 10$ m $\Omega$	0.7		1.7	A
$V_{demag}$	Turn-off output clamp voltage	$I_{OUT} = 0.5$ A; $L = 6$ mH	$V_{CC}-57$	$V_{CC}-52$	$V_{CC}-47$	V

Table 7. Status pin

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$I_{HSTAT}$	High level output current	$V_{CC} = 18...32$ V; $R_{STAT} = 1$ k $\Omega$ (Fault condition)	2	3	4	mA
$I_{LSTAT}$	Leakage current	Normal operation; $V_{CC} = 32$ V			0.1	$\mu$ A
$V_{CLSTAT}$	Clamp voltage	$I_{STAT} = 1$ mA $I_{STAT} = -1$ mA	6.0	6.8 -0.7	8.0	V V

### 3 Pin connections

Figure 2. Connection diagram (top view)



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Table 8. Pin functions

Pin N°	Symbol	Function
TAB	V <sub>CC</sub>	Positive power supply voltage
1	V <sub>CC</sub>	Positive power supply voltage
2,3,4,5	NC	Not connected
6	Input 1	Input of channel 1
7	Input 2	Input of channel 2
8	Input 3	Input of channel 3
9	Input 4	Input of channel 4
10	Input 5	Input of channel 5
11	Input 6	Input of channel 6
12	Input 7	Input of channel 7
13	Input 8	Input of channel 8
14,15,16,17,18	NC	Not connected
19	GND	Logic ground
20	STATUS	Common open source diagnostic for over-temperature
21,22	Output 8	High-side output of channel 8
23,24	Output 7	High-side output of channel 7

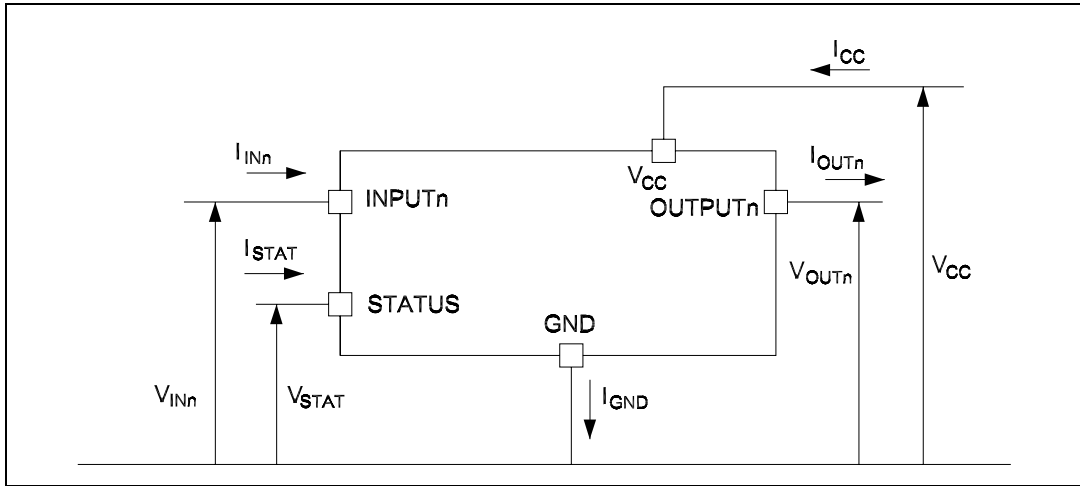
**Table 8. Pin functions (continued)**

Pin N°	Symbol	Function
25, 26	Output 6	High-side output of channel 6
27, 28	Output 5	High-side output of channel 5
29, 30	Output 4	High-side output of channel 4
31, 32	Output 3	High-side output of channel 3
33, 34	Output 2	High-side output of channel 2
35, 36	Output 1	High-side output of channel 1

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# 4 Current, voltage conventions and internal diagram

Figure 3. Current and voltage conventions



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Figure 4. Equivalent internal block diagram (same structure for all channel)

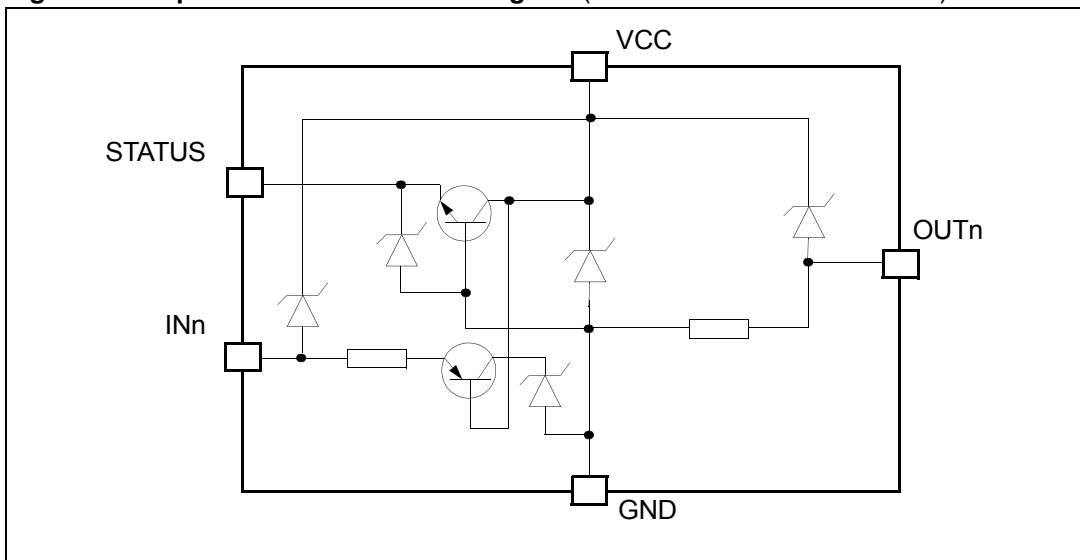




Figure 5. Application example

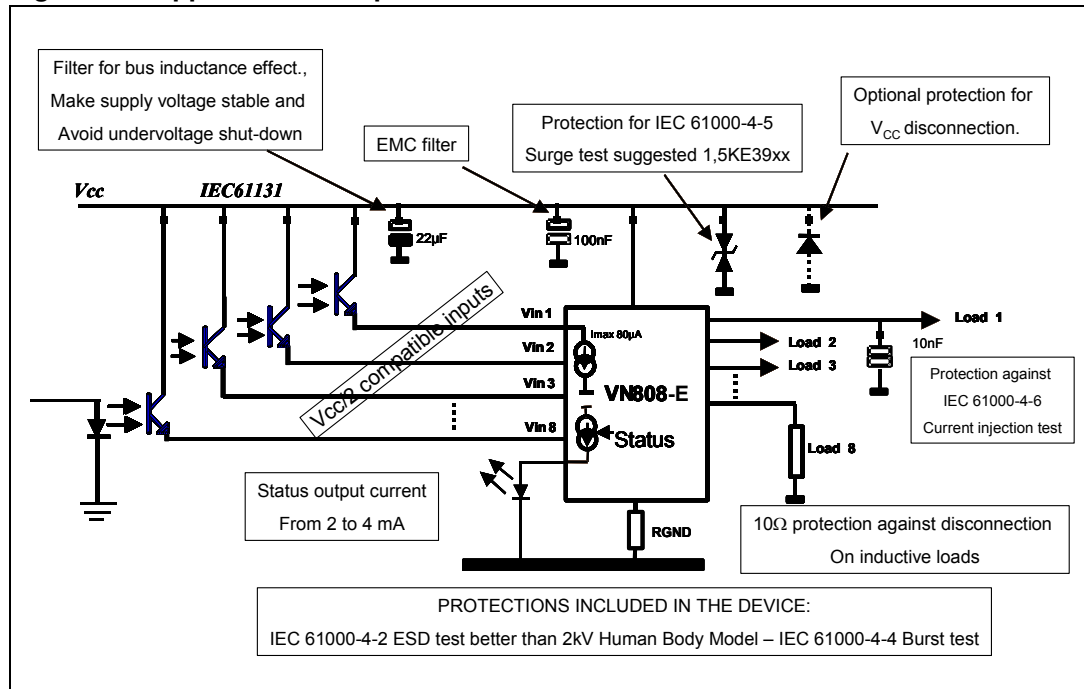
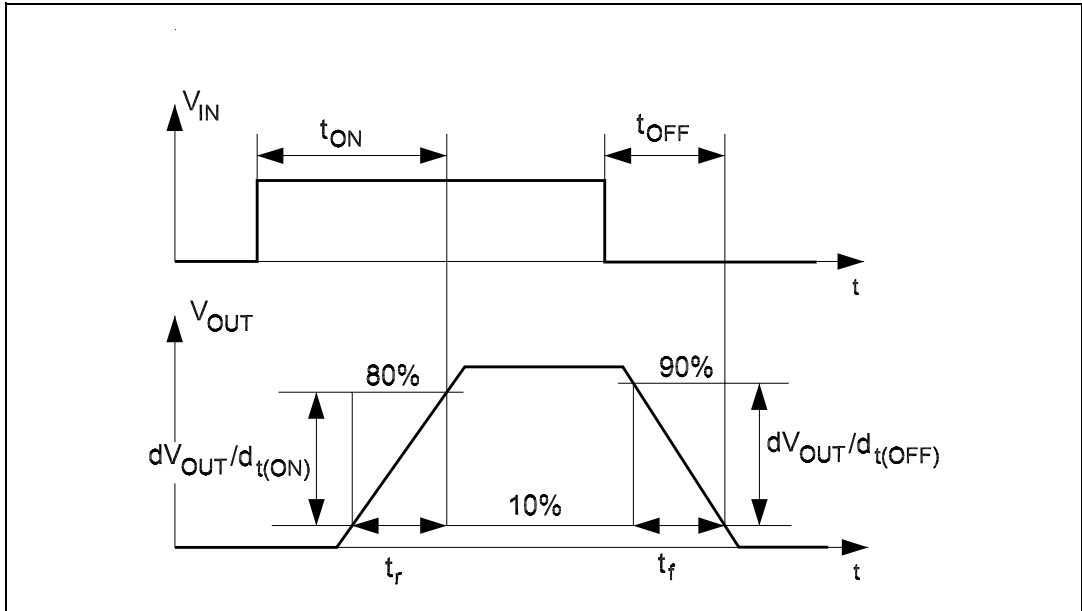


Table 9. Truth table

Conditions	INPUTn	OUTPUTn	STATUS
Normal operation	L	L	L
	H	H	L
Current limitation	L	L	L
	H	X	L
Overtemperature (see waveforms 3, 4 <a href="#">Figure 8</a> ) -> T <sub>J</sub> > T <sub>TSD</sub>	L	L	L
	H	L	H
Undervoltage	L	L	X
	H	L	X

# 5 Switching time waveforms

Figure 6. Turn-ON and turn-OFF



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Figure 7.  $V_{CC}$  turn-ON

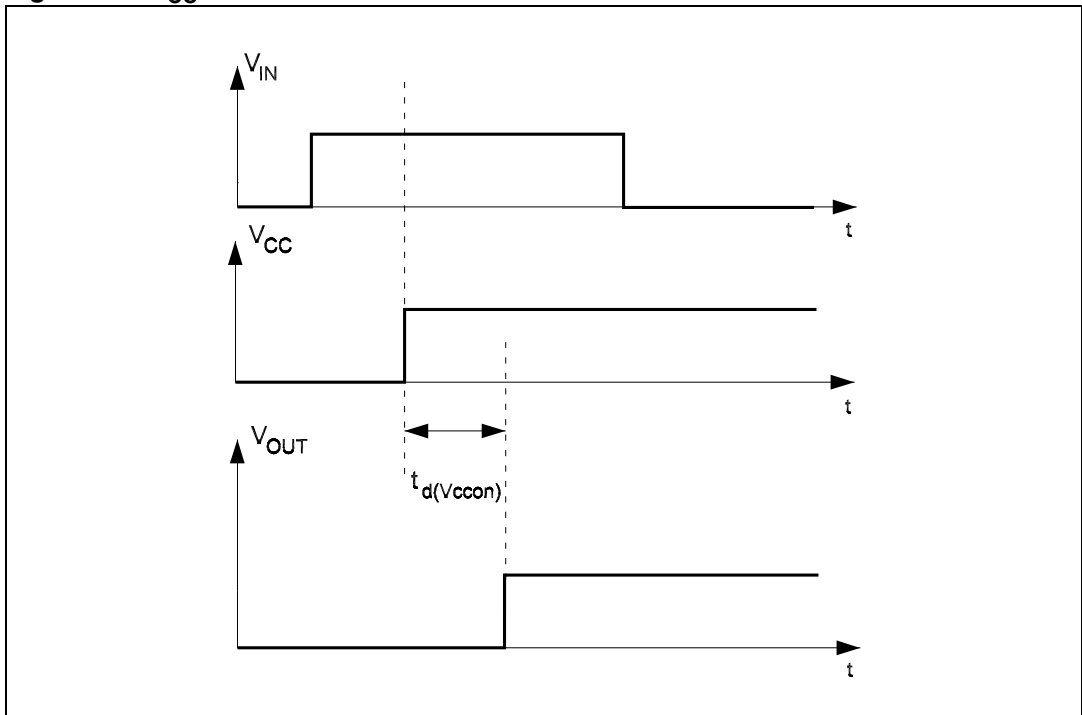
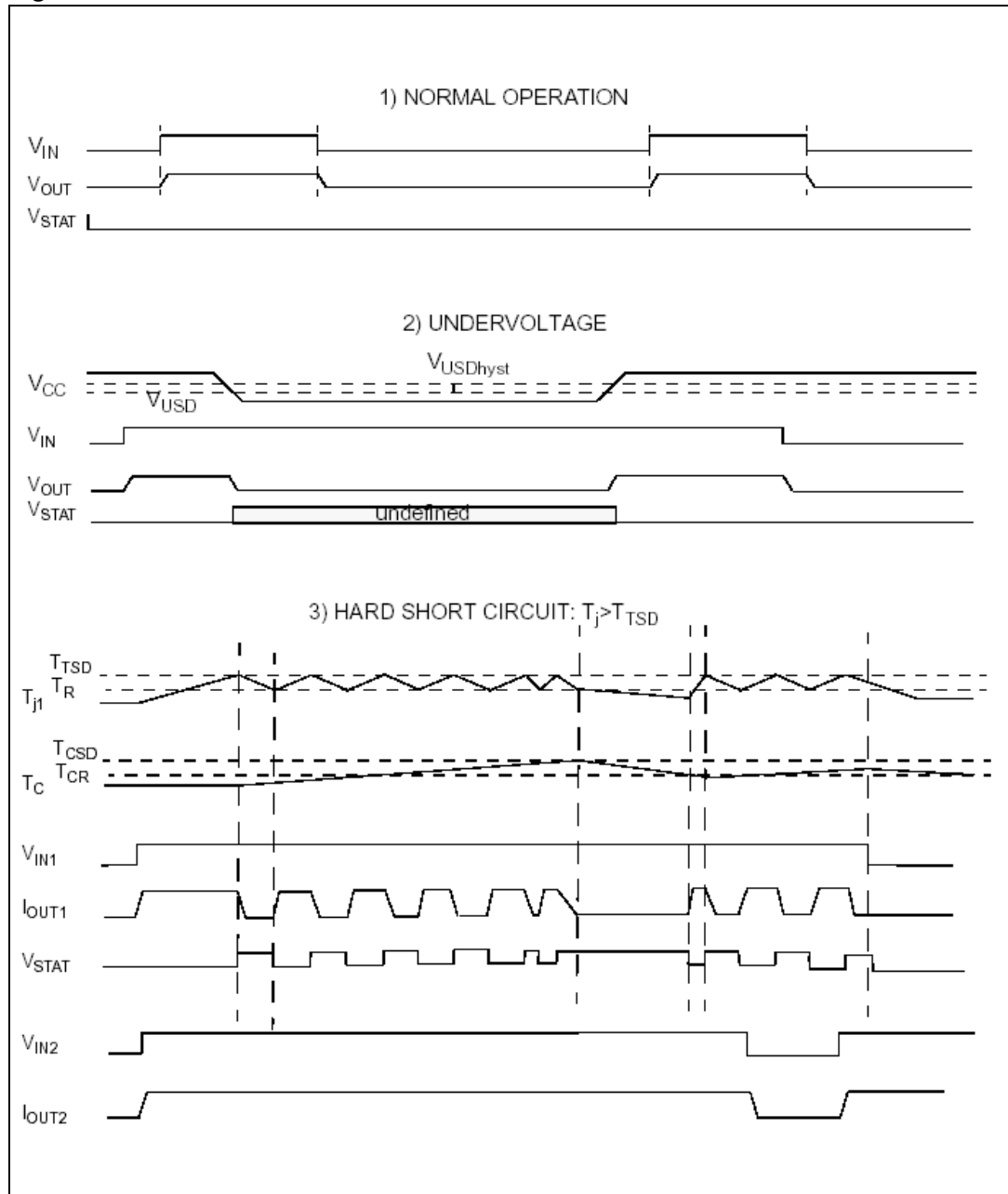
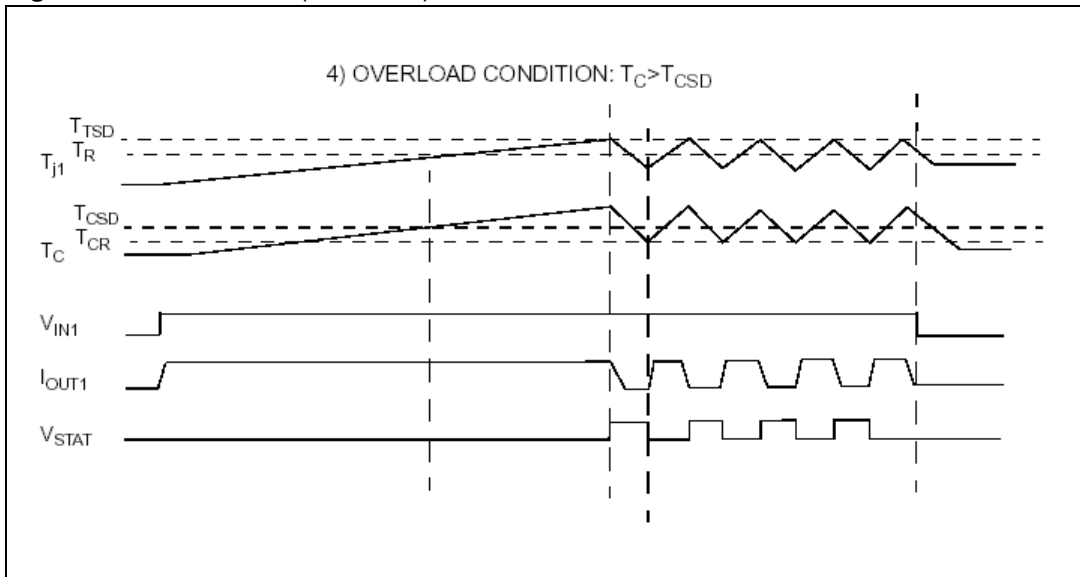


Figure 8. Waveforms



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Figure 8. Waveforms (continued)



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## 6 Reverse polarity protection

A schematic solution to protect the IC against a reverse polarity condition is proposed.

This schematic is effective with any type of load connected to the outputs of the IC.

The  $R_{GND}$  resistor value can be selected according to the following conditions to be met:

1.  $R_{GND} \leq 600 \text{ mV} / (I_S \text{ in ON state max})$ .
2.  $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where  $-I_{GND}$  is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

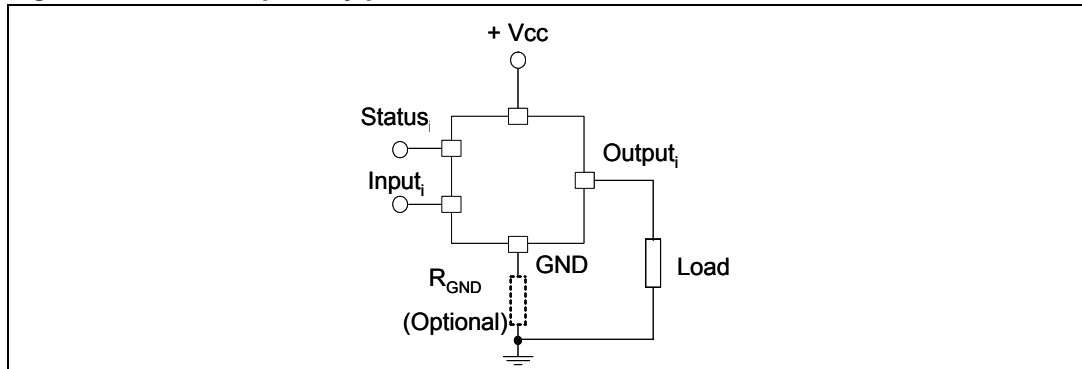
The power dissipation associated to  $R_{GND}$  during reverse polarity condition is:

$$PD = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared by several different ICs. In such case  $I_S$  value on formula (1) is the sum of the maximum ON-state currents of the different devices.

Please note that if the microprocessor ground and the device ground are separated then the voltage drop across the  $R_{GND}$  (given by  $I_S$  in ON state max \*  $R_{GND}$ ) produce a difference between the generated input level and the IC input signal level. This voltage drop will vary depending on how many devices are ON in the case of several high side switches sharing the same  $R_{GND}$ .

**Figure 9. Reverse polarity protection**



## 7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

**Table 10. PowerSO-36 mechanical data**

Dim.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			3.60			0.1417
a1	0.10		0.30	0.003		0.0118
a2			3.30			0.1299
a3	0		0.10	0		0.0039
b	0.22		0.38	0.008		0.0150
c	0.23		0.32	0.009		0.0126
D (1)	15.80		16.00	0.622		0.6299
D1	9.40		9.80	0.370		0.3858
E	13.90		14.50	0.547		0.5709
E1 (1)	10.90		11.10	0.429		0.4370
E2			2.90			0.1142
E3	5.8		6.2	0.228		0.2441
e		0.65			0.025	
e3		11.05			0.435	
G	0		0.10	0.000		0.0039
H	15.50		15.90	0.610		0.6260
h			1.10			0.0433
L	0.80		1.10	0.031		0.0433
N			10°			10°
S	0°		8°	0°		8°

Figure 10. PowerSO-36 drawings

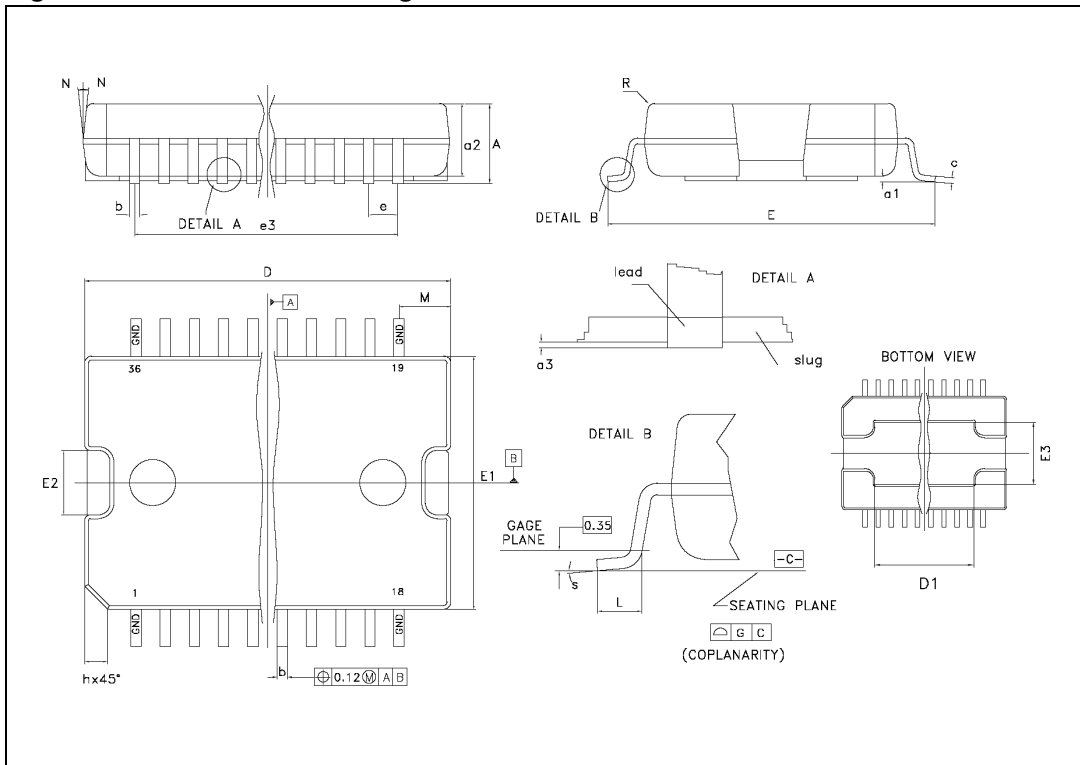
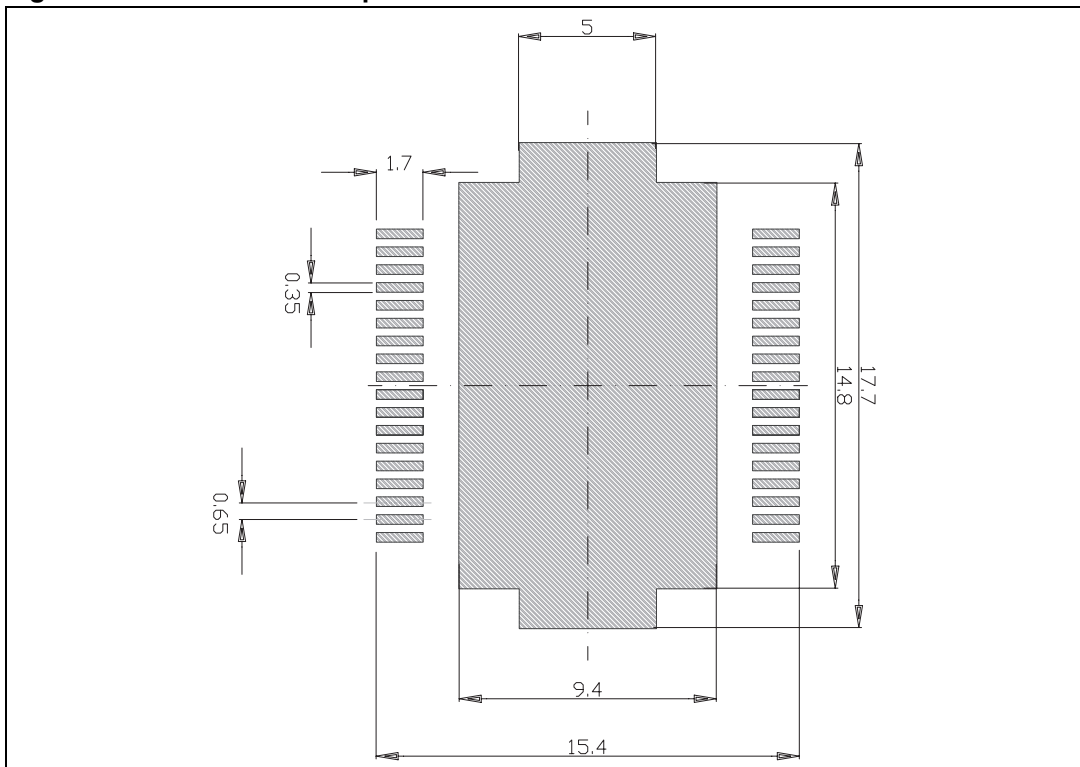


Figure 11. PowerSO-36 footprint



## 8 Order codes

**Table 11. Order codes**

Order codes	Package	Packaging
VN808-E	PowerSO-36	Tube
VN808TR-E	PowerSO-36	Tape and reel



## 9 Revision history

**Table 12. Document revision history**

Date	Revision	Changes
13-Sep-2005	1	Initial release
1-Mar-2007	2	Document reformatted
12-Mar-2007	3	Typo in <i>Figure 3</i> .
26-Mar-2007	4	Typo note <i>Table 2</i> .
07-Jul-2008	5	Added: <i>Section 6 on page 13</i>
04-Aug-2008	6	Added: <i>Figure 11: PowerSO-36 footprint on page 15</i>

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