

FEATURES

- 8-Bit Bus Compatible 12-Bit DAC
- Versatile Microprocessor Interface with Selectable Data Input Format and Data Override
- Faster Interface Timing
- High Accuracy: Low $\pm 1/2$ LSB INL Error Over Temperature and ± 1 LSB Gain Error
- Superior Power Supply Rejection from +5V to +15V 0.001%/ % Max
- Low Feedthrough Error and Digital Charge Injection
- Data Inputs Designed with ESD Protective Circuitry
- Narrow (0.3") DIP Packages Suitable for Auto-Insertion
- Superior Direct Replacement for AD7548
- Full Four Quadrant Multiplication
- Available in Die Form

APPLICATIONS

- Process Control
- Programmable Amplifiers
- Digitally Controlled Power Supplies
- Digitally Controlled Attenuators
- Digitally Controlled Filters

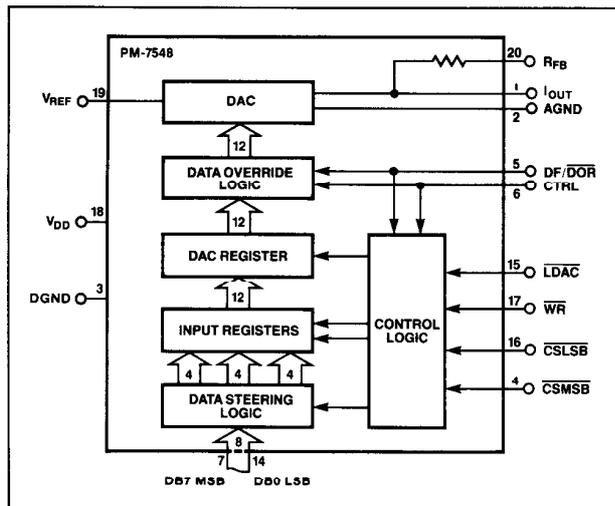
ORDERING INFORMATION [†]

PACKAGE: 20-PIN				
GAIN ERROR	NON-LINEARITY	MILITARY*	EXTENDED INDUSTRIAL	COMMERCIAL
		TEMPERATURE -55°C to +125°C	TEMPERATURE -40°C to +85°C	TEMPERATURE 0°C to +70°C
± 1 LSB	$\pm 1/2$ LSB	PM7548AR	PM7548ER	PM7548GP
± 2 LSB	$\pm 1/2$ LSB	PM7548BR	PM7548FR	—
± 2 LSD	$\pm 1/2$ LSD	PM7548DRC/003	PM7548FP	—
± 2 LSB	$\pm 1/2$ LSB	—	PM7548FPC	—
± 2 LSB	$\pm 1/2$ LSB	—	PM7548FS	—

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

[†] Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

FUNCTIONAL BLOCK DIAGRAM



CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7548AR	AD7548TD	MIL
PM7548BR	AD7548SD	
PM7548ER	AD7548BQ	IND
PM7548FR	AD7548AQ	
PM7548GP	AD7548KN	COM
PM7548FP	AD7548IN	
PM7548FPC	AD7548JP	

GENERAL DESCRIPTION

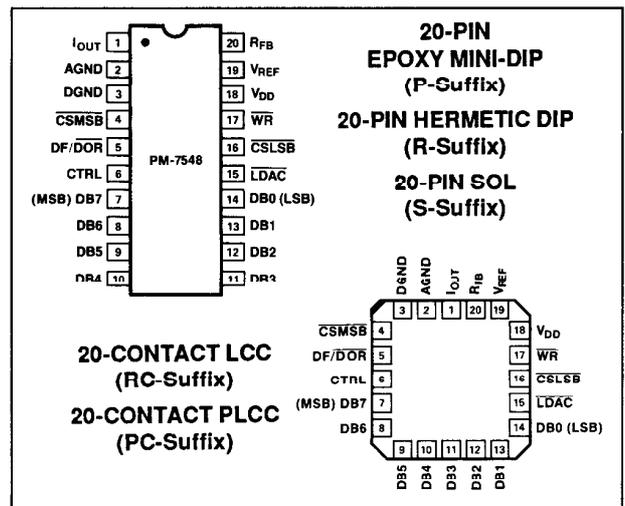
The PM-7548 is a 12-bit resolution, current output, CMOS D/A converter with a microprocessor interface for 8-bit busses. Its improved accuracy and inputs designed with ESD protection circuitry make it a superior pin-compatible replacement to the industry standard 7548. These performance improvements permit the upgrading of existing designs with greater accuracy and ruggedness. Tighter linearity and gain error specifications may permit a reduced circuit parts count through the elimination of trimming components. The PM-7548 is available in standard plastic and CERDIP packages that are compatible with auto-insertion equipment.

The PM-7548's versatile interface allows data to be loaded into an output register in two bytes. The PM-7548 can accept data right or left justified, least or most significant byte first, under microprocessor control. Faster interface timing minimizes microprocessor wait states.

Analog output updating and the loading of new data into the input registers may be coincident or separated in time by use of the $\overline{\text{LDAC}}$ control input. This allows user control of data update and analog output update timing.

Data override control allows full-scale or zero-scale analog outputs without altering the contents of the DAC registers. This permits the user to perform circuit calibration without the need to load calibration data into the DAC registers.

PIN CONNECTIONS



PM-7548

ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$, unless otherwise noted.)

V_{DD} (to GND)	+17V
V_{REF} (to GND)	$\pm 25\text{V}$
V_{REFB} (to GND)	$\pm 25\text{V}$
Digital Input Voltage Range	-0.3V to V_{DD}
Output Voltage (Pin 1, Pin 2)	-0.3 to V_{DD}
Operating Temperature Range	
AR/BR/BRC Versions	-55°C to $+125^\circ\text{C}$
ER/FR/FP/FPC/FS Versions	-40°C to $+85^\circ\text{C}$
GP Version	0°C to $+70^\circ\text{C}$
Junction Temperature	$+150^\circ\text{C}$
Storage Temperature	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)	$+300^\circ\text{C}$

PACKAGE TYPE	θ_{JA} (Note 1)	θ_{JC}	UNITS
20-Pin Hermetic DIP (R)	76	11	$^\circ\text{C/W}$
20-Pin Plastic DIP (P)	69	27	$^\circ\text{C/W}$
20-Contact LCC (RC, TC)	88	33	$^\circ\text{C/W}$
20-Pin SOL (S)	88	25	$^\circ\text{C/W}$
20-Contact PLCC (PC)	73	33	$^\circ\text{C/W}$

NOTES:

1. θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; θ_{JA} is specified for device soldered to printed circuit board for SOL and PLCC packages.

CAUTION:

1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} (Pin 17) and R_{FB} (Pin 18).
2. The digital control inputs are zener protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Use proper antistatic handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and dice. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS at $V_{DD} = +5\text{V}, +12\text{V}$ or $+15\text{V}$; $V_{REF} = +10\text{V}$; $V_{OUT} = V_{AGND} = V_{DGND} = 0\text{V}$; $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ for PM-7548AR/BR/BRC, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ for PM-7548ER/FR/FP/FPC/FS, and $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ for PM-7548GP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7548			UNITS
			MIN	TYP	MAX	
STATIC ACCURACY						
Resolution	N		12	—	—	Bits
Integral Nonlinearity (Note 1)	INL		—	—	1/2	LSB
Differential Nonlinearity (Note 2)	DNL	PM-7548A/E/G PM-7548B/F	—	—	1/2 1	LSB
Gain Error (Note 3)	G_{FSE}	$T_A = +25^\circ\text{C}$ PM-7548A/E/G PM-7548B/F $T_A = \text{Full Temperature Range}$ PM-7548A/E/G PM-7548B/F	—	—	1 2 3	LSB
Gain Temperature Coefficient (Note 6)	TCG_{FS}		—	± 1	± 5	ppm/ $^\circ\text{C}$
Power Supply Rejection Ratio	PSRR	$T_A = +25^\circ\text{C}$ $T_A = \text{Full Temperature Range}$	—	—	± 0.001 ± 0.002	%/%
Output Leakage Current (Notes 4, 5)	I_{LKG}	$T_A = +25^\circ\text{C}$ $T_A = \text{Full Temperature Range}$ PM-7548A/B PM-7548E/F/G	—	± 12	± 5 ± 100 ± 25	nA
Feedthrough Error (Note 6)	FT	$V_{REF} = 20\text{V}_{p-p}$ at $f = 10\text{kHz}$ All digital inputs LOW	—	—	5	mV_{p-p}
Zero Scale Error (Notes 12, 13)	I_{ZSE}	$T_A = +25^\circ\text{C}$ $T_A = \text{Full Temperature Range}$ PM-7548A/B PM-7548E/F/G	—	0.002 0.07 0.01	—	LSB
Input Resistance (Note 9)	R_{IN}		7	11	15	k Ω

ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V, +12V$ or $+15V$; $V_{REF} = +10V$; $V_{OUT} = V_{AGND} = V_{DGND} = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ for PM-7548AR/BR/BRC, $T_A = -40^\circ C$ to $+85^\circ C$ for PM-7548ER/FR/FP/FPC/FS, and $T_A = -^\circ C$ to $+70^\circ C$ for PM-7548GP, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-7548			UNITS
			MIN	TYP	MAX	
AC PERFORMANCE						
Output Current Settling Time (Notes 6, 7, 8)	t_s	$T_A = +25^\circ C$	-	-	1	μs
Digital-to-Analog Glitch Energy (Notes 6, 11)	Q	$V_{REF} = 0V$ I_{OUT} Load = 100Ω $C_{EXT} = 13pF$ DAC Register Loaded Alternately with All 0s and All 1s	-	-	200	nVs
Total Harmonic Distortion (Note 6)	THD	$V_{REF} = 6V_{rms}$ @ 1kHz DAC Register Loaded with All 1s	-	-	-90	dB
Output Noise Voltage Density (Notes 6, 14)	e_n	10Hz to 100kHz Measured Between R_{FB} and I_{OUT}	-	-	13	nV/\sqrt{Hz}
DIGITAL INPUTS						
Digital Input HIGH	V_{IH}		2.4	-	-	V
Digital Input LOW	V_{IL}		-	-	0.8	V
Input Leakage Current (Note 10)	I_{IL}	$V_{IN} = 0V$ to $+15V$	-	-	± 1	μA
Input Capacitance (Note 6)	C_{IN}	$V_{IN} = 0V$	-	-	8	pF
ANALOG OUTPUTS						
Output Capacitance (Note 6)	C_{OUT}	Digital Inputs = V_{IH}	-	-	140	pF
Output Capacitance (Note 6)	C_{OUT}	Digital Inputs = V_{IL}	-	-	70	pF
TIMING CHARACTERISTICS (Note 6)						
Data Valid Setup Time	t_{DS}	$T_A = +25^\circ C$ $T_A =$ Full Temperature Range	160 210	- -	- -	ns
Data Valid Hold Time	t_{DH}	$T_A = +25^\circ C$ $T_A =$ Full Temperature Range	10 10	- -	- -	ns
CSMSB or CSLSB to WR Setup Time	t_{CWS}	$T_A = +25^\circ C$ $T_A =$ Full Temperature Range	0 0	- -	- -	ns
CSMSB or CSLSB to WR Hold Time	t_{CWH}	$T_A = +25^\circ C$ $T_A =$ Full Temperature Range	0 0	- -	- -	ns
LDAC to WR Setup Time	t_{LWS}	$T_A = +25^\circ C$ $T_A =$ Full Temperature Range	0 0	- -	- -	ns
LDAC to WR Hold Time	t_{LWH}	$T_A = +25^\circ C$ $T_A =$ Full Temperature Range	0 0	- -	- -	ns
Write Pulse Width	t_{WR}	$T_A = +25^\circ C$ $T_A =$ Full Temperature Range	120 120	- -	- -	ns

NOTES:

- $\pm 1/2$ LSB = $\pm 0.012\%$ of Full Scale.
- All grades are monotonic to 12-bits over temperature.
- Using internal feedback resistor.
- Applies to I_{OUT} ; digital inputs = V_{IL} .
- Specification also applies for AGND with all digital inputs = V_{IL} .
- Guaranteed by design and not subject to test.
- I_{OUT} Load = 100Ω , $C_{EXT} = 13pF$, digital inputs = $0V$ to V_{DD} or V_{DD} to $0V$.
- Extrapolated to $1/2$ LSB: $t_s =$ Propagation Delay (t_{PD}) + 9τ , where $\tau =$ measured first time constant of the final RC decay.
- Absolute temperature coefficient is approximately $+50ppm/^\circ C$.
- Digital inputs are CMOS gates; I_{IN} is typically $1nA$ at $+25^\circ C$.
- $V_{REF} = 0V$, all digital inputs = $0V$ to V_{DD} or V_{DD} to $0V$.
- $V_{REF} = +10V$, all digital inputs = $0V$.
- Calculated from worst case $R_{REF} \cdot I_{ZSE}$ (in LSBs) = $(R_{REF} \times I_{LKG} \times 4096) / V_{REF}$.
- Calculated from $e_n = \sqrt{4KTRB}$
where: K = Boltzmann Constant, $J/^\circ K$
T = Resistor Temperature, $^\circ K$
R = Resistance, Ω
B = Bandwidth, Hz.

2

PM-7548

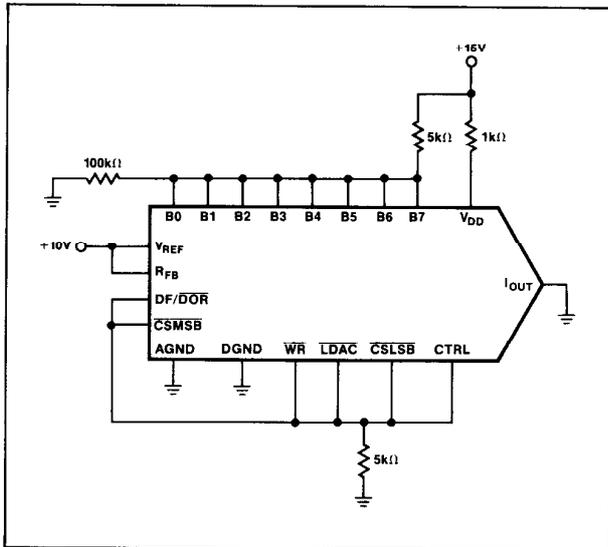
ELECTRICAL CHARACTERISTICS at $V_{DD} = +12V$ or $+15V$; $V_{REF} = +10V$; $V_{OUT} = V_{AGND} = V_{DGND} = 0V$; $T_A = -55^{\circ}C$ to $+125^{\circ}C$ for PM-7548AR/BR/BRC, $T_A = -40^{\circ}C$ to $+85^{\circ}C$ for PM-7548ER/FR/FP/FPC/FS, and $T_A = 0^{\circ}C$ to $+70^{\circ}C$ for PM-7548GP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7548			UNITS
			MIN	TYP	MAX	
POWER SUPPLY						
V_{DD} Range	V_{DD}		11.4	—	15.75	V
Supply Current	I_{DD}	All digital inputs = V_{INH} or V_{INL} All digital input = $0V$ or V_{DD}	—	—	3	mA
			—	—	1	μA

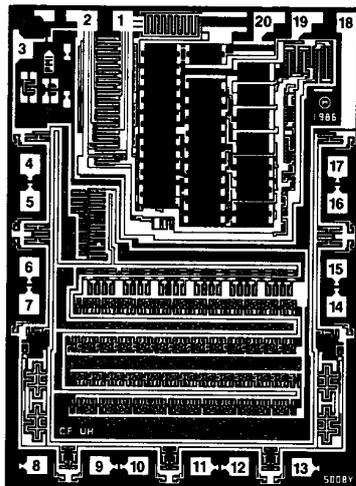
ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$; $V_{REF} = +10V$; $V_{OUT} = V_{AGND} = V_{DGND} = 0V$; $T_A = -55^{\circ}C$ to $+125^{\circ}C$ for PM-7548AR/BR/BRC, $T_A = -25^{\circ}C$ to $+85^{\circ}C$ for PM-7548ER/FR, and $T_A = 0^{\circ}C$ to $+70^{\circ}C$ for PM-7548GP/HP/HPC, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7548			UNITS
			MIN	TYP	MAX	
POWER SUPPLY						
V_{DD} Range	V_{DD}		4.75	5	5.25	V
Supply Current	I_{DD}	All digital inputs = V_{INH} or V_{INL} All digital input = $0V$ or V_{DD}	—	—	2	mA
			—	120	300	μA

BURN-IN CIRCUIT



DICE CHARACTERISTICS



- | | |
|------------------------|------------------------|
| 1. I_{OUT} | 11. DB3 |
| 2. AGND | 12. DB2 |
| 3. DGND | 13. DB1 |
| 4. \overline{CSMSB} | 14. DB0 (LSB) |
| 5. $\overline{DF/DOR}$ | 15. \overline{LDAC} |
| 6. CTRL | 16. \overline{CSLSB} |
| 7. DB7 (MSB) | 17. \overline{WR} |
| 8. DB6 | 18. V_{DD} |
| 9. DB5 | 19. V_{REF} |
| 10. DB4 | 20. R_{FB} |

DIE SIZE 0.096 × 0.130 inch, 12,480 sq. mils
(2.46 × 3.33mm, 8.20 sq. mm)

WAFER TEST LIMITS at $V_{DD} = +5V$, $V_{REF} = +10V$, $AGND = DGND = 0V$, $V_{OUT} = AGND = 0V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7548GBC LIMIT	UNITS
STATIC ACCURACY				
Resolution	N		12	Bits MIN
Nonlinearity	INL		$\pm 1/2$	LSB MAX
Differential Nonlinearity	DNL		$\pm 1/2$	LSB MAX
Gain Error (Note 1)	G_{FSE}		± 1	LSB MAX
Power Supply Rejection	PSRR	$\Delta V_{DD} = \pm 5\%$	± 0.001	%/% MAX
Output Leakage Current (I_{OUT})	I_{LKG}	$V_{DD} = +15V$ Digital Inputs = V_{IL}	± 5	nA MAX
REFERENCE INPUT				
Input Resistance	R_{REF}		//15	k Ω MIN/MAX
DIGITAL INPUTS				
Digital Input HIGH	V_{IH}		2.4	V MIN
Digital Input LOW	V_{IL}		0.8	V MAX
Input Leakage Current	I_{IL}	$V_{DD} = +15V$ $V_{IN} = 0$ to $15V$	± 1	μA MAX
POWER SUPPLY				
Supply Current	I_{DD}	$V_{DD} = +15V$ Digital Inputs = V_{IH} or V_{IL} Digital Inputs = $0V$ or V_{DD}	3 1	mA MAX

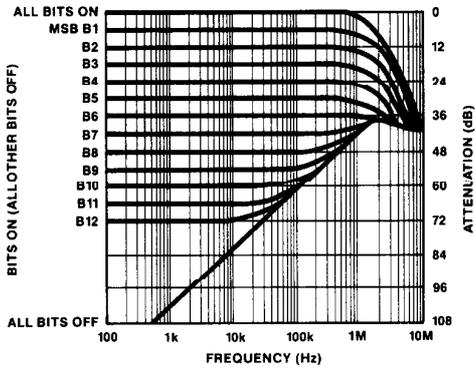
NOTES:

1. Using internal feedback resistor.

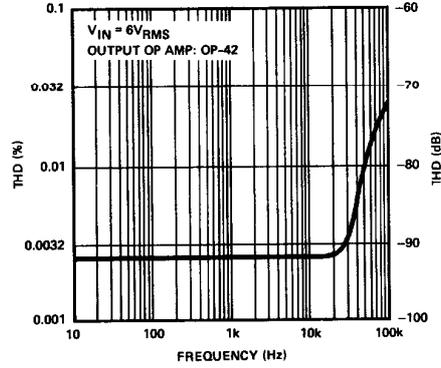
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

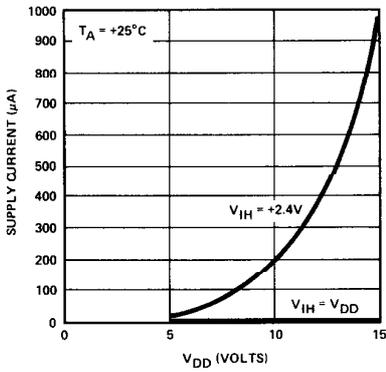
**MULTIPLYING MODE
FREQUENCY RESPONSE
vs DIGITAL CODE**



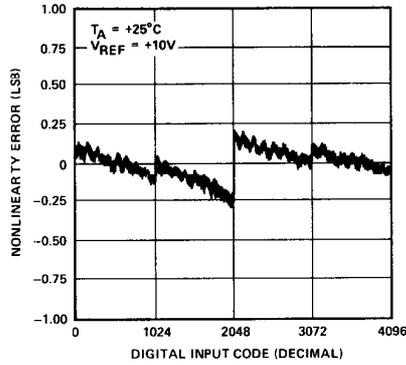
**MULTIPLYING MODE
TOTAL HARMONIC
DISTORTION vs FREQUENCY**



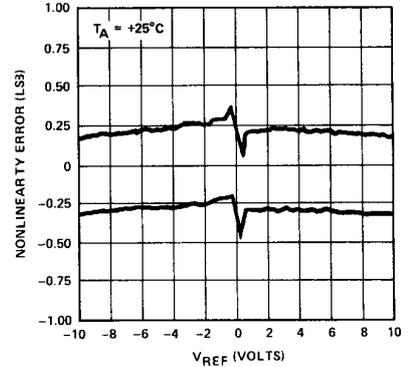
**SUPPLY CURRENT vs
SUPPLY VOLTAGE**



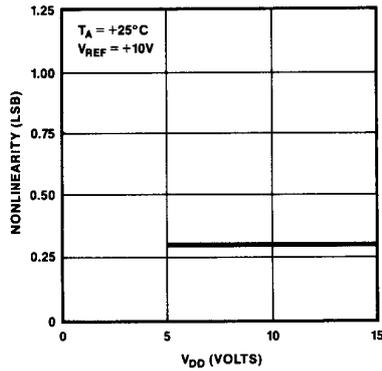
**NONLINEARITY ERROR vs
DIGITAL CODE
(VDD = +5V OR +15V)**



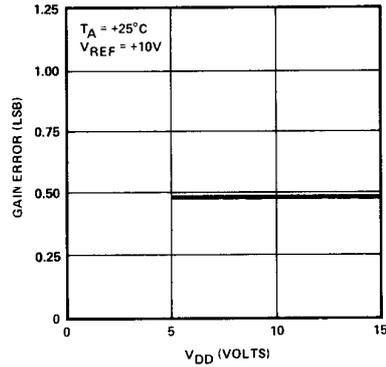
**NONLINEARITY ERROR vs
REFERENCE VOLTAGE
(VDD = +5V OR +15V)**



**NONLINEARITY vs
SUPPLY VOLTAGE**



**GAIN ERROR vs
SUPPLY VOLTAGE**



SPECIFICATION DEFINITIONS

RESOLUTION

The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into, where "n" is equal to the number of bits.

SETTLING TIME

Time required for the analog output of the DAC to settle to within 1/2 LSB of its final value for a given digital input stimulus; i.e. zero to full scale.

GAIN

Ratio of the DAC's external operational amplifier output voltage to the V_{REF} input voltage when all digital inputs are HIGH.

FEEDTHROUGH ERROR

Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE

Capacitance from I_{OUT} terminal with all digital inputs LOW, or on AGND terminal when all inputs are HIGH.

OUTPUT LEAKAGE CURRENT

Current appearing at I_{OUT} when all digital inputs are LOW, or at AGND when all inputs are HIGH.

GENERAL CIRCUIT INFORMATION

The PM-7548 is a 12-bit multiplying D/A converter with a very low temperature coefficient, R-2R resistor ladder network, data-steering and control logic, and two data registers.

The digital circuitry forms a versatile interface between the 12-bit DAC and an 8-bit data bus. Several data formats can be accommodated, single or double buffering is available, and a data override function allows calibration data to be loaded into the DAC without altering data stored in the buffer registers.

A simplified circuit of the PM-7548 is shown in Figure 1. An inverted R-2R ladder network consisting of silicon-chrome, thin-film resistors, and twelve pairs of NMOS current-steering switches steer binarily weighted currents into either I_{OUT} or AGND. Switching current to ground or I_{OUT} yields a constant current in each ladder leg, regardless of digital input code. This constant current results in a constant input resistance at V_{REF} equal to R (typically 11k Ω). The V_{REF} input may be driven by any reference voltage or current, ac or dc, that is within the limits stated in the Absolute Maximum Ratings chart.

The PM-7548 design incorporates a regulator circuit which assures TTL compatibility at any V_{DD} from +5V to +15V across the full military temperature range. This regulator also contributes to the DAC's exceptional PSRR performance, and maintains timing performance independent of supply voltage.

The twelve output current-steering switches are in series with the R-2R resistor ladder, and therefore, can introduce bit errors. It is essential then, that the switch "ON" resistance be binarily scaled so that the voltage drop across each switch remains constant. If, for example, switch 1 of Figure 1 was designed with an "ON" resistance of 10 ohms, switch 2 for 20 ohms, etc., a constant 5mV drop will then be maintained across each switch.

To further insure accuracy across the full temperature range, permanently "ON" MOS switches are included in series with the feedback resistor and the R-2R ladder's terminating resistor. The "Simplified DAC Circuit", Figure 1, shows the location of the series switches. These series switches are equivalently scaled to two times switch 1 (MSB) and to switch 12 (LSB) respectively to maintain constant relative voltage drops with varying temperature. During any testing of the resistor ladder or $R_{FEEDBACK}$ (such as incoming inspection), V_{DD} must be present to turn "ON" these series switches.

ESD PROTECTION

The PM-7548 data inputs have been designed with ESD resistance incorporated through careful layout and the inclusion of input protection circuitry.

Figure 2 shows the input protection diodes. High voltage static charges applied to the digital inputs are shunted to the supply and ground rails through forward biased diodes.

FIGURE 1: Simplified DAC Circuit

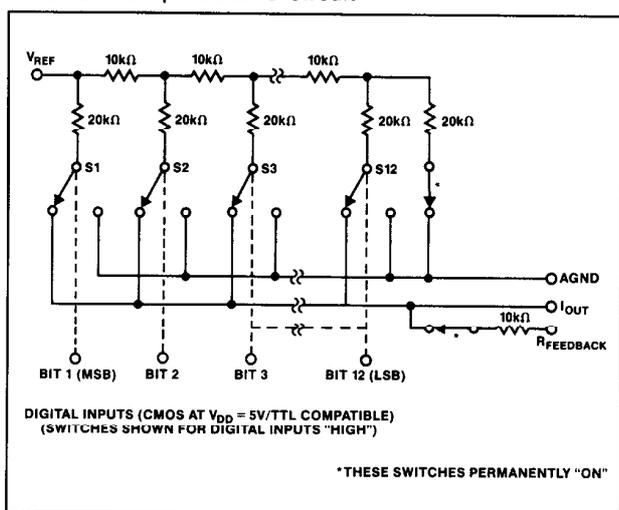
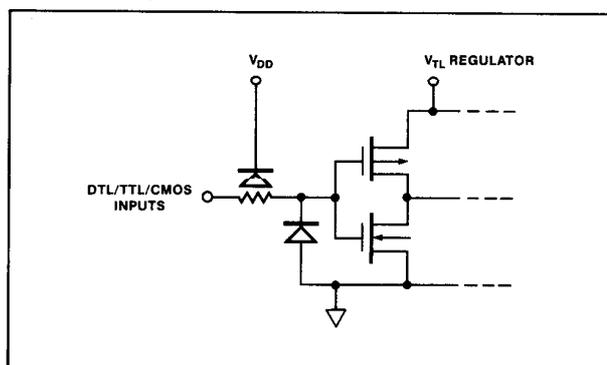


FIGURE 2: Digital Input Protection



PM-7548

These protection diodes are designed to clamp the inputs well below dangerous levels during static discharge conditions.

EQUIVALENT CIRCUIT ANALYSIS

Figures 3 and 4 show equivalent circuits for the DAC with all bits LOW and HIGH, respectively. The reference current is switched to AGND when all data bits are LOW and to I_{OUT} when all bits are HIGH. The $I_{LEAKAGE}$ current source is the combination of surface and junction leakages to the substrate. The $1/4096$ current source represents the constant 1-bit current drain through the ladder's terminating resistor.

Output capacitance is dependent upon the digital input code. This is because the gate capacitance of MOS transistors increases with applied gate voltage. This output capacitance varies between the low and high values.

FIGURE 3: PM-7548 Equivalent Circuit (All Inputs LOW)

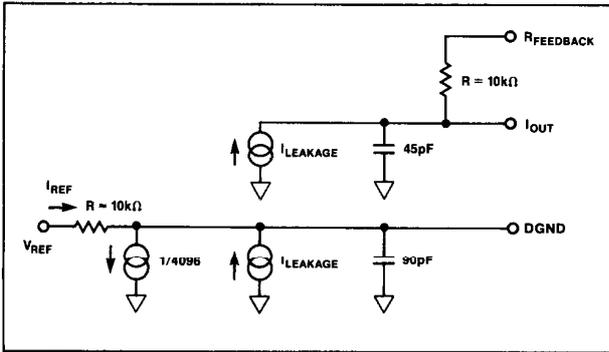
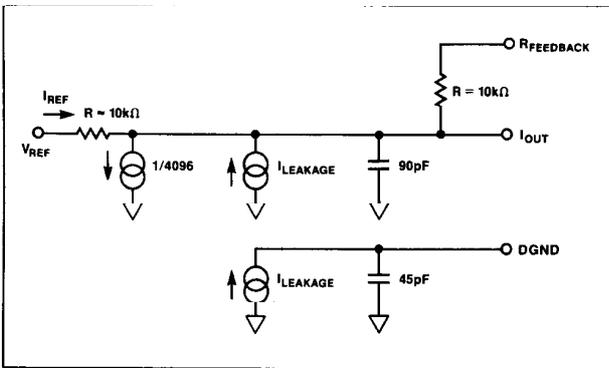


FIGURE 4: PM-7548 Equivalent Circuit (All Digital Inputs HIGH)



INPUT CONTROL INFORMATION

FIGURE 5: PM-7548 Data Input and Control Timing Diagram

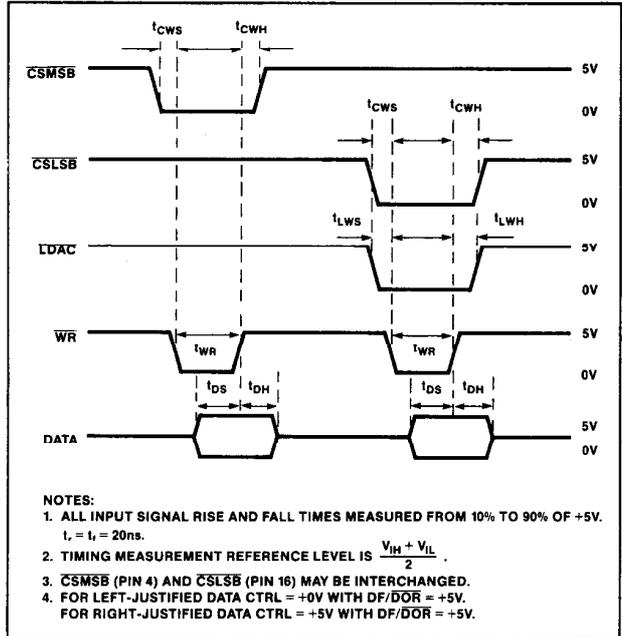
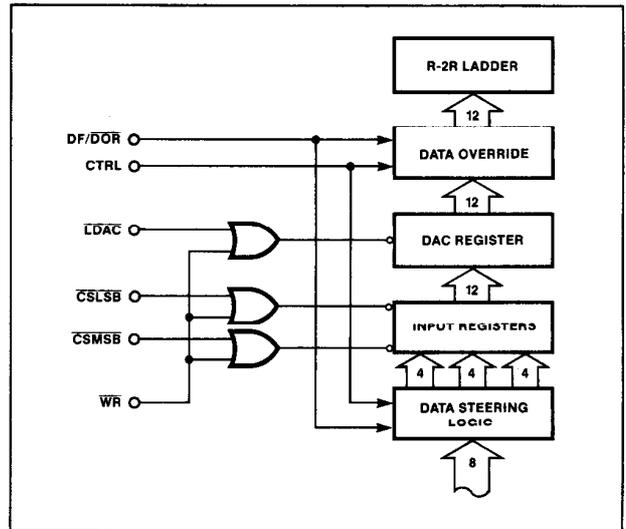


FIGURE 6: Simplified PM-7548 Input Control Structure



DYNAMIC PERFORMANCE

OUTPUT IMPEDANCE

The output resistance, as in the case of the output capacitance, varies with the digital input code. This resistance, looking back into the I_{OUT} terminal, may be between 11kΩ (the feedback resistor alone when all digital inputs are low) and 7.5kΩ (the feedback resistor in parallel with approximately 30kΩ of the R-2R ladder network resistance when any single bit logic is high). Static accuracy and dynamic performance will be affected by these variations. The gain and phase stability of the output amplifier, board layout, and power supply decoupling will all affect the dynamic performance of the PM-7548. The use of a compensation capacitor may be required when high-speed operational amplifiers are used. It may be connected across the amplifiers' feedback resistor to provide the necessary phase compensation to critically damp the output.

The considerations when using high-speed amplifiers are:

1. Phase compensation (see Figures 9 and 10).
2. Power supply decoupling at the device socket and use of proper grounding techniques.

INTERFACE INPUT DESCRIPTION

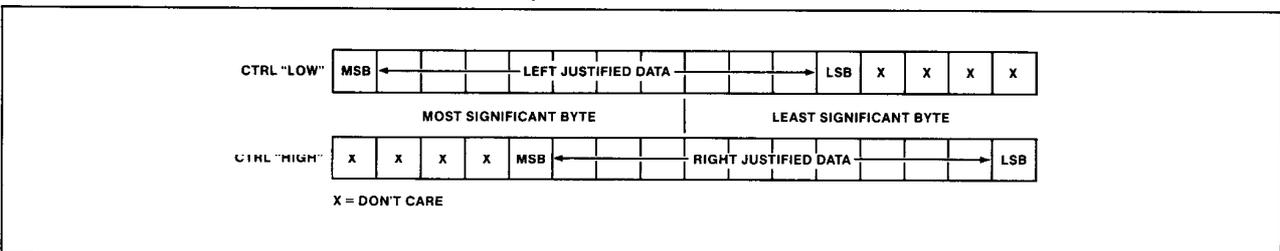
CSMSB (Pin 4) - Chip Select Most Significant Byte. Active Low. Selected either with \overline{WR} , to load most significant byte data into the input register, or with \overline{WR} and \overline{LDAC} to load data into both input and DAC registers.

CSLSB (Pin 16) - Chip Select Least Significant Byte. Active Low. Selected either with \overline{WR} to load least significant byte data into the input register, or with \overline{WR} and \overline{LDAC} to load data into both input and DAC registers.

DF/ \overline{DOR} (Pin 5) - Data Format/Data Override. When LOW, DAC is forced to full-scale or zero-scale output as selected by CTRL. Use of Data Override does not affect data held in DAC register. When DF/ \overline{DOR} is HIGH, CTRL selects either right or left data input format. DF/ \overline{DOR} is normally held HIGH.

DF/ \overline{DOR}	CTRL	Function
0	0	DAC forced to zero-scale (all zeros)
0	1	DAC forced to full-scale (all ones)
1	0	Left-justified data format selected
1	1	Right-justified data format selected

CTRL (Pin 6) - Control Input (Refer also to DF/ \overline{DOR})



\overline{LDAC} (Pin 15) - Load DAC Input. Active Low. Selected, with other interface inputs, to load DAC register from input register or external data bus.

\overline{WR} (Pin 17) - Write Input. Active Low. Selected, with other interface input, to load data into input register and to transfer data from input register to DAC register.

Selected, with other interface input, to load data into input register and to transfer data from input register to DAC register.

\overline{WR}	CSMSB	CSLSB	\overline{LDAC}	Function
0	1	0	1	Load LSByte to Input Register
0	1	0	0	Load LSByte to Input and DAC Registers
0	0	1	1	Load MSByte to Input Register
0	0	1	0	Load MSByte to Input and DAC Registers
0	1	1	0	Load Input Register to DAC Register
1	X	X	X	No Data Transfer

DATA LOADING AND TRANSFER

DATA INPUT AND TRANSFER

Data may be loaded into the input register in either a left- or right-justified format. The data format is selected through the DF/ \overline{DOR} and CTRL inputs (refer to Interface Input Description).

Data transfer, from the input register to the DAC register, can be automatic upon loading of the second data byte into the input register or can occur at a later time through a strobed transfer.

STROBED DATA TRANSFER MODE

Strobed data transfer allows the full 12-bit digital word to be loaded into the input register and transferred to the DAC register at some later time. This transfer mode requires three write cycles: two to load the new digital word, and a third to

FIGURE 7: Strobed Data Transfer Mode

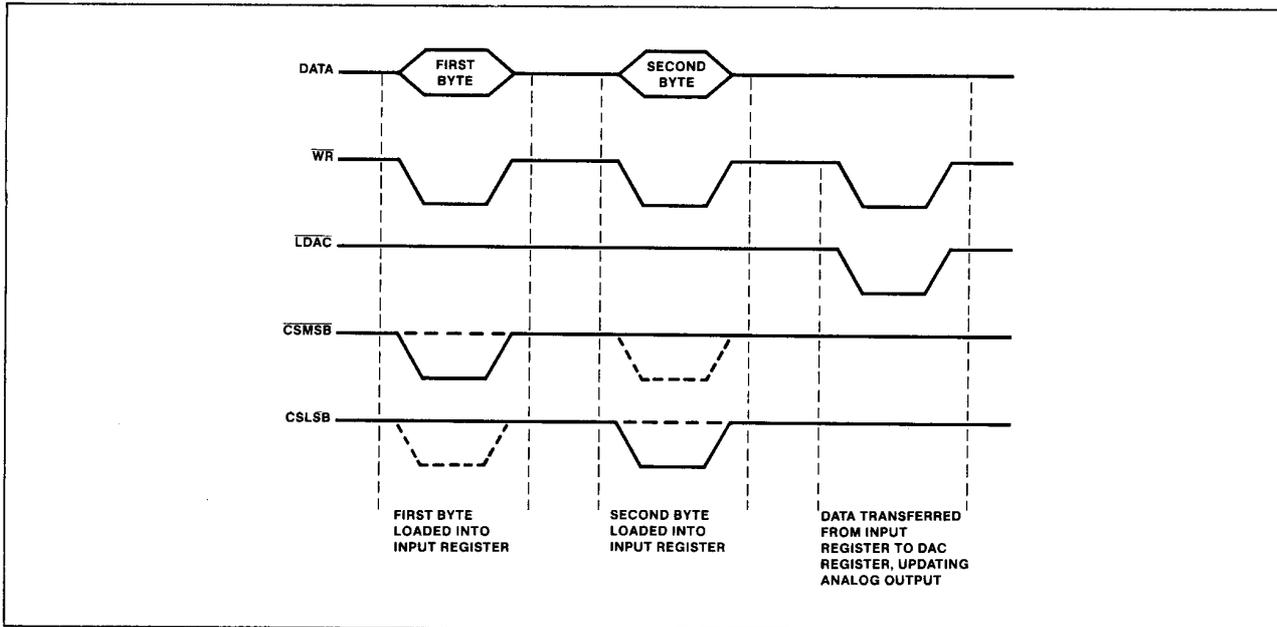
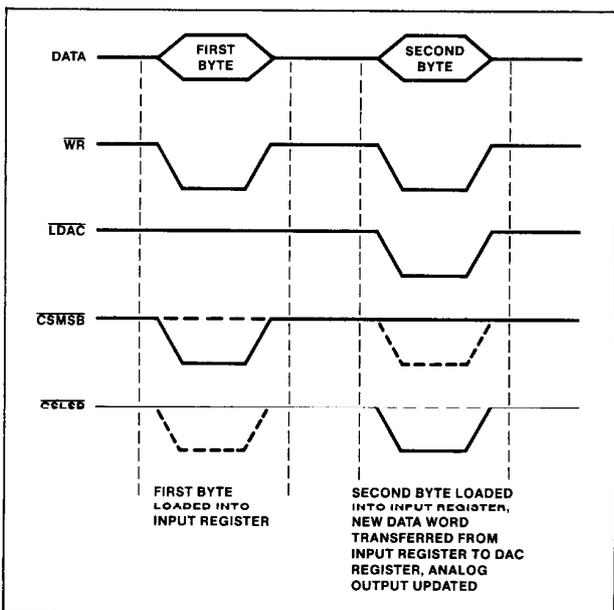


FIGURE 8: Automatic Data Transfer Mode



transfer data to the DAC register. The timing diagram for strobed data transfer is shown in Figure 7.

Strobed data transfer has two primary uses. By separating data loading and transfer operations, the timing of DAC output updating may be more precisely controlled. Simultaneous updating of multiple PM-7548s can also be accomplished by the use of a master strobe signal applied to the LDAC pins of the DACs.

A single data byte can be updated in two write cycles with the strobed transfer mode.

DATA OVERRIDE

System calibration typically requires full-scale and zero-scale DAC outputs (digital words all 1s and 0s respectively). The PM-7548's data override ability allows full-scale and zero-scale outputs without altering the contents of the DAC and input registers, or requiring the controlling microprocessor to load calibration data.

Data override is accessed by setting the DF/\overline{DOR} pin LOW. The CTRL pin then selects the override code: CTRL LOW yields all 0s, CTRL HIGH yields all 1s.

AUTOMATIC DATA TRANSFER MODE

Data may be transferred automatically from the input register to the DAC register while loading the second (High or Low) byte. This is the simplest and fastest transfer mode, requiring only two write cycles to load and transfer a complete new digital word. This operation can be simplified by connecting LDAC directly to either CSMSB or CSLSB so that the write cycle which loads the second data byte also initiates data word transfer.

The timing diagram for automatic transfer is shown in Figure 8. The first write cycle loads the first data byte into the input register. The second write cycle loads the second data byte and simultaneously transfers the full data word to the DAC register.

Automatic transfer allows updating of a single byte in one write cycle.

APPLICATIONS INFORMATION
APPLICATION TIPS

In most applications, linearity depends upon the potential of I_{OUT} and AGND (pins 1 and 2) being exactly equal to each other. In most applications, the DAC is connected to an external op amp with its noninverting input tied to ground, (see Figures 9 and 10). The amplifier selected should have a low input bias current and low drift over temperature. The amplifier's input offset voltage should be nulled to less than $\pm 200\mu V$ (less than 10% of 1 LSB).

The operational amplifier's noninverting input should have a minimum resistance connection to ground; the usual bias current compensation resistor should not be used. This resistor can cause a variable offset voltage appearing as a varying output error. All grounded pins should tie to a common ground point, avoiding ground loops. The V_{DD} power supply should have a low noise level with no transients greater than +17V.

Unused digital inputs must always be grounded or taken to V_{DD} ; this will prevent noise from triggering the high impedance digital input resulting in output errors. It is also recommended that the used digital inputs be taken to ground

or V_{DD} via a high value (1M Ω) resistor; this will prevent the accumulation of static charge if the PC card is disconnected from the system.

Peak supply current flows as the digital inputs pass through the transition voltage. The supply current decreases as the input voltage approaches the supply rails (V_{DD} or DGND), i.e. rapidly slewing logic signals that settle very near the supply rails will minimize supply current.

OUTPUT AMPLIFIER CONSIDERATIONS

When using high speed op amps, a small feedback capacitor (typically 15pF) should be used across the amplifier to minimize overshoot and ringing. For low speed or static applications, AC specifications of the amplifier are not very critical. In high-speed applications, slew rate, settling time, open-loop gain, and gain/phase margin specifications of the amplifier should be selected for the desired performance. It has already been noted that an offset can be caused by including the usual bias current compensation resistor in the amplifier's noninverting input-terminal. This resistor should not be used. Instead, the amplifier should have a bias current which is low over the temperature range of interest.

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FIGURE 9: Unipolar Binary Operation with High Accuracy Op Amp (2-Quadrant)

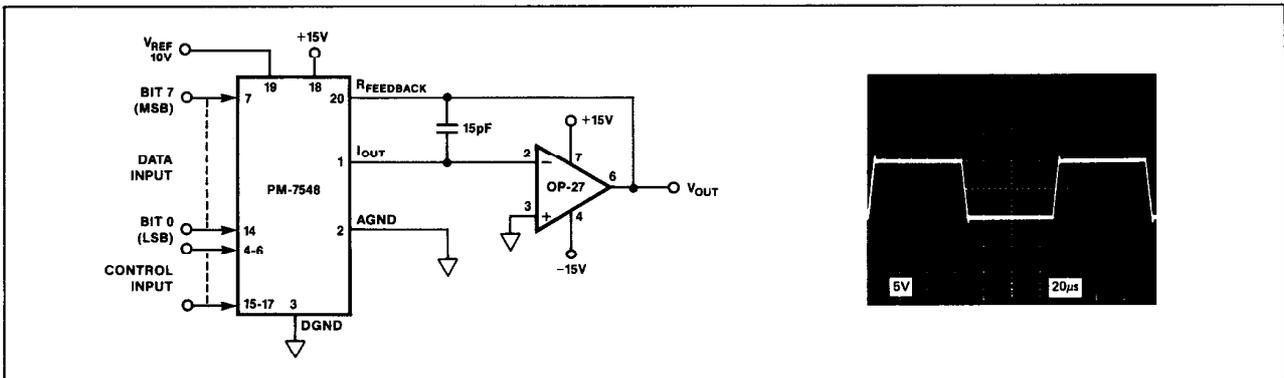
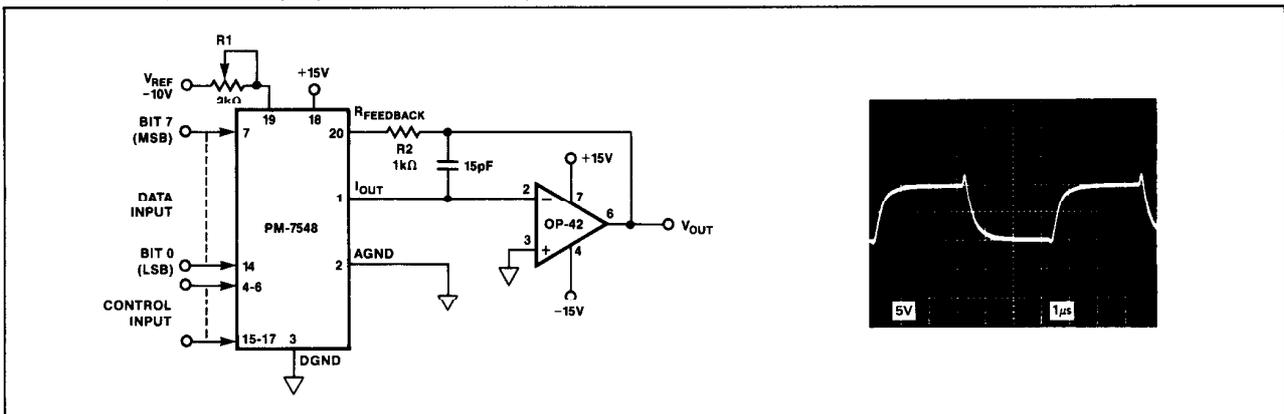


FIGURE 10: Unipolar Binary Operation with Fast Op Amp and Gain Error Trimming (2-Quadrant)



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Static accuracy is affected by the variation in the DAC's output resistance. This variation is best illustrated by using the circuit of Figure 11 and the equation:

$$V_{\text{ERROR}} = V_{\text{OS}} \left(1 + \frac{R_{\text{FB}}}{R_{\text{O}}} \right)$$

where R_{O} is a function of the digital code, and:

- $R_{\text{O}} = 10\text{k}\Omega$ for more than 4-bits of logic 1
- $R_{\text{O}} = 30\text{k}\Omega$ for any single bit logic 1

Therefore, the offset gain varies as follows:

At code 0011 1111 1111,

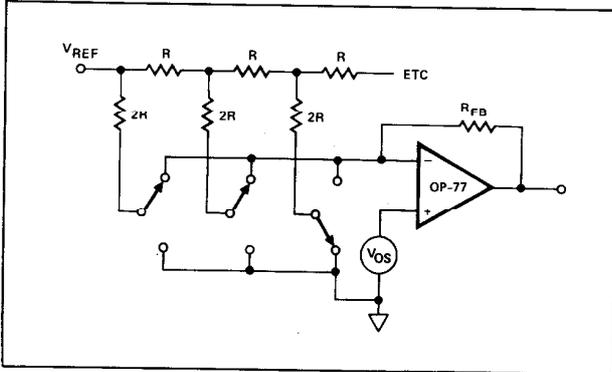
$$V_{\text{ERROR}} = V_{\text{OS}} \left(1 + \frac{10\text{k}\Omega}{10\text{k}\Omega} \right) = 2V_{\text{OS}}$$

At code 0100 0000 0000.

$$V_{\text{ERROR}} = V_{\text{OS}} \left(1 + \frac{10\text{k}\Omega}{30\text{k}\Omega} \right) = 4/3V_{\text{OS}}$$

The error difference is $2/3 V_{\text{OS}}$.

FIGURE 11: Simplified Circuit



Since one LSB has a weight (for $V_{\text{REF}} = +10\text{V}$) of 2.4mV for the PM-7548, it is clearly important that V_{OS} be minimized, either using the amplifier's nulling pins, an external nulling network, or by selection of an amplifier with inherently low V_{OS} . Amplifiers with sufficiently low V_{OS} include PMI's OP-77, OP-07, OP-27, and OP-42.

UNIPOLAR BINARY OPERATION (2-QUADRANT)

The circuit shown in Figures 9 and 10 may be used with an AC or DC reference voltage. The circuit's output will range between 0V and approximately $-V_{\text{REF}} (4095/4096)$ depending upon the digital input code. The relationship between the

digital input code and the analog output is shown in Table 1. The limiting parameters for the V_{REF} range are the maximum input voltage range for the op amp or $\pm 25\text{V}$, whichever is lowest.

Gain error may be trimmed by adjusting R_1 as shown in Figure 10. The DAC register must first be loaded with all 1s. This is most easily accomplished by asserting Data Override HIGH (DF/DOR LOW and CTRL HIGH). R_1 may then be adjusted until $V_{\text{OUT}} = -V_{\text{REF}} (4095/4096)$. In the case of an adjustable V_{REF} , R_1 and R_{FEEDBACK} may be omitted, with V_{REF} adjusted to yield the desired full-scale output.

In many applications the PM-7548's negligible zero scale error and very low gain error permit the elimination of the trimming components (R_1 and the external R_{FEEDBACK}) without adverse effects on circuit performance.

TABLE 1: Unipolar Binary Code Table

DIGITAL INPUT MSB	LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figures 9 and 10)
1 1 1 1	1 1 1 1 1 1 1 1	$-V_{\text{REF}} \left(\frac{4095}{4096} \right)$
1 0 0 0	0 0 0 0 0 0 0 1	$-V_{\text{REF}} \left(\frac{2049}{4096} \right)$
1 0 0 0	0 0 0 0 0 0 0 0	$-V_{\text{REF}} \left(\frac{2048}{4096} \right) = -\frac{V_{\text{REF}}}{2}$
0 1 1 1	1 1 1 1 1 1 1 1	$-V_{\text{REF}} \left(\frac{2047}{4096} \right)$
0 0 0 0	0 0 0 0 0 0 0 1	$-V_{\text{REF}} \left(\frac{1}{4096} \right)$
0 0 0 0	0 0 0 0 0 0 0 0	$-V_{\text{REF}} \left(\frac{0}{4096} \right) = 0$

NOTES:

- Nominal full scale for the circuits of Figures 9 and 10 is given by $\text{FS} = V_{\text{REF}} \left(\frac{4095}{4096} \right)$.
- Nominal LSB magnitude for the circuits of Figures 9 and 10 is given by $\text{LSB} = V_{\text{REF}} \left(\frac{1}{4096} \right)$ or $V_{\text{REF}} (2^{-n})$.

BIPOLAR BINARY OPERATION (4-QUADRANT)

Figure 12 details a suggested circuit for bipolar, or offset binary operation. Table 2 shows the digital input to analog output relationship. The circuit uses offset binary coding. Two's complement code can be converted to offset binary by software inversion of the MSB or by the addition of an external inverter to the MSB input.

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The applied reference voltage must always be positive with respect to AGND. This will avoid the forward biasing of an internal diode found between I_{OUT} and AGND. The reference voltage must also be maintained within +2.5V of AGND (with V_{DD} between +12V and +15V) to maintain linearity.

The output voltage of this circuit can be described as:

$$V_{OUT} = V_{REF} (n/4096) \left(\frac{R_1 + R_2}{R_1} \right)$$

where n is the decimal equivalent of the digital input word. The ratio of R_1 and R_2 may be varied to give the desired output range.

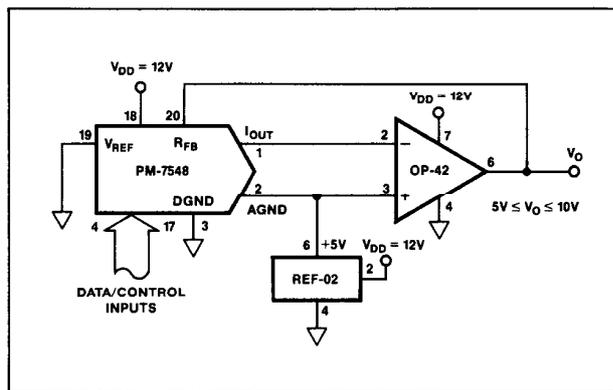
False Ground Mode: Single supply operation can be implemented in a current steering mode as shown in Figure 14. In this circuit, analog ground is offset to a false ground, typically +5V. V_{OUT} ranges between +5V and +10V depending on the digital code and the V_{OFFSET} . V_{OUT} is described by:

$$V_{OUT} = V_{OFFSET} + (n/4096) (V_{OFFSET})$$

where n is the decimal equivalent of the digital input word.

This configuration allows the use of an op amp which cannot operate down to 0V, or "true" ground. For best linearity, V_{DD} should be at least 10V above the false ground.

FIGURE 14: Single Supply Operation (False Ground, Current Steering Mode)



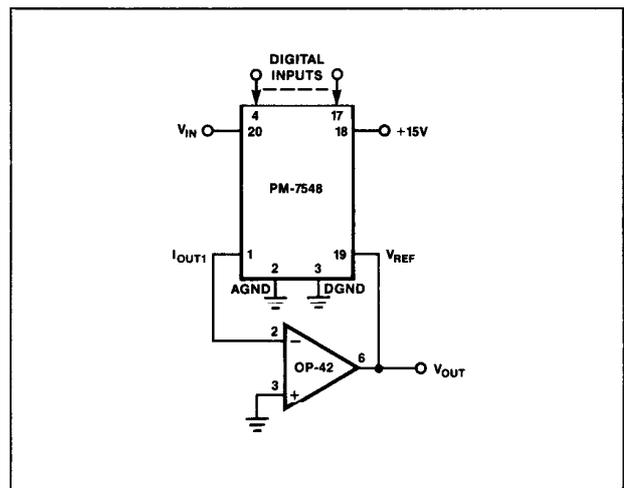
ANALOG/DIGITAL DIVISION

The transfer function for the PM 7548 connected in the multiplying mode as shown in Figure 15 is:

$$V_O = -V_{IN} \left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \dots + \frac{A_{12}}{2^{12}} \right)$$

where A_x assume a value of 1 for an "ON" bit and 0 for an "OFF" bit.

FIGURE 15: Analog/Digital Divider



The transfer function is modified when the DAC is connected in the feedback of an operational amplifier as shown in Figure 15. It is now:

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \dots + \frac{A_{12}}{2^{12}}} \right)$$

The above transfer function is the division of an analog voltage (V_{REF}) by a digital word. The amplifier goes to the rails with all bits "OFF" since division by zero is infinity. With all bits "ON", the gain is 1 (± 1 LSB). The gain becomes 4096 with the LSB, bit 12, "ON".

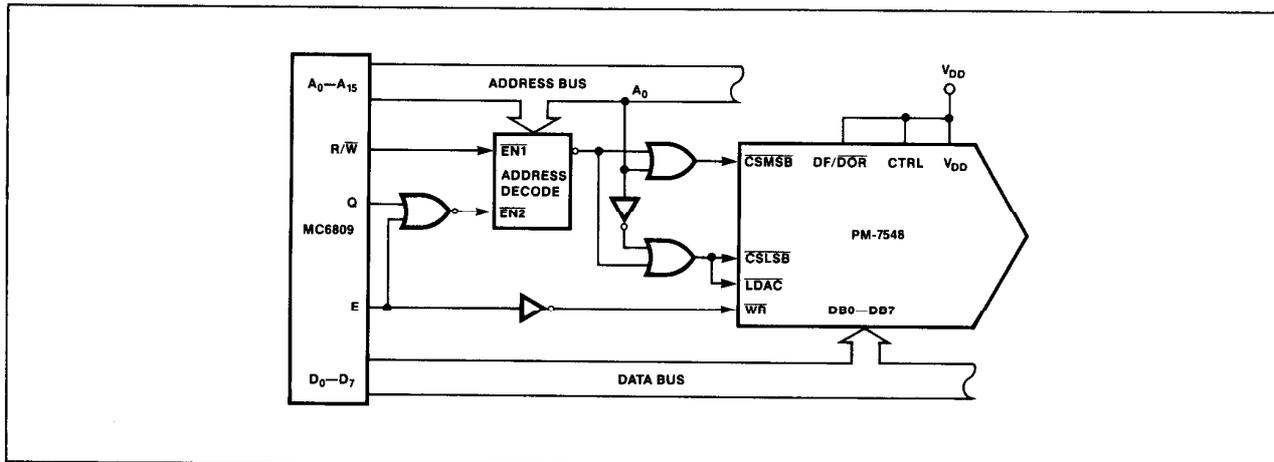
MICROPROCESSOR INTERFACE

The PM-7548 can be directly interfaced to an 8-bit microprocessor's bus. Two such interfaces are shown in Figures 16 and 17.

Figure 16 shows an automatic transfer interface with an MC6809 microprocessor. The PM-7548 is assigned an address, through use of the decoder, that does not use A_0 . The 8-bit high byte may then be loaded using an even (X) address. Next, the 4-bit low byte is loaded to an odd address (X + 1), A_0 selecting both the low byte data loading and the 12-bit data transfer.

Figure 17 shows a multiple DAC, strobed transfer interface configuration, also using the MC6809. Decoding allows independent loading of data with simultaneous updating of both DACs. This technique can be extended to accommodate an unlimited number of DACs with the use of additional decoding.

FIGURE 16: PM-7548/MC6809 Interface Automatic Transfer Mode



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FIGURE 17: PM-7548/MC6809 Interface Multiple DAC, Strobed Transfer Mode

