Final COM'L MIL

T-46-19-13

PAL20R8 Family

24-pin TTL Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- As fast as 7.5 ns maximum propagation delay
- Popular 24-pin architectures: 20L8, 20R8, 20R6, 20R4
- Programmable replacement for high-speed TTL logic
- Power-up reset for initialization
- Easy design with PALASM® software
- Programmable on standard PAL® device programmers
- 24-pin SKINNYDIP® and 28-pin PLCC packages save space

GENERAL DESCRIPTION

The PAL20R8 Family (PAL20L8, PAL20R8, PAL20R6, PAL20R4) is AMD's standard 24-pin PAL device family. The devices provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The family allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

In addition, the PAL device provides the following options:

- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback

Product terms with all connections opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state. Registers consist of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock. Unused input pins should be tied to V_{CC} or GND.

The entire PAL device family is supported by the PALASM software package. The PAL family is programmed on conventional PAL device programmers with appropriate personality and socket adapter modules. See the Programmer Reference Guide for approved programmers. Once the PAL device is programmed and verified an additional connection may be opened to prevent pattern readout. This feature secures proprietary circuits.

2

PRODUCT SELECTOR GUIDE

DEVICE	DEDICATED INPUTS	OUTPUTS	PRODUCT TERMS/ OUTPUT	FEEDBACK	ENABLE
PAL20L8	14	6 comb. 2 comb.	7 7	I/O –	prog. prog.
PAL20R8	12	8 reg.	8	reg.	pin
PAL20R6	12	6 reg. 2 comb.	8 7	reg. I/O	pin prog.
PAL20R4	12	4 reg. 4 comb.	8 7	reg. I/O	pin prog.

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PERFORMANCE OPTIONS

(Commercial)

Speed (t_{PD}, ns)			
	35	A-2	
	25	B-2	A
	15		B
	10		-10
	7.5		-7
Power (I_{CC}, mA)		105	210

Note:

For low power and high speed, the EE CMOS PALCE20V8 can directly replace the PAL20R8 Family.

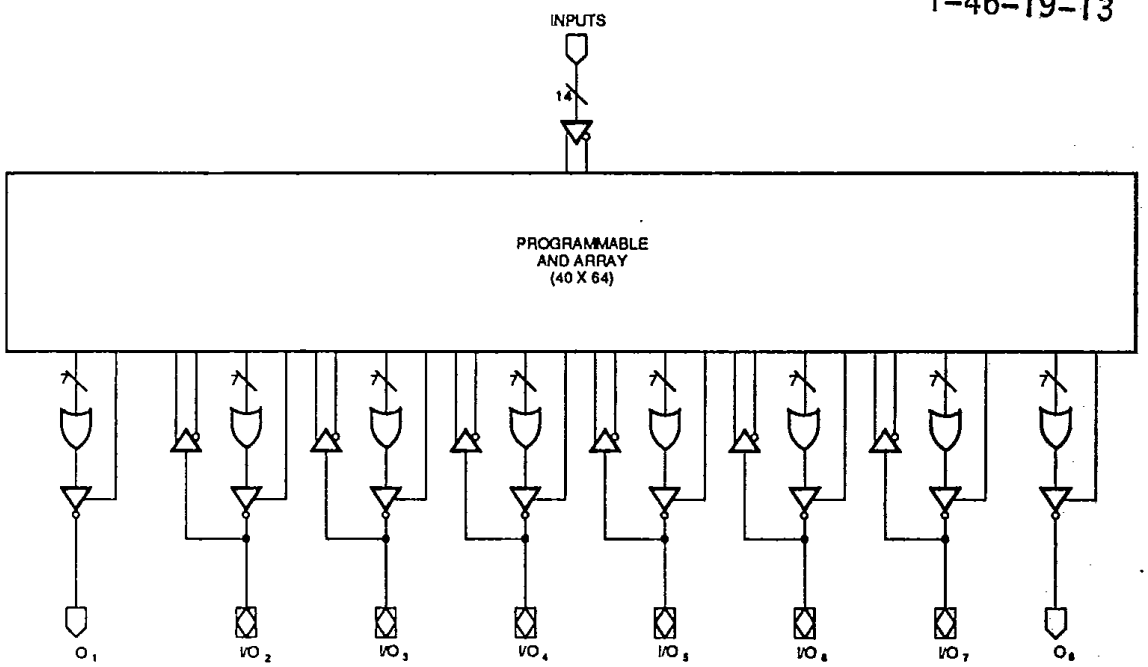
OPERATING RANGES

Commercial	Military
-7	-12
-10	-15
B (15 ns)	B (20 ns)
B-2 (25 ns)	
A (25 ns)	A (30 ns)
A-2 (35 ns)	A-2 (50 ns)

BLOCK DIAGRAMS

T-46-19-13

PAL20L8



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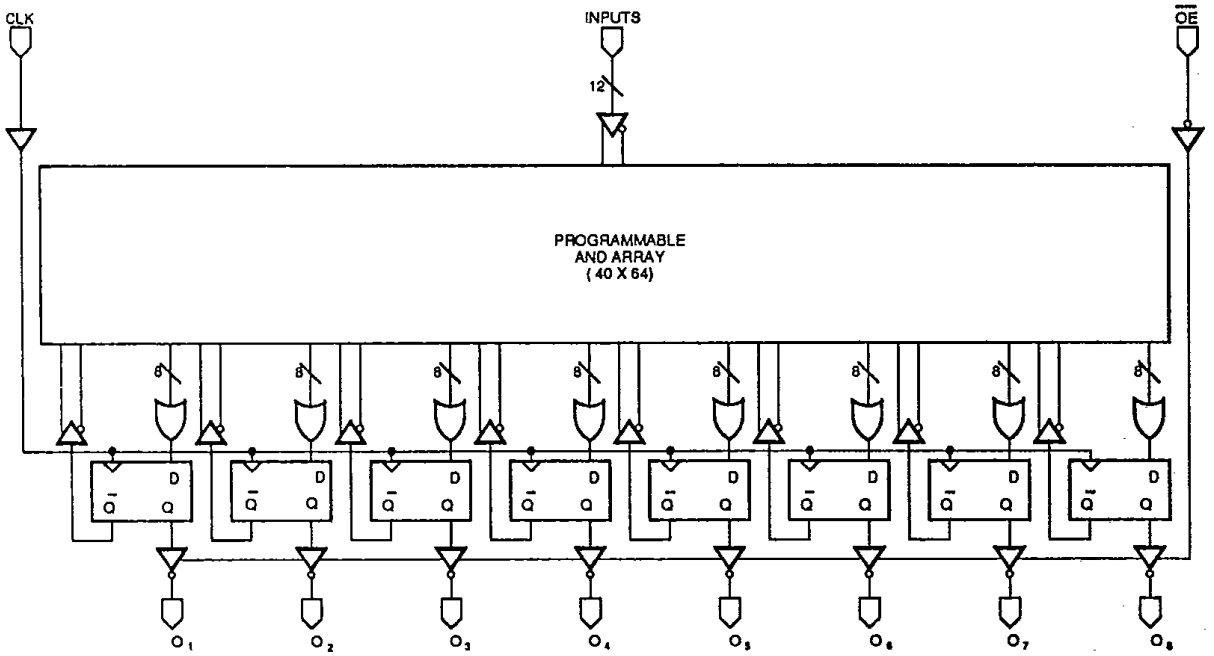
PAL20R8



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BLOCK DIAGRAMS

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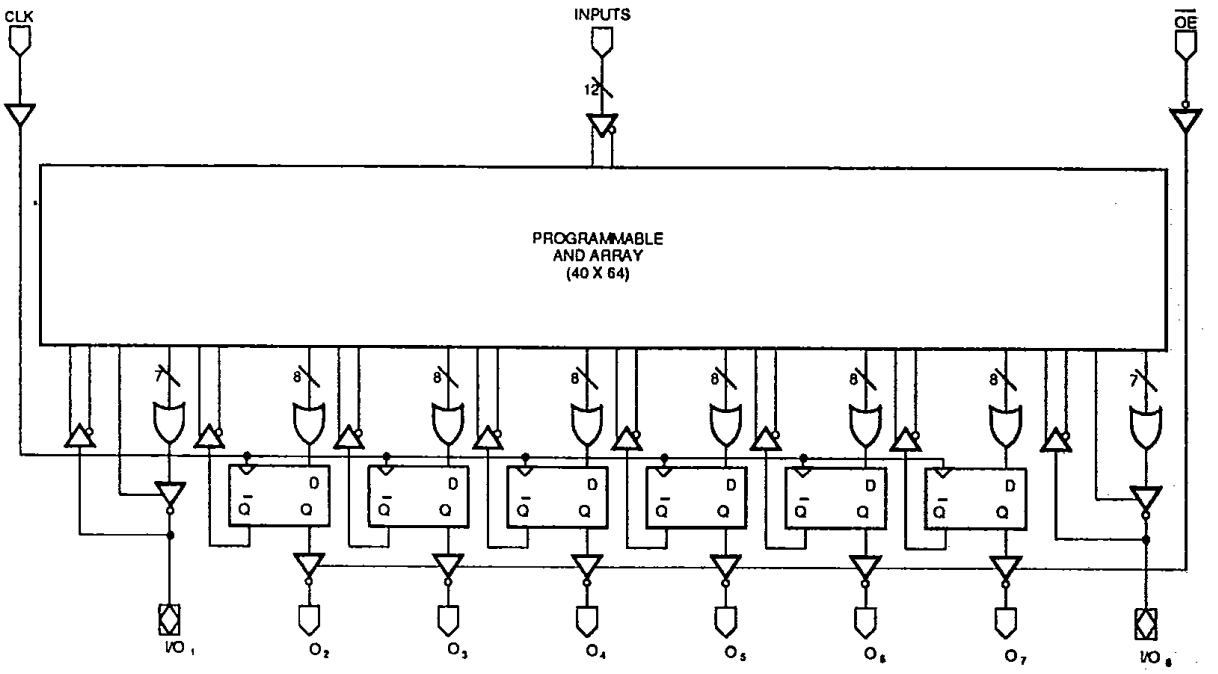
PAL20R6



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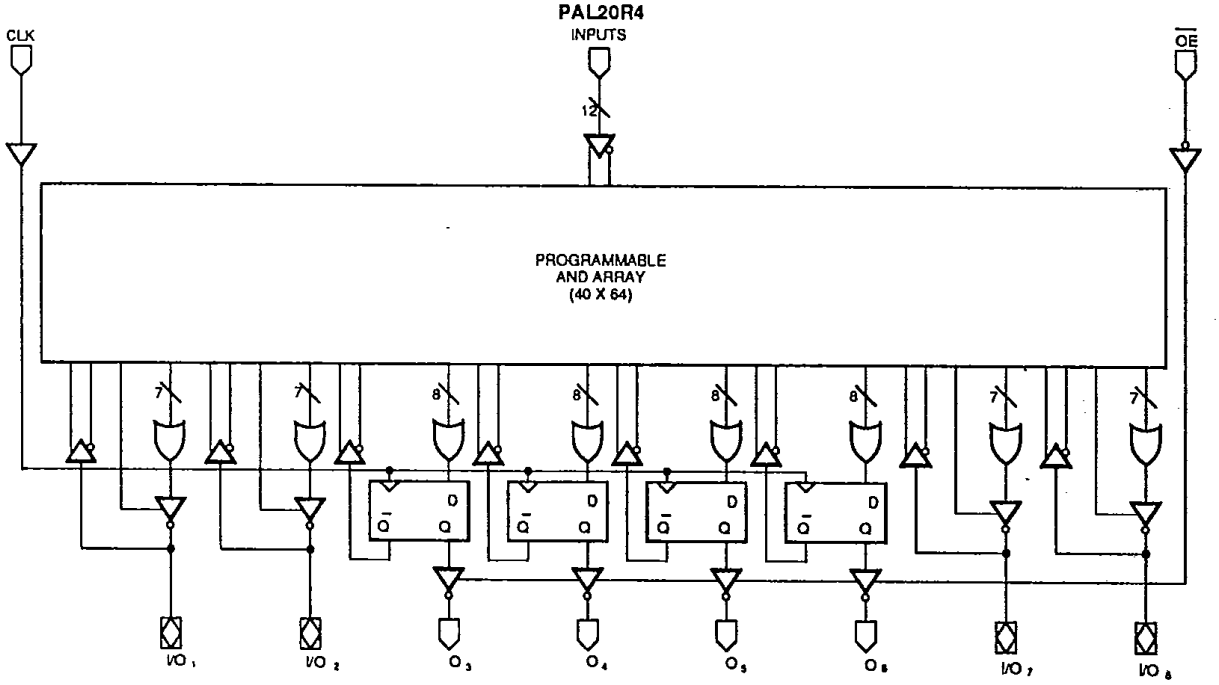
PAL20R4



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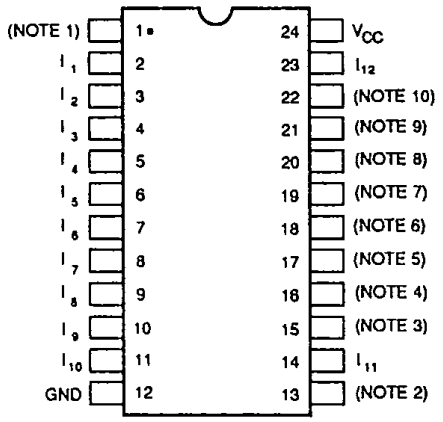
CONNECTION DIAGRAMS
T-46-19-13

Top View

SKINNYDIP/FLATPACK



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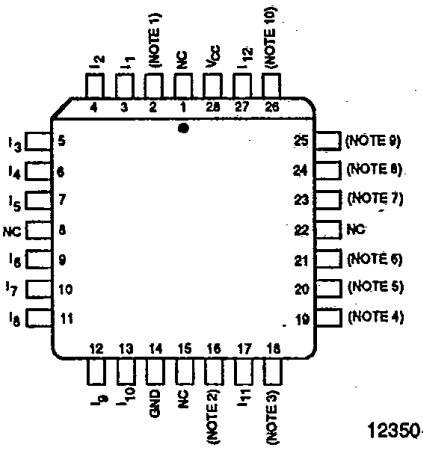
PLCC/LCC

JEDEC: Applies to -7(-12 mil), -10(-15 mil), B-2 Series Only



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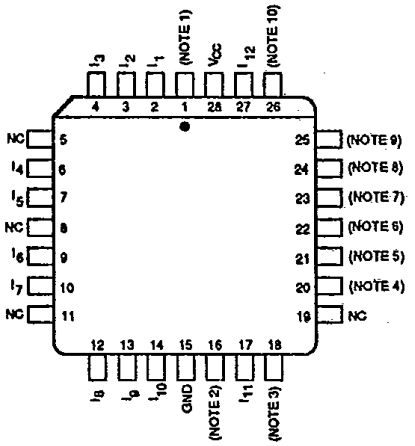
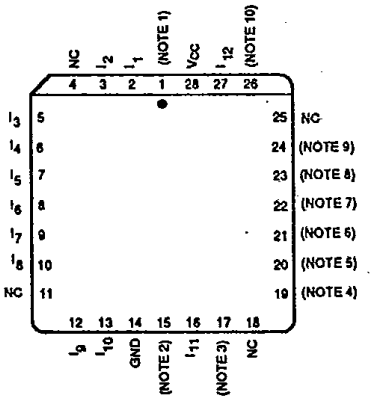
PLCC

Applies to B, A, A-2 Series Only



LCC

Applies to B, A, A-2 Series Only



Note	20L8	20R8	20R6	20R4
1	I_0	CLK	CLK	CLK
2	I_{13}	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
3	O_1	O_1	I/O_1	I/O_1
4	I/O_2	O_2	O_2	I/O_2
5	I/O_3	O_3	O_3	O_3
6	I/O_4	O_4	O_4	O_4
7	I/O_5	O_5	O_5	O_5
8	I/O_6	O_6	O_6	O_6
9	I/O_7	O_7	O_7	I/O_7
10	O_8	O_8	I/O_8	I/O_8

PIN DESIGNATIONS

CLK	Clock
GND	Ground
I	Input
I/O	Input/Output
NC	No Connect
O	Output
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage

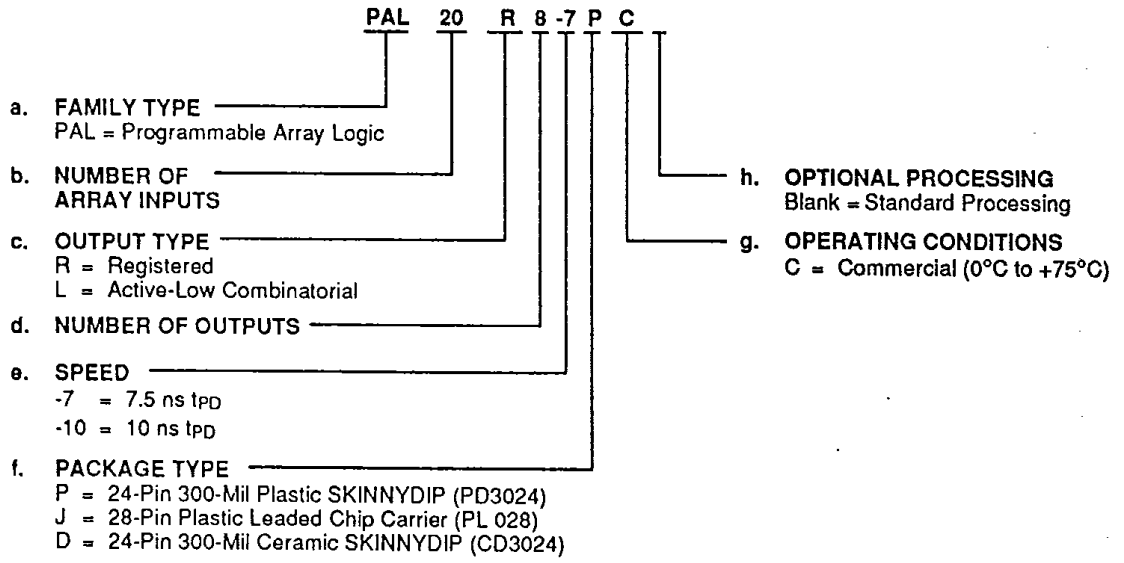
Note:
Pin 1 is marked for orientation.

ORDERING INFORMATION
Commercial Products (AMD Marking Only)

T-46-19-13

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Number of Array Inputs
c. Output Type
d. Number of Outputs
e. Speed
f. Package Type
g. Operating Conditions
h. Optional Processing



Valid Combinations		
PAL20L8	-7, -10	PC, JC, DC
PAL20R8		
PAL20R6		
PAL20R4		

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with AMD logo.

ORDERING INFORMATION
Commercial Products (MMI Marking Only)

T-46-19-13

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Number of Array Inputs
c. Output Type
d. Number of Outputs
e. Speed
f. Power
g. Operating Conditions
h. Package Type
i. Optional Processing

PAL 20 R 8 B -2 C NS

a. **FAMILY TYPE**
PAL = Programmable Array Logic

b. **NUMBER OF ARRAY INPUTS**

c. **OUTPUT TYPE**
R = Registered
L = Active-Low Combinatorial

d. **NUMBER OF OUTPUTS**

e. **SPEED**
B = Very High Speed (15–25 ns t_{PD})
A = High speed (25–35 ns t_{PD})

f. **POWER**
Blank = Full Power (210 mA I_{CC})
-2 = Half Power (105 mA I_{CC})

g. **OPERATING CONDITIONS**
C = Commercial (0°C to +75°C)

h. **PACKAGE TYPE**
NS = 24-Pin 300-Mil Plastic SKINNYDIP (PD3024)
FN = 28-Pin Plastic Leaded Chip Carrier (PL 028), JEDEC pinout
NL = 28-Pin Plastic Leaded Chip Carrier (PL 028), non-JEDEC pinout
JS = 24-Pin 300-Mil Ceramic SKINNYDIP (CD3024)

i. **OPTIONAL PROCESSING**
Blank = Standard Processing

Valid Combinations		
PAL20L8,	B-2	CNS, CFN, CJS
PAL20R8, PAL20R6, PAL20R4	B, A, A-2	CNS, CNL, CJS

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

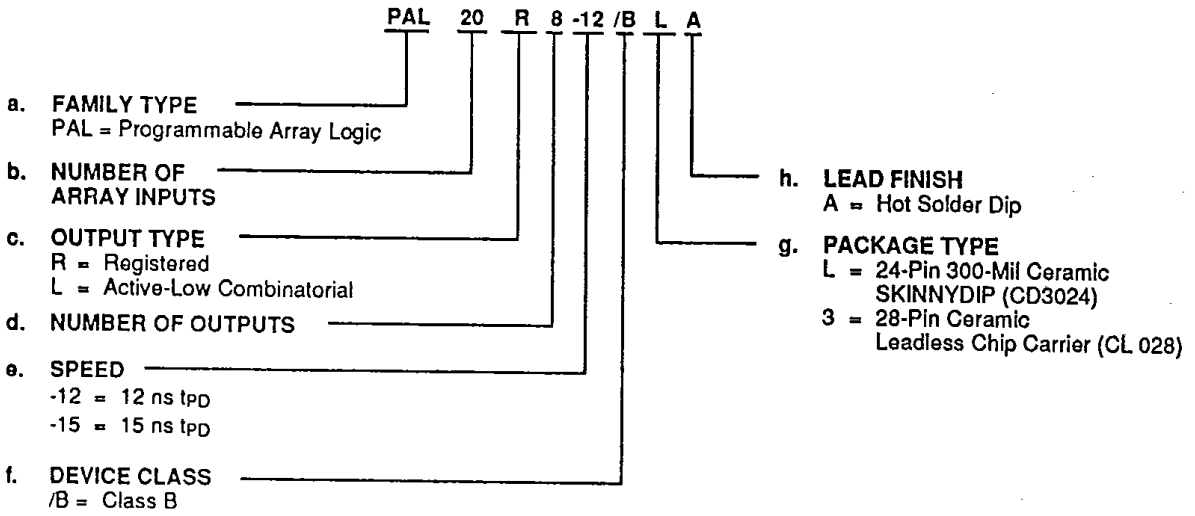
Note: Marked with MMI logo.

ORDERING INFORMATION
APL Products (AMD Marking Only)

T-46-19-13

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Number of Array Inputs
c. Output Type
d. Number of Outputs
e. Speed
f. Device Class
g. Package Type
h. Lead Finish



Valid Combinations		
PAL20L8	-12, -15	/BLA, /B3A
PAL20R8		
PAL20R6		
PAL20R4		

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

Group A Tests

Group A Tests consist of Subgroups: 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.

ORDERING INFORMATION
APL Products (MMI Marking Only)

T-46-19-13

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Number of Array Inputs
c. Output Type
d. Number of Outputs
e. Speed
f. Power
g. Operating Conditions
h. Package Type
i. Optional Processing

PAL 20 R 8 A -2 M JS /883B

a. **FAMILY TYPE**
PAL = Programmable Array Logic

b. **NUMBER OF ARRAY INPUTS**

c. **OUTPUT TYPE**
R = Registered
L = Active-Low Combinatorial

d. **NUMBER OF OUTPUTS**

e. **SPEED**
B = Very High Speed (20 ns t_{PD})
A = High speed (30–50 ns t_{PD})

f. **POWER**
Blank = Full Power (210 mA I_{CC})
-2 = Half Power (105 mA I_{CC})

i. **OPTIONAL PROCESSING**
/883B = MIL-STD-883, Class B

h. **PACKAGE TYPE (Per 09–000)**
JS = 24-Pin 300-Mil Ceramic SKINNYDIP (CD3024)
W = 24-Pin Ceramic Flatpack (CFL024)
L = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

g. **OPERATING CONDITIONS**
M = Military

2

Valid Combinations		
PAL20L8	B, A, A-2	MJS/883B, MW/883B, ML/883B
PAL20R8		
PAL20R6		
PAL20R4		

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with MMI logo.

Group A Tests

Group A Tests consist of Subgroups: 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.

FUNCTIONAL DESCRIPTION

Standard 24-pin PAL Family

The standard 24-pin PAL family is comprised of four different devices, including both registered and combinatorial devices. All parts are produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Information on approved programmers can be found in the Programmer Reference Guide. Extra test words are pre-programmed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve excellent parametric correlation.

Variable Input/Output Pin Ratio

The registered devices have twelve dedicated input lines, and each combinatorial output is an I/O pin. The PAL20L8 has fourteen dedicated input lines, and only six of the eight combinatorial outputs are I/O pins. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. On combinatorial outputs, a product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled. On registered outputs, an input pin controls the enabling of the three-state outputs.

Registers with Feedback

Registered outputs are provided for data storage and synchronization. Registers are composed of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock input.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PAL20R8 Family will be HIGH due to the active-low outputs. The V_{CC} rise must be monotonic and the reset delay time is 1000 ns maximum.

T-46-19-13

Register Preload

Applies to -7 (-12 Mil), -10 (-15 Mil), Series Only

The register on the listed Series can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Fuse

After programming and verification, a PAL20R8 Family design can be secured by programming the security fuse. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is unprogrammed. An exception is the -7 (-12 Mil) Series, where the array will read as if every fuse is programmed.

Pinouts

All members of the PAL20R8 Family have the same SKINNYDIP pinouts independent of technology, performance, and operating conditions. Because the 24-pin SKINNYDIP requires four no-connects when mapped into the 28-pin PLCC/LCC packages, the PLCC/LCC pinouts can vary.

Two different PLCC pinouts are offered. Newer devices and all future devices will follow the JEDEC electronics committee's standard pinout ("JEDEC pinout") with no-connects on pins 1, 8, 15, and 22. The devices following this pinout are the -7, -10, and B-2 Series. Older devices retain their original pinouts, with no-connects on pins 5, 8, 11, and 19. These include the B, A, and A-2 Series.

PAL20R8 Family devices with the MMI marking indicate the PLCC pinout by the package designator: FN indicates JEDEC, and NL indicates non-JEDEC. Devices with the AMD marking all follow the JEDEC pinout.

Two different LCC pinouts are offered for military products. Newer devices and all future devices will follow the JEDEC pinout with no-connects on pins 1, 8, 15, and 22. These include the -12 and -15 Series. Older devices retain their original pinouts, with no-connects on pins 4, 11, 18, and 25. These include the B, A, and A-2 Series.

Series	Com'l PLCC No-connects	Mil LCC No-connects
-7, -10, B-2	1, 8, 15, 22 (JEDEC)	N/A
-12, -15	N/A	1, 8, 15, 22 (JEDEC)
B, A, A-2	5, 8, 11, 19	4, 11, 18, 25

Quality and Testability

T-46-19-13

The PAL20R8 Family offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The high-speed -7 (-12 Mil) and -10 (-15 Mil) Series are fabricated with AMD's advanced oxide-isolated bipolar process. This process reduces parasitic capacitances and minimum geometries to provide higher performance. The array connections are formed with proven PtSi fuses for the -7 and TiW fuses for the -10. The B, B-2, A, and A-2 Series are fabricated with AMD's junction-isolated process, utilizing TiW fuses.

LOGIC DIAGRAM

DIP (JEDEC PLCC and LCC) Pinouts

See Connection Diagrams for B, A, A-2 Series PLCC/LCC Pinouts

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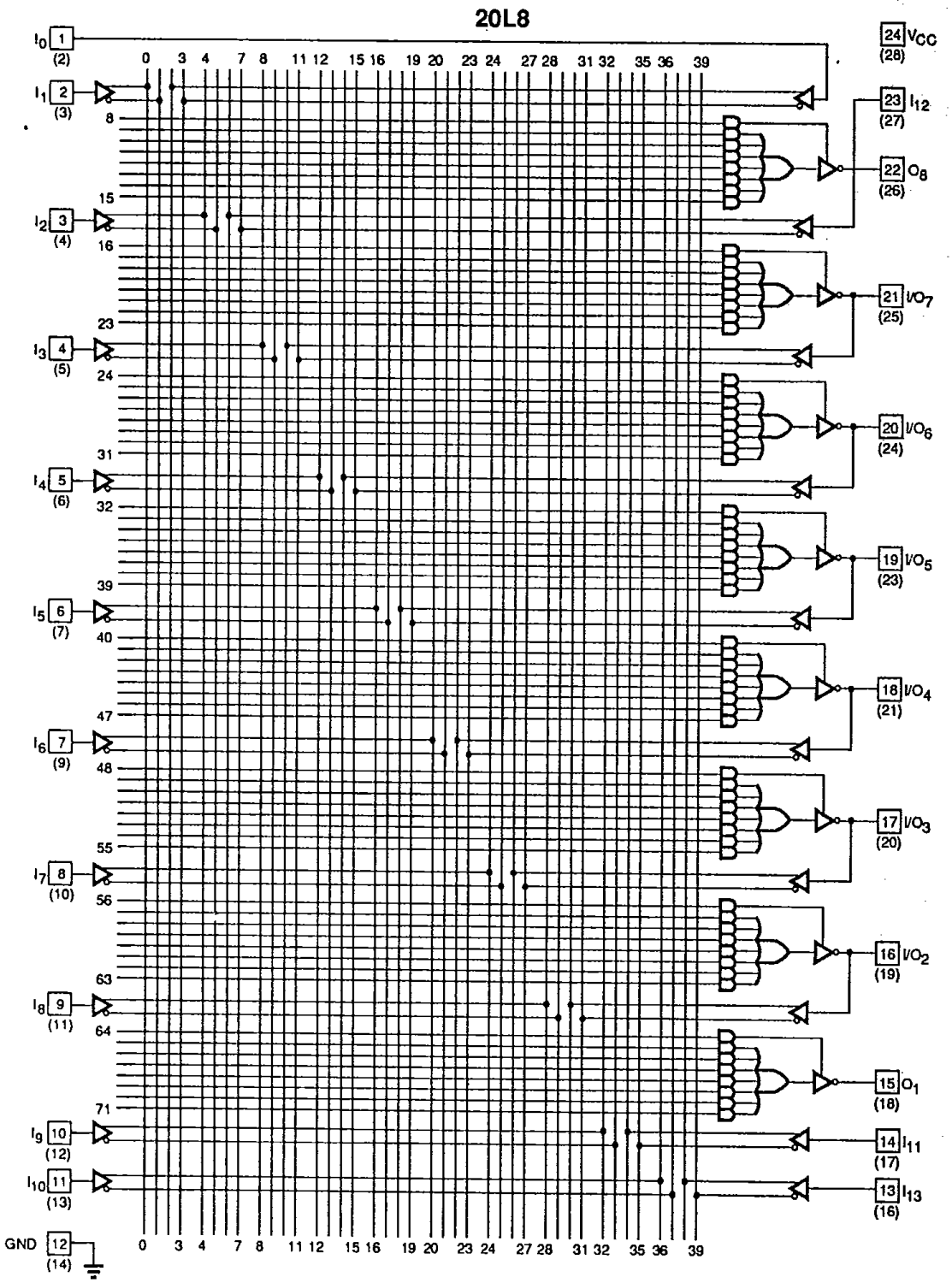

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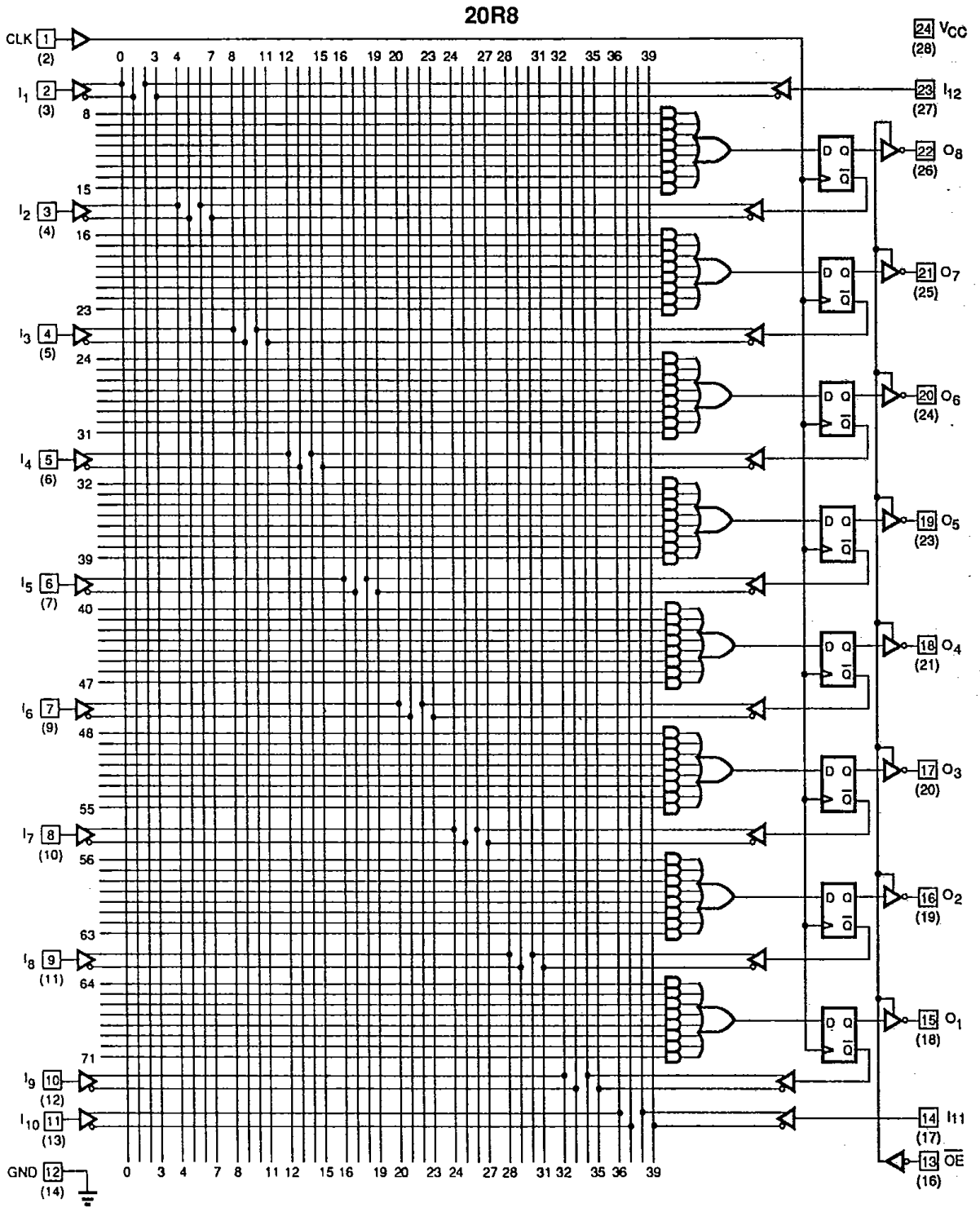
LOGIC DIAGRAM

T-46-19-13

DIP (JEDEC PLCC and LCC) Pinouts

See Connection Diagrams for B, A, A-2 Series PLCC/LCC Pinouts



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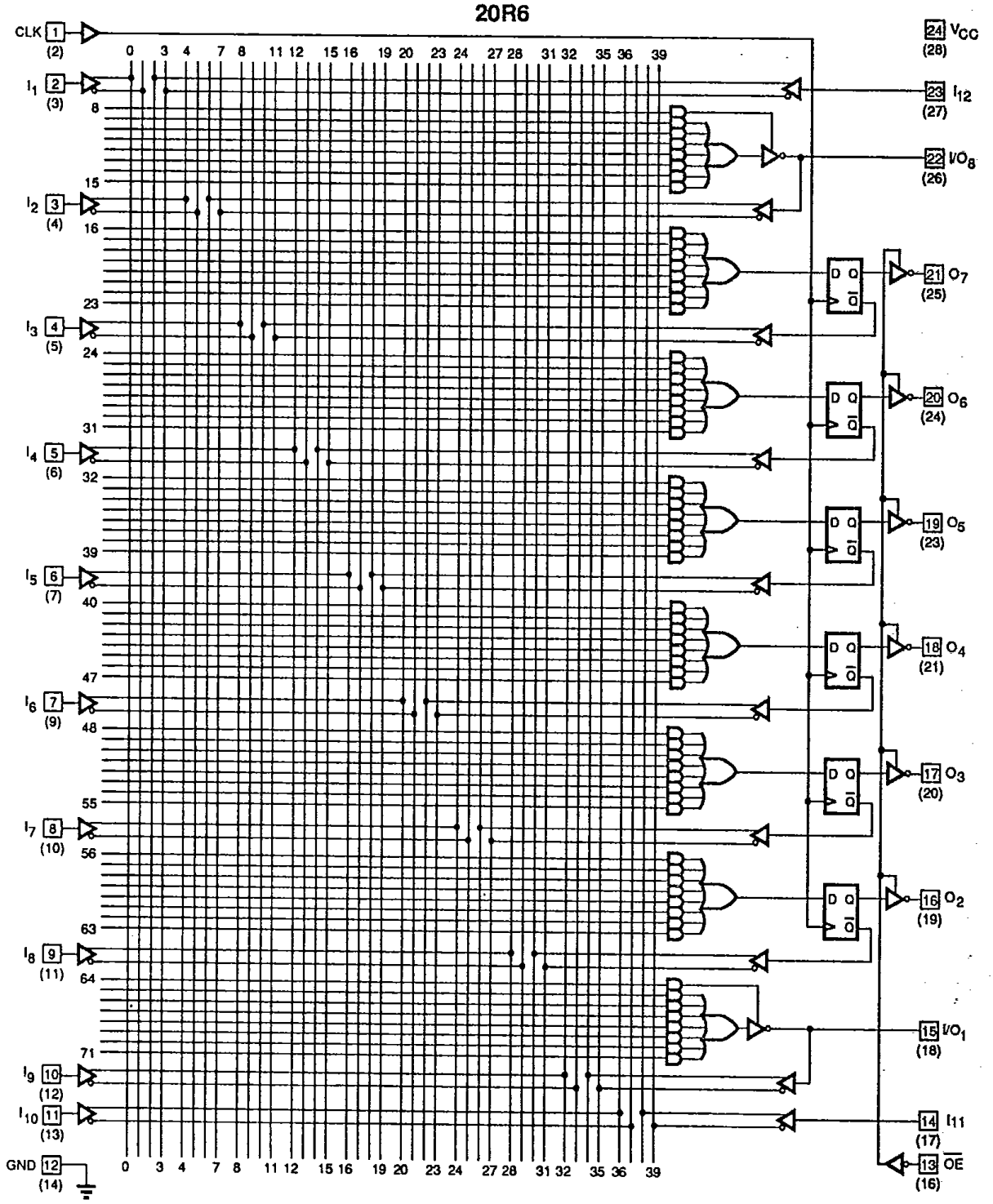
LOGIC DIAGRAM

T-46-19-13

DIP (JEDEC PLCC and LCC) Pinouts

See Connection Diagrams for B, A, A-2 Series PLCC/LCC Pinouts



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LOGIC DIAGRAM

DIP (JEDEC PLCC and LCC) Pinouts

See Connection Diagrams for B, A, A-2 Series PLCC/LCC Pinouts

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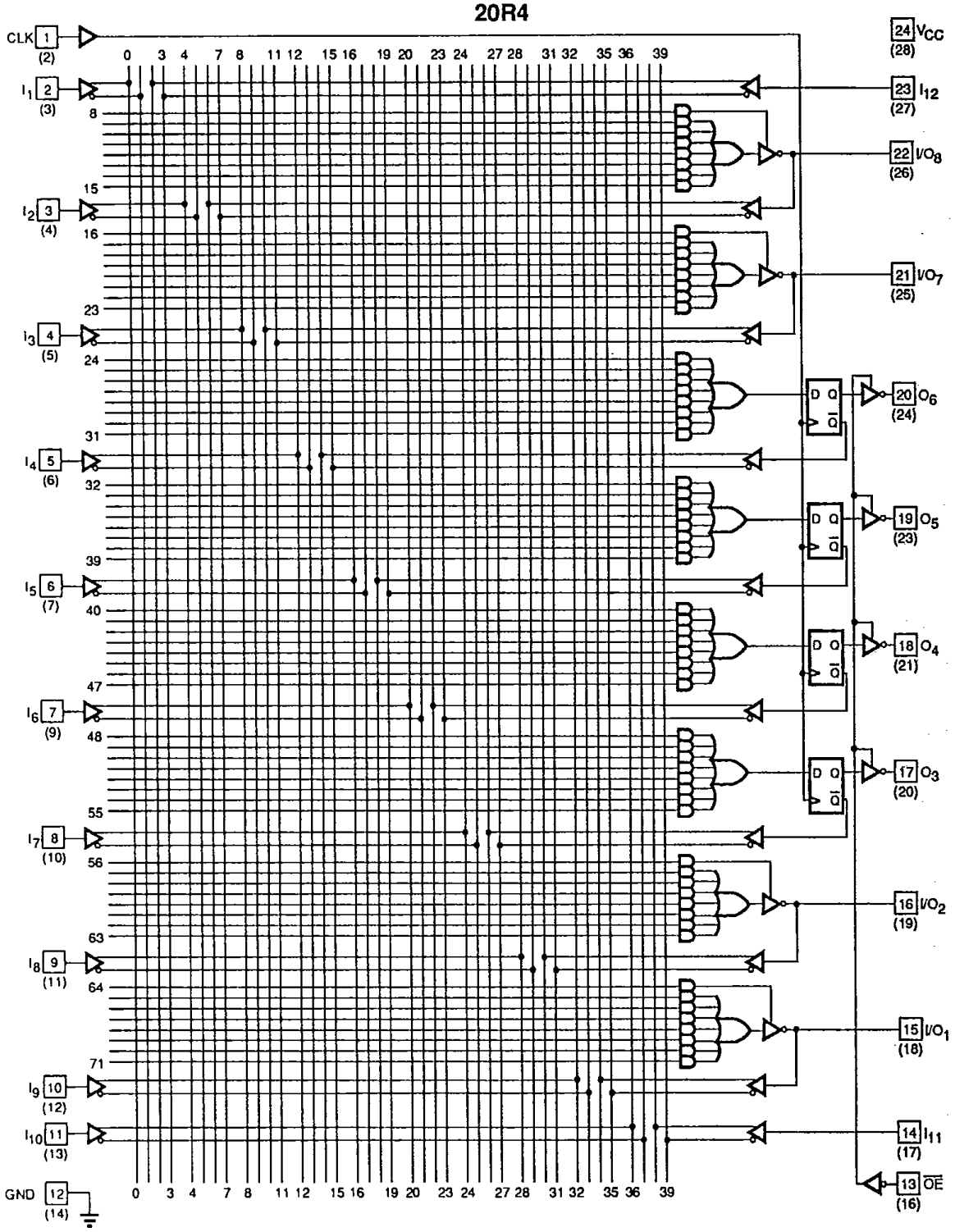
20R4



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ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−1.2 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

T-46-19-13

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = −18 mA, V_{CC} = Min.		−1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		−250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	−30	−130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		210	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

T-46-19-13

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = +25°C f = 1 MHz	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min. (Note 3)	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6	3	7.5	ns
		1 Output Switching		20R4	3	7	
t_S	Setup Time from Input or Feedback to Clock			20R8, 20R6, 20R4	7		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output				3	6.5	ns
t_{CF}	Clock to Feedback (Note 4)					3	ns
t_{SKEW}	Skew Between Registered Outputs (Note 5)					1	ns
t_{WL}	Clock Width	LOW			5		ns
t_{WH}		HIGH			5		ns
f_{MAX}	Maximum Frequency (Note 6)	External Feedback	$1/(t_S + t_{CO})$		74		MHz
		Internal Feedback	$1/(t_S + t_{CF})$		100		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		100		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				3	8	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				3	8	ns
t_{EA}	Input to Output Enable Using Product Term Control			20L8, 20R6	3	10	ns
t_{ER}	Input to Output Disable Using Product Term Control			20R4	3	10	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Output delay minimums are measured under best-case conditions.
4. Calculated from measured f_{MAX} internal.
5. Skew is measured with all outputs switching in the same direction.
6. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.

T-46-19-13

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−1.2 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Operating Case (T_C) Temperature	−55°C to +125°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and −55°C per MIL-STD-883.

PRELIMINARY

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −2 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = −18 mA, V_{CC} = Min.		−1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		−250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	−30	−130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		210	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

T-46-19-13

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = +25°C f = 1 MHz	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		10	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min. (Note 3)	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6	3	12.5	ns
		1 Output Switching		20R4	3	12	
t_S	Setup Time from Input or Feedback to Clock			20R8, 20R6 20R4	12		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output				3	11	ns
t_{CF}	Clock to Feedback (Note 4)					6.5	ns
t_{SKEW}	Skew Between Registered Outputs (Note 5)					1	ns
t_{WL}	Clock Width	LOW			10		ns
t_{WH}		HIGH			8		ns
f_{MAX}	Maximum Frequency (Note 6)	External Feedback	$1/(t_S + t_{CO})$		43.4		MHz
		Internal Feedback	$1/(t_S + t_{CF})$		54		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		55.5		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 7)				3	20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 7)				3	20	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 7)			20L8, 20R6 20R4	3	20	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 7)				3	20	ns

Notes:

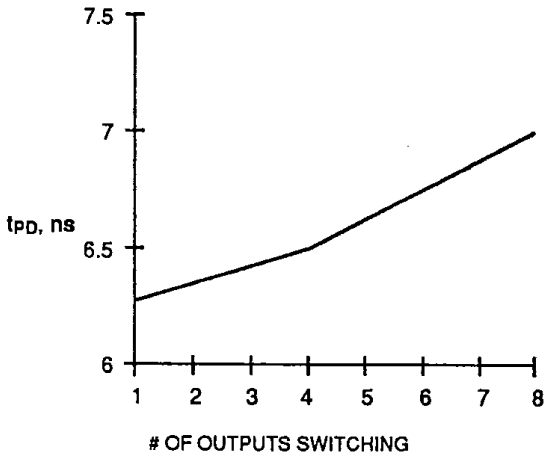
2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. Minimum value for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} parameters should be used for simulation purposes only and are not tested.
4. Calculated from measured f_{MAX} internal.
5. Skew is measured with all outputs switching in the same direction.
6. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
7. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

PRELIMINARY

MEASURED SWITCHING CHARACTERISTICS

V_{CC} = 5.25 V, T_A = 75°C (Note 1)

T-46-19-13



t_{PD} vs. Number of Outputs Switching

10294-005A

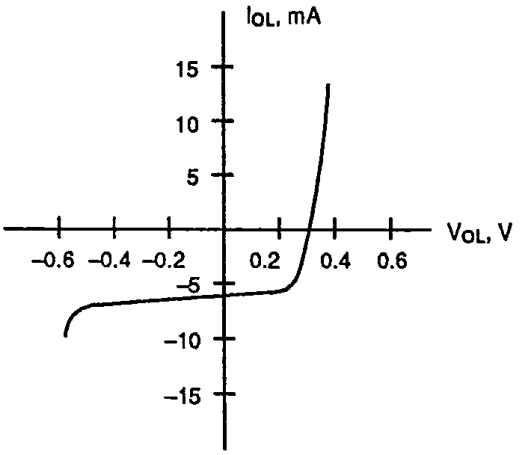
Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where t_{PD} may be affected.

CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

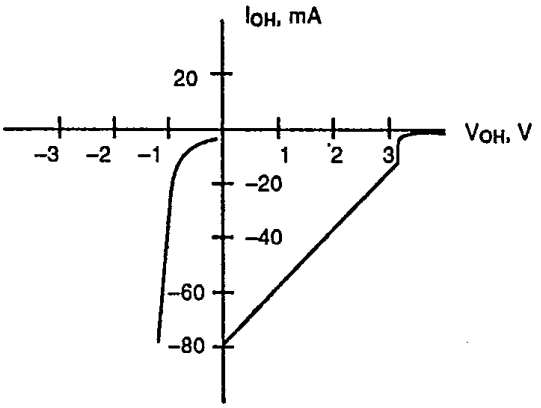
V_{CC} = 5.0 V, T_A = 25°C

T-46-19-13



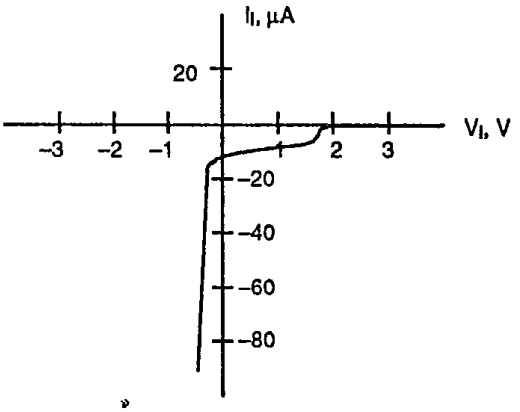
Output, LOW

10240-003A



Output, HIGH

10240-004A



Input

10240-005A

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} Max.
DC Input Current	–30 mA to +5 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

T-46-19-13

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		210	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

T-46-19-13

Parameter Symbol	Parameter Description	Test Conditions			Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V	CLK, $\overline{OE}$	12	pF
			T_A = 25°C	Other Inputs	7	
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	Outputs	8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min. (Note 3)	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6 20R4	3	10	ns
t_S	Setup Time from Input or Feedback to Clock			20R8, 20R6 20R4	10		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output				2	8	ns
t_{CF}	Clock to Feedback (Note 4)					7	ns
t_{WL}	Clock Width	LOW			7		ns
t_{WH}		HIGH			7		ns
f_{MAX}	Maximum Frequency (Note 5)	External Feedback	$1/(t_S + t_{CO})$		55.5		MHz
		Internal Feedback	$1/(t_S + t_{CF})$		58.8		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		71.4		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				1	10	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				1	10	ns
t_{EA}	Input to Output Enable Using Product Term Control			20L8, 20R6 20R4	3	10	ns
t_{ER}	Input to Output Disable Using Product Term Control				3	10	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Output delay minimums are measured under best-case conditions.
4. Calculated from measured f_{MAX} internal.
5. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.

T-46-19-13

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to +5.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} Max.
DC Input Current	−30 mA to + 5 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	−55°C Min.
Operating Case (T_C) Temperature	+125°C Max.
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and −55°C per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = −18 mA, V_{CC} = Min.		−1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		−250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	−30	−130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		210	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

T-46-19-13

Parameter Symbol	Parameter Description	Test Conditions			Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	CLK, $\overline{OE}$	12	pF
				Other Inputs	7	
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		Outputs	8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min. (Note 3)	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6 20R4	3	15	ns
t_S	Setup Time from Input or Feedback to Clock			20R8, 20R6 20R4	15		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output				2	13	ns
t_{CF}	Clock to Feedback (Note 4)					12	ns
t_{WL}	Clock Width	LOW			10		ns
t_{WH}		HIGH			10		ns
f_{MAX}	Maximum Frequency (Note 5)	External Feedback	$1/(t_S + t_{CO})$		35.7		MHz
		Internal Feedback	$1/(t_S + t_{CF})$		37		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		50		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 6)				1	15	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 6)				1	15	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 6)			20L8, 20R6 20R4	3	15	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 6)				3	15	ns

Notes:

2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. Minimum value for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} parameters should be used for simulation purposes only and are not tested.
4. Calculated from measured f_{MAX} internal.
5. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
6. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−1.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

T-46-19-13

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = −18 mA, V_{CC} = Min.		−1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		−250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	−30	−130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		210	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

T-46-19-13

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6 20R4		15	ns
t_S	Setup Time from Input or Feedback to Clock			20R8 20R6 20R4	15		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					12	ns
t_{WL}	Clock Width	LOW			10		ns
t_{WH}		HIGH			12		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$		37		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		45		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					15	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					12	ns
t_{EA}	Input to Output Enable Using Product Term Control			20L8, 20R6 20R4		18	ns
t_{ER}	Input to Output Disable Using Product Term Control					15	ns

Notes:

1. See Switching Test Circuit for test conditions.
2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

FOR CMOS SEE PALCE20V8

T-46-19-13

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to + 5.5 V
DC Output or I/O Pin Voltage	5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	–55°C Min.
Operating Case (T_C) Temperature	+125°C Max.
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and –55°C per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} ≥ 2.4 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		210	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 1)

T-46-19-13

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6 20R4		20	ns
t_S	Setup Time from Input or Feedback to Clock			20R8, 20R6 20R4	20		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					15	ns
t_{WL}	Clock Width	LOW			12		ns
t_{WH}		HIGH			12		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$		28.5		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		41.6		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 3)					20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 3)					20	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 3)			20L8, 20R6 20R4		25	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 3)					20	ns

2

Notes:

1. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

FUTURE DMDS SEE PALCE20V8

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−1.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

T-46-19-13

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = −18 mA, V_{CC} = Min.		−1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		−250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	−30	−130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		105	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

T-46-19-13

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6 20R4		25	ns
t_S	Setup Time from Input or Feedback to Clock			20R8, 20R6 20R4	25		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output					15	ns
t_{CF}	Clock to Feedback (Note 2)					10	ns
t_{WL}	Clock Width	LOW			15		ns
t_{WH}		HIGH			15		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$		25		MHz
		Internal Feedback	$1/(t_S + t_{CF})$		28.5		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		33.3		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					20	ns
t_{EA}	Input to Output Enable Using Product Term Control			20L8, 20R6 20R4		25	ns
t_{ER}	Input to Output Disable Using Product Term Control					25	ns

Notes:

1. See Switching Test Circuit for test conditions.
2. Calculated from measured f_{MAX} internal.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

FOR CMOS SYS PALCE20V8

2

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

T-46-19-13

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		210	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

T-46-19-13

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6 20R4		25	ns
t_S	Setup Time from Input or Feedback to Clock			20R8, 20R6 20R4	25		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output					15	ns
t_{CF}	Clock to Feedback (Note 2)					10	ns
t_{WL}	Clock Width	LOW			15		ns
t_{WH}		HIGH			15		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$		25		MHz
		Internal Feedback	$1/(t_S + t_{CF})$		28.5		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		33		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					20	ns
t_{EA}	Input to Output Enable Using Product Term Control			20L8, 20R6 20R4		25	ns
t_{ER}	Input to Output Disable Using Product Term Control					25	ns

Notes:

1. See Switching Test Circuit for test conditions.
2. Calculated from measured f_{MAX} internal.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

FUNCTIONAL SET PALCE20V8

2

T-46-19-13

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to +5.5 V
DC Output or I/O Pin Voltage	5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	–55°C Min.
Operating Case (T_C) Temperature	+125°C Max.
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and –55°C per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		210	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

AMD CONFIDENTIAL

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 1)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6 20R4		30	ns
t_S	Setup Time from Input or Feedback to Clock			20R8, 20R6 20R4	30		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					20	ns
t_{WL}	Clock Width	LOW			20		ns
t_{WH}		HIGH			20		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$		20		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		25		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 3)					25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 3)					25	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 3)			20L8, 20R6 20R4		30	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 3)					30	ns

Notes:

1. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

PRELIMINARY PALCE20V8

T-46-19-13

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		105	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

T-46-19-13

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6 20R4		35	ns
t_S	Setup Time from Input or Feedback to Clock			20R8, 20R6 20R4	35		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					25	ns
t_{WL}	Clock Width	LOW			25		ns
t_{WH}		HIGH			25		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$		16		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		20		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					25	ns
t_{EA}	Input to Output Enable Using Product Term Control			20L8, 20R6 20R4		35	ns
t_{ER}	Input to Output Disable Using Product Term Control					35	ns

Notes:

1. See Switching Test Circuit for test conditions.
2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

FOR CMOS SEE PALCE20V8

T-46-19-13

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−1.5 V to +5.5 V
DC Output or I/O Pin Voltage	5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	−55°C to +125°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and −55°C per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = −18 mA, V_{CC} = Min.		−1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		−250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	−30	−130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		105	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

PLEASE REF PLA/PLE/ARRAYS

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 1)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6 20R4		50	ns
t_S	Setup Time from Input or Feedback to Clock			20R8, 20R6 20R4	50		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					25	ns
t_{WL}	Clock Width	LOW			25		ns
t_{WH}		HIGH			25		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$		13.3		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		20		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 3)					25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 3)					25	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 3)			20L8, 20R6 20R4		45	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 3)					45	ns

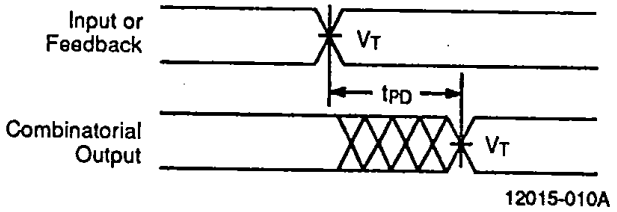
Notes:

1. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

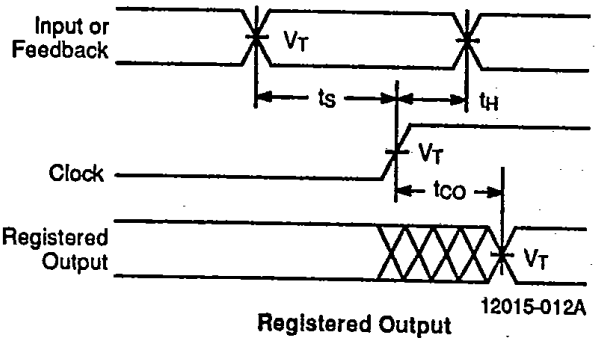
FUTURE SEE PALCE20V8

SWITCHING WAVEFORMS

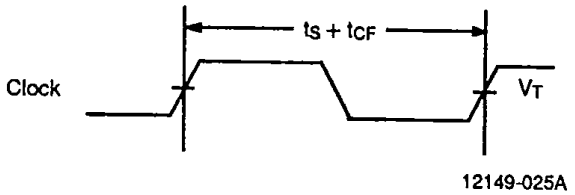
T-46-19-13



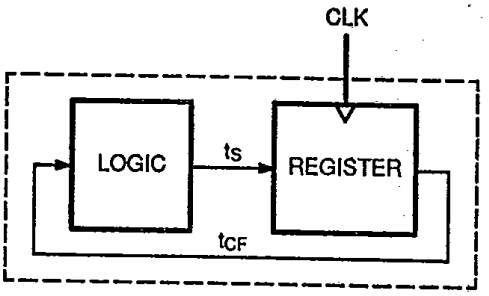
Combinatorial Output

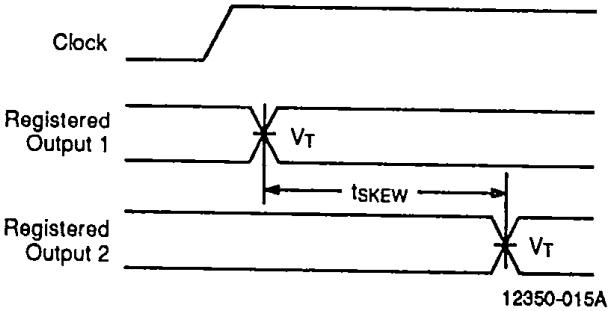


Registered Output

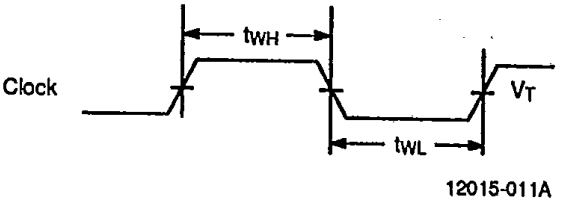


Clock to Feedback (f_{MAX} Internal)
See Path at Right

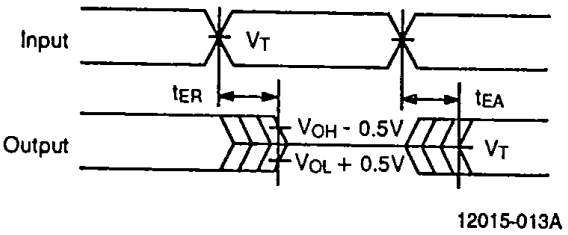




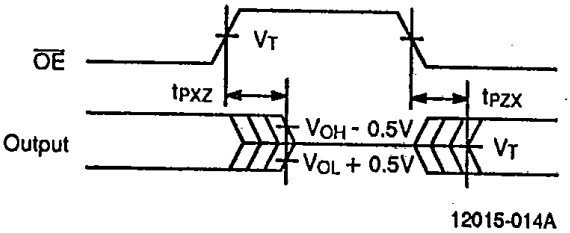
Registered Output Skew for Outputs
Switching in the Same Direction



Clock Width



Input to Output Disable/Enable



$\overline{OE}$ to Output Disable/Enable

Notes:

1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2–5 ns typical.
   (2–4 ns for -7 (-12 Mil) and -10 (-15 Mil) Series)

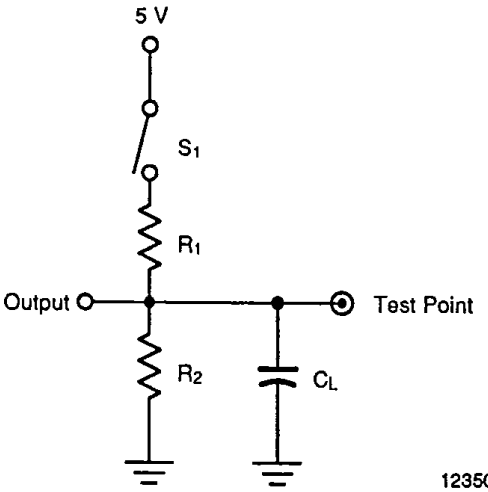
KEY TO SWITCHING WAVEFORMS

T-46-19-13

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT

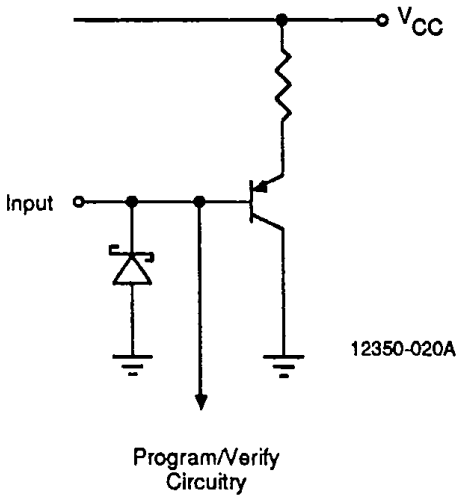


12350-019A

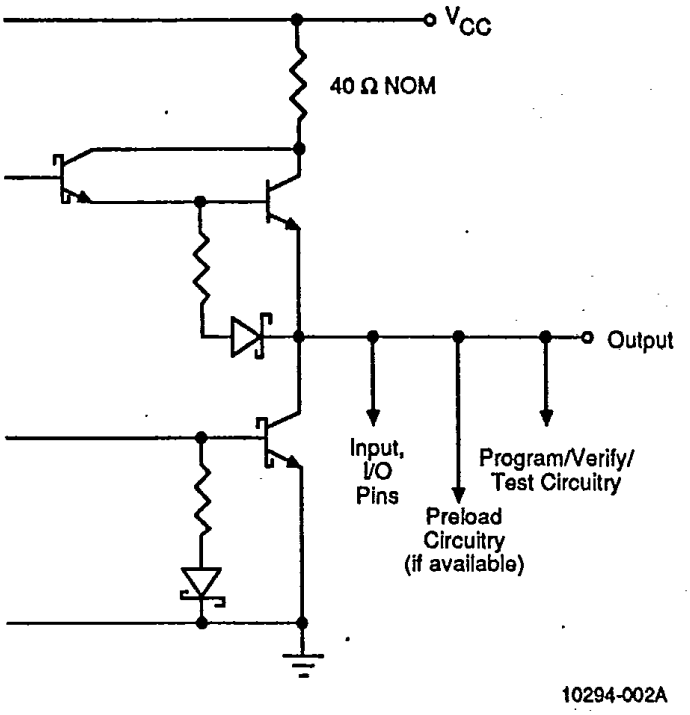
Specification	S_1	C_L	Commercial R_1	Commercial R_2	Military R_1	Military R_2	Measured Output Value
t_{PD}, t_{CO}, t_{CF}	Closed	50 pF	200 Ω	390 Ω	390 Ω	750 Ω	1.5 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed						1.5 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	5 pF					H → Z: V_{OH} − 0.5 V L → Z: V_{OL} + 0.5 V

INPUT/OUTPUT EQUIVALENT SCHEMATICS

Typical Input



Typical Output



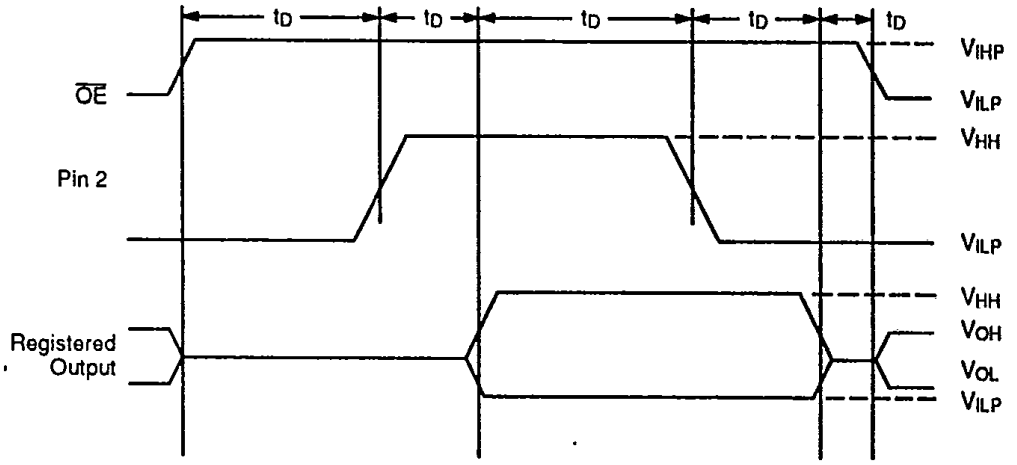
OUTPUT REGISTER PRELOAD

Applies to -7 (-12 Mil) Series Only

The preload function allows the register to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for preloading follows.

1. Raise V_{CC} to V_{CCH}.
2. Set $\overline{OE}$ to V_{IHP} to disable output registers.
3. Raise pin 2 to V_{HH} to enter preload mode.
4. Apply either V_{HH} or V_{ILP} to all registered outputs. Use V_{HH} to preload a LOW in the flip-flop; use V_{ILP} to preload a HIGH in the flip-flop. Leave combinatorial outputs floating.
5. Lower pin 2 to V_{ILP}.
6. Remove V_{ILP}/V_{HH} from all registered output pins.
7. Lower $\overline{OE}$ to V_{ILP} to enable the output registers.
8. Verify V_{OL}/V_{OH} at all registered output pins. Note that because of the output inverter, a register that has been preloaded HIGH will provide a LOW at the output.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{HH}	Super-level input voltage	10	11	12	V
V_{ILP}	Low-level input voltage	0	0	0.5	V
V_{IHP}	High-level input voltage	2.4	5.0	5.5	V
V_{CCH}	Power supply during preload	5.4	5.7	6.0	V
t_D	Delay time	100	200	1000	ns



10294-003A

Output Register Preload Waveform

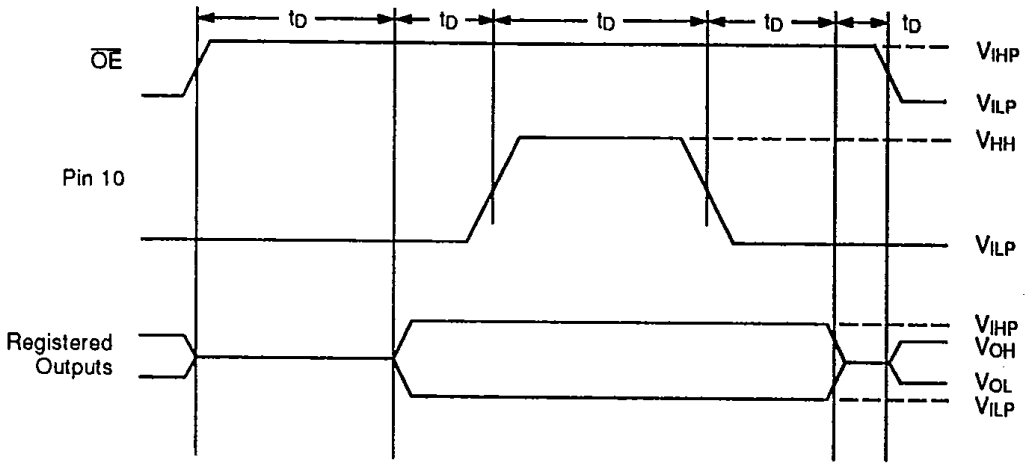
OUTPUT REGISTER PRELOAD

Applies to -10 (-15 Mil) Series Only

The preload function allows the register to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for preloading follows.

1. Raise V_{CC} to 4.5 V.
2. Set $\overline{OE}$ to V_{IHP} to disable output registers.
3. Apply either V_{IHP} or V_{ILP} to all registered outputs. Use V_{IHP} to preload a HIGH in the flip-flop; use V_{ILP} to preload a LOW in the flip-flop. Leave combinatorial outputs floating.
4. Pulse pin 10 to V_{HH}, then back to 0 V.
5. Remove V_{ILP}/V_{IHP} from all registered output pins.
6. Lower $\overline{OE}$ to V_{ILP} to enable the output registers.
7. Verify V_{OL}/V_{OH} at all registered output pins. Note that because of the output inverter, a register that has been preloaded HIGH will provide a LOW at the output.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{HH}	Super-level input voltage	19	20	21	V
V_{ILP}	Low-level input voltage	0	0	0.5	V
V_{IHP}	High-level input voltage	2.4	5.0	5.5	V
t_D	Delay time	100	200	1000	ns



10294-004A

Output Register Preload Waveform

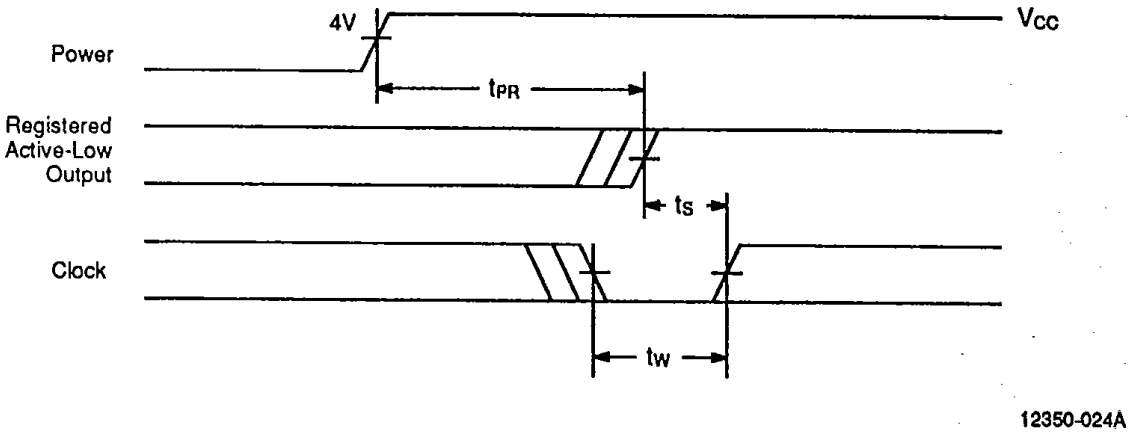
POWER-UP RESET

T-46-19-13

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will be HIGH due to the inverting output buffer. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max.	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform