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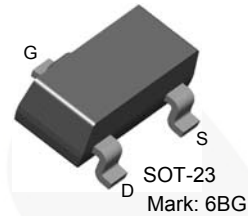
June 2015

# MMBF4416A

## N-Channel RF Amplifier

### Features

- This device is designed for RF amplifiers.
- Sourced from process 50.



### Ordering Information

Part Number	Top Mark	Package	Packing Method
MMBF4416A	6BG	SOT-23 3L	Tape and Reel

### Absolute Maximum Ratings<sup>(1),(2)</sup>

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Value	Unit
$V_{DG}$	Drain-Gate Voltage	35	V
$V_{GS}$	Gate-Source Voltage	-35	V
$I_{GF}$	Forward Gate Current	10	mA
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$

#### Notes:

1. These ratings are based on a maximum junction temperature of  $150^\circ\text{C}$ .
2. These are steady-state limits. Fairchild Semiconductor should be consulted on applications involving pulsed or low-duty-cycle operations.

**Thermal Characteristics<sup>(3)</sup>**

Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Max.	Unit
$P_D$	Total Device Dissipation	225	mW
	Derate Above $25^\circ\text{C}$	1.8	mW/ $^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	556	$^\circ\text{C}/\text{W}$

**Note:**

3. Device mounted on FR-4 PCB 1.6" x 1.6" x 0.06".

**Electrical Characteristics**

Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Max.	Unit
<b>Off Characteristics</b>					
$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	$V_{DS} = 0, I_G = 1.0 \mu\text{A}$	-35		V
$I_{GSS}$	Gate Reverse Current	$V_{GS} = -20 \text{ V}, V_{DS} = 0$		-100	pA
$V_{GS(off)}$	Gate-Source Cut-Off Voltage	$V_{DS} = 15 \text{ V}, I_D = 1.0 \text{ nA}$	-2.5	-6.0	V
$V_{GS}$	Gate-Source Voltage	$V_{DS} = 15 \text{ V}, I_D = 500 \mu\text{A}$	-1.0	-5.5	V
<b>On Characteristics</b>					
$I_{DSS}$	Zero-Gate Voltage Drain Current	$V_{DS} = 15 \text{ V}, V_{GS} = 0$	5	15	mA
$V_{GS(f)}$	Gate-Source Forward Voltage	$V_{DS} = 0, I_G = 1.0 \text{ mA}$		1	V
<b>Small Signal Characteristics</b>					
$g_{fs}$	Forward Transfer Conductance <sup>(4)</sup>	$V_{DS} = 15 \text{ V}, V_{GS} = 0, f = 1.0 \text{ kHz}$	4500	7500	$\mu\text{mhos}$
$g_{os}$	Output Conductance <sup>(4)</sup>	$V_{DS} = 15 \text{ V}, V_{GS} = 0, f = 1.0 \text{ kHz}$		50	$\mu\text{mhos}$
$C_{iss}$	Input Capacitance	$V_{DS} = 15 \text{ V}, V_{GS} = 0, f = 1.0 \text{ MHz}$		4.0	pF
$C_{rss}$	Reverse Transfer Capacitance	$V_{DS} = 15 \text{ V}, V_{GS} = 0, f = 1.0 \text{ MHz}$		0.8	pF
$C_{oss}$	Output Capacitance	$V_{DS} = 15 \text{ V}, V_{GS} = 0, f = 1.0 \text{ MHz}$		2.0	pF
NF	Noise Figure	$V_{DS} = 15 \text{ V}, V_{GS} = 0, I_D = 5 \text{ mA}, R_g = 1 \text{ k}\Omega, f = 400 \text{ MHz}$		4.0	dB

**Note:**

4. Pulse test: pulse width  $\leq 300 \text{ ms}$ , duty cycle  $\leq 2\%$

Physical Dimensions

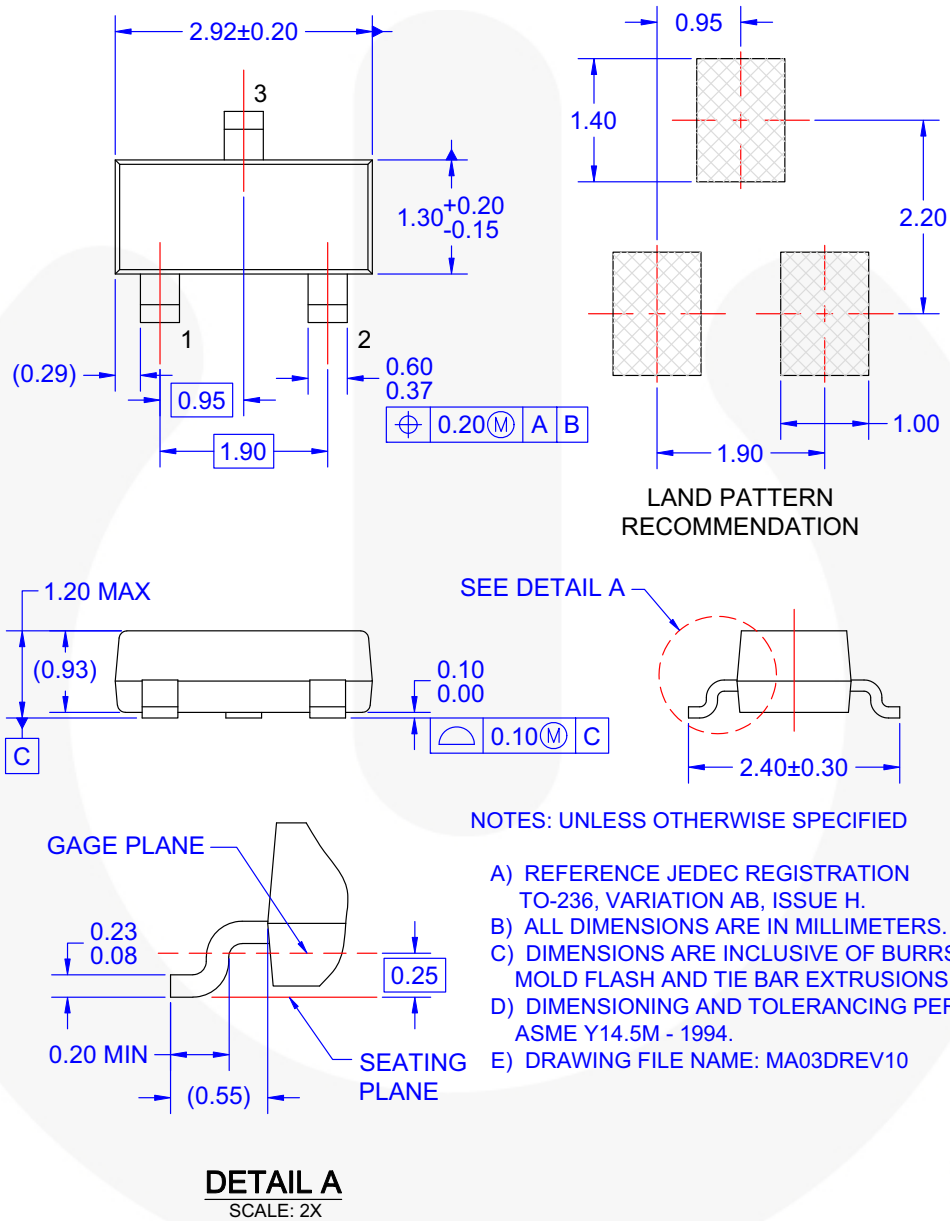







Figure 1. 3-LEAD, SOT23, JEDEC TO-236, LOW PROFILE



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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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