HDK _ _

LVDS Differential **(Non - PLL)**
Jitter **0.2 pS** (typical)

SMD

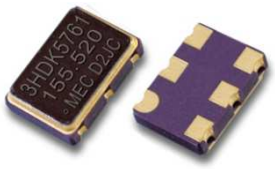
2.5 V | **3.3 V**

Min. **10 MHz**

Max. **200 MHz**

Features

- Femto second integrated phase jitter (200 fs typical , 12 KHz to 20 MHz)
- Supeior phase noise (-138 dBc/Hz at 10 KHz and -144 dBc/Hz at 100 KHz offset)



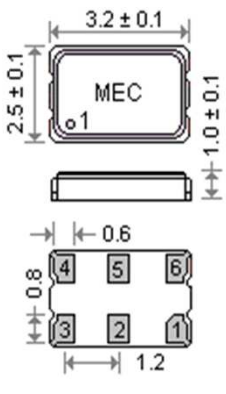
RoHS Compliance

General specifications , at Ta=+25°C , CL=15pF

Output Logic		LVDS Differential		
Model		HDK		
Package (dimensions) unit : mm		HDK 3261 (3.2 * 2.5 * 1.0)	HDK 5361 (5.0 * 3.2 * 1.2)	HDK 5761 (7.0 * 5.0 * 1.8)
Supply Voltage V_{DD}		+2.5 V_{DD} ± 5%		+3.3 V_{DD} ± 5%
Available Frequency Range	min.	13.5 MHz		
	max.	200.0 MHz		
Integrated Phase Jitter (12 KHz to 20 MHz)		0.2 ps typical; 0.5 ps max. [For 156.250 MHz , 3.3V]		
Current Consumption		16 mA typical , 27 mA max.		
Rise Time / Fall Time (20%↔80% of the PECL wave form)		0.2 ns typical , 0.4 ns max.		
SSB Phase Noise [dBc / Hz (typical)]		Offset	62.5 MHz (3.3V)	156.250 MHz (3.3V)
		10 Hz	-50	-50
		100 Hz	-82	-80
		1 KHz	-116	-115
		10 KHz	-138	-135
		100 KHz	-144	-142
		1 MHz	-149	-147
		10 MHz	-155	-152
Output Logic " High " , " 1 "		1.4 V (typical) ; 1.6 V (max.) , RL = 100 Ω ,		
Output Logic " Low " , " 0 "		0.9 V (min.) ; 1.1 V (typical) , RL = 100 Ω ,		
Output Voltage Swing		250 mV min. , 350 mV typ. , 450 mV max. , RL = 100 Ω ,		
Load		100 Ω between output and complimentary output		
Start-up Time		5.0 ms typical , 10 m sec. (max.)		
Duty Cycle		50% ± 5% (measured at V_{DD} -1.25V)		
Storage Temperature		-55°C to + 150°C		
Aging at Ta = +25°C		± 3 ppm max. first year ; ± 2 ppm max. per year thereafter		
Frequency Stability Codes		Frequency Stability over Operating Temperature Range	± 25 ppm	± 50 ppm / ± 100 ppm
		Commercial (*-10°C to +70°C*)	*A*	*B* / *C*
		Industrial (*-40°C to +85°C*)	*D*	*E* / *F*
		If non-standard, please enter the desired stability after the " C " or " I " represents . For example : " C20 " ± 20 ppm over -10°C to +70°C ; " I30 " ± 30 ppm over -40°C to +85°C		
Tri - State Function. 5761 on pad No. 1	No Connection	Differential LVDS and compliantary LVDS outputs .		
	Disable	Both outputs are disabled (high impedance) when the Tri-state pad taken below 0.45*Vcc referenced to ground (threshold) Oscillator is always On . Only buffer stage is disabled . Disable current : 50 uA max. (at 0.0V) , Disable time : 10 ns (max.)		
	Enable	At disabled mode , both outputs are enabled when Tri-state pad is taken above 0.45*Vcc referenced to ground (threshold) ; Enable time : 10ns + one period of the output frequency (max.)		

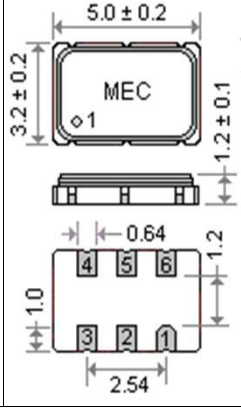
Outline Dimensions (Unit : mm) , Suggested pad Layout for SMDs

HDK3261



Pad 1 : Tri - state
Pad 2 : No Connection
Pad 3 : Ground
Pad 4 : Output
Pad 5 : Complementary
Pad 6 : Supply Voltage

HDK5361



Pad 1 : Tri - state
Pad 2 : No Connection
Pad 3 : Ground
Pad 4 : Output
Pad 5 : Complementary
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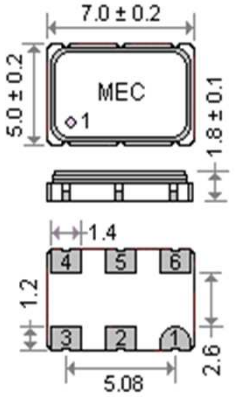
HDK5761



pad 1 : Tri - state
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